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PAM-FM GROUND STATION
(G-A AND VIBRATION)

VOLUME II
THEORY OF OPERATION AND MAINTENANCE

(FIRST REVISION)

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FOREWORD

This instruction manual on the PAM-FM Ground Station has been prepared as a guide to the operation and maintenance of the Vibration and G-A Ground Station developed under Contract AF 04(647)-347. It is divided into two volumes: Vol. I, Installation, Checkout, and Operation; Vol. II, Theory of Operation and Maintenance.

Volume I is published in two parts. Part 1 describes the installation, checkout, and operation procedures for the trailer-mounted station at Atlantic Missile Range (Patrick Air Force Base). Part 2 describes the installation, checkout, and operation procedures applicable at locations where the ground station is installed on a permanent or semi-permanent basis. Part 2 constitutes a manual of instruction for a complete ground station with record, reproduce, and display capabilities for Vibration and G-A signals. Operators can use the instructions that apply to their installation capabilities and ignore instructions that do not apply. Thus, if capabilities at a specific installation should change, appropriate instructions for installation, checkout, and operation will be available.

Volume II, published as a single unit, contains a description of the theory of operation for a ground station having record and reproduce capabilities for Vibration and G-A and specific information designed to assist the operator in maintenance of the equipment.

Instruction manuals for operation and maintenance of components supplied by manufacturers other than Lockheed Missiles and Space Division are also furnished to each station.

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Section 7
THEORY OF OPERATION

7.1 INTRODUCTION

The purpose of the PAM-FM Ground Station is to receive, process, record, and present for on-line, real-time readout PAM-FM telemetered information from a vehicle. Certain Ground Station installations are capable of reproducing the recorded information for delayed readout on visual-display equipment. The Ground Station consists of a Receiver, Base Band Unit, Demultiplexer, Digitizer (Datrac), Record and Reproduce Electronics, a Magnetic Tape Recorder, Sample and Hold Output circuitry, and in the case of Vibration operation, a Visual Display Unit (Visicorder).

The input to the receiver of the Ground Station is a PAM-FM signal. The receiver output is an amplitude-modulated pulse train proportional to the pulse train delivered to the vehicle transmitter by the vehicle multiplexer. This pulse train is amplified, band-limited, and delivered to the Datrac for digitization. Each pulse of the pulse train, including the sync intervals, is digitized into a nine-bit binary word and delivered to the Magnetic Tape Recorder for parallel recording in Non-Return-to-Zero (NRZ) form. The pulse train is also delivered to the Demultiplexer for separation into individual channels corresponding to the channels of the vehicle multiplexer. The information from the Demultiplexer is used for real-time readout on visual display equipment.

In the reproduce mode of operation, the recorded binary words are delivered to the Datrac for conversion to analog form. This analog pulse train is delivered to the Demultiplexer for separation into individual channels corresponding to the channels of the vehicle multiplexer. The information from the Demultiplexer is then used for delayed readout on visual display equipment. The Visual Display Unit (Visicorder)

for Vibration is included at certain installations as a part of the Ground Station. Visual display equipment for G-A is not included as a part of the Ground Station and is not discussed in this manual. Block diagrams illustrating the signal flow in record and reproduce modes of operation for the Vibration and G-A systems are shown in Figs. 7-1, 7-2, 7-3, and 7-4.

Since two data links, Vibration and G-A, are included in this Ground Station manual, characteristics peculiar to each are described briefly in paragraphs 7.1.1 and 7.1.2. The theory of operation for Vibration is described in detail in paragraph 7.2, and for G-A in paragraph 7.3. Procedural instructions for maintenance are detailed in Section 8.

7.1.1 Vibration

The Vibration data link is a PAM-FM communication system so arranged that it can operate with seven high-frequency data channels with a bandwidth of 2000 cps each or with six high-frequency data channels with a bandwidth of 2000 cps each and seven subcommutated data channels with a bandwidth of 250 cps each. This system has a sampling rate of 40,000 samples per second and a 50 percent duty cycle. In addition to the data channels, there is a subframe sync channel and an alternating frame sync. This alternating frame sync channel provides additional reliability as well as zero data calibrate.

Channel 1 is reserved for a main channel sync interval and a calibrate pulse. These pulses appear on alternate frames. Channel 8 is subcommutated into eight channels. Of these channels, 8.1 is the subcommutated sync interval and Channels 8.2 through 8.8 are subcommutated data channels. When subcommutated channels are not used, Channel 8 operates as a high-frequency information channel without a sync interval.

With a basic clock rate of 40 kc, an information pulse occurs every 25 microseconds. A complete cycle, going through eight permutations of the subcommutated channel, requires 1600 microseconds. During this 0.0016-second period, each subcommutated

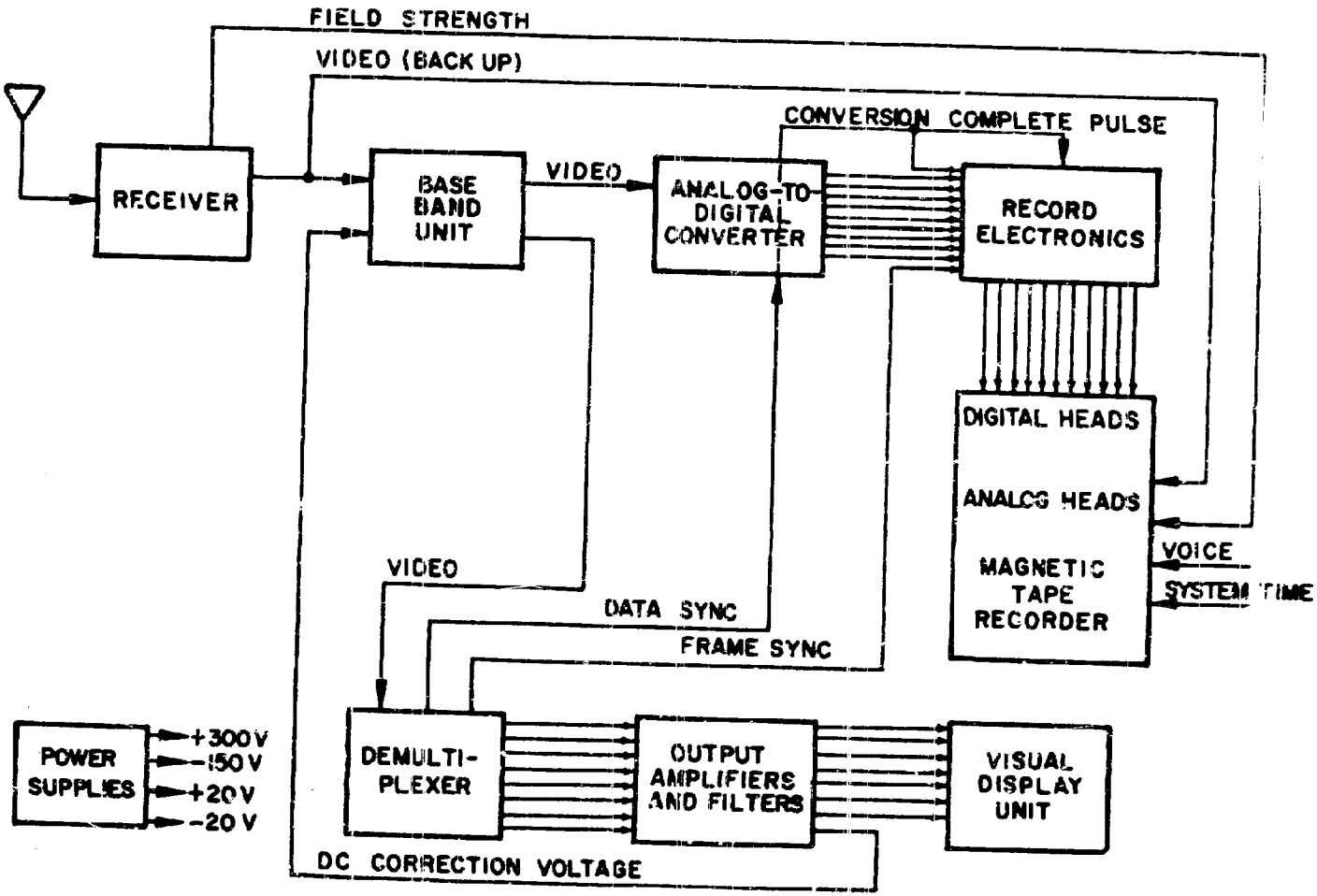


Fig. 7-1 Vibration PAM-FM Ground Station, Record Mode

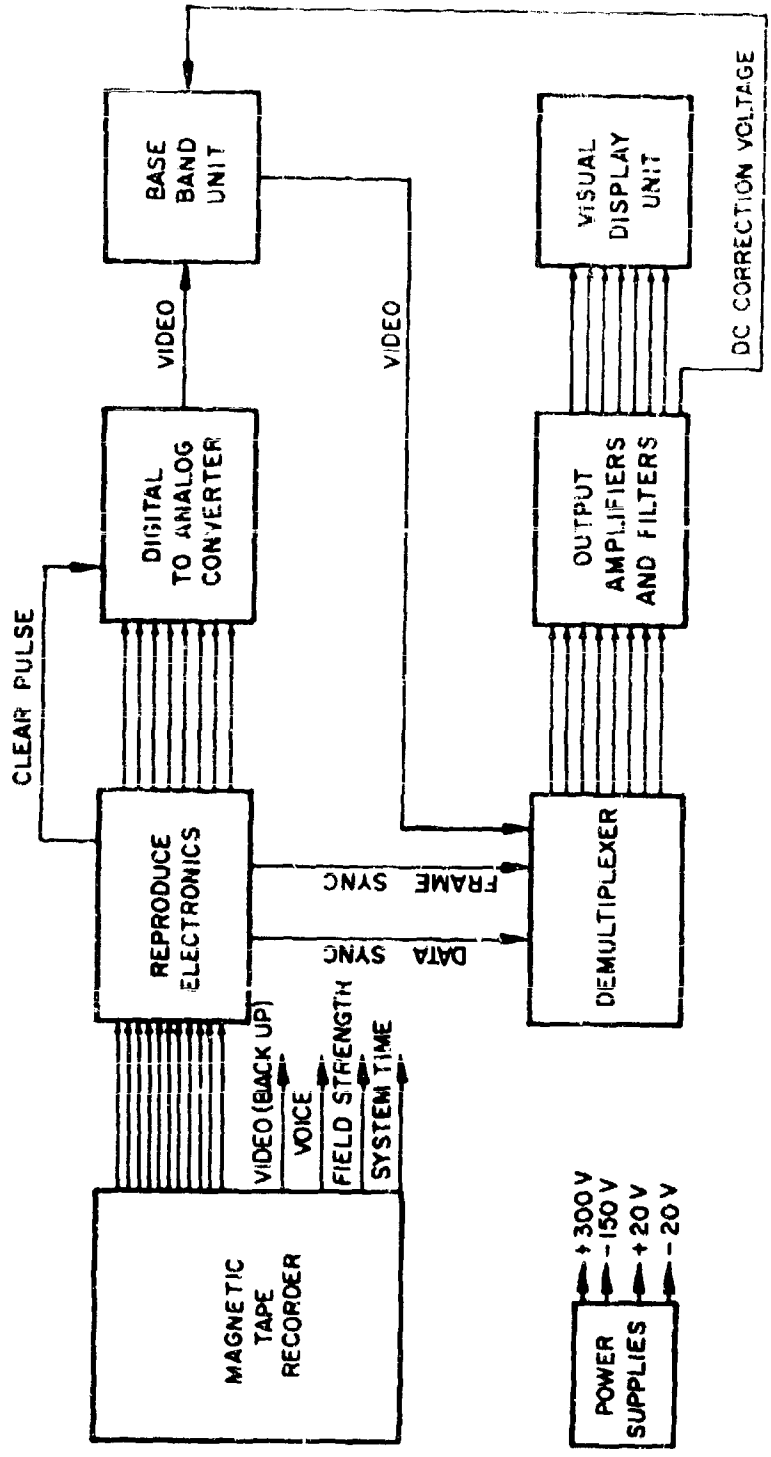


Fig. 7-2 Vibration PAM-FM Ground Station, Reproduce Mode

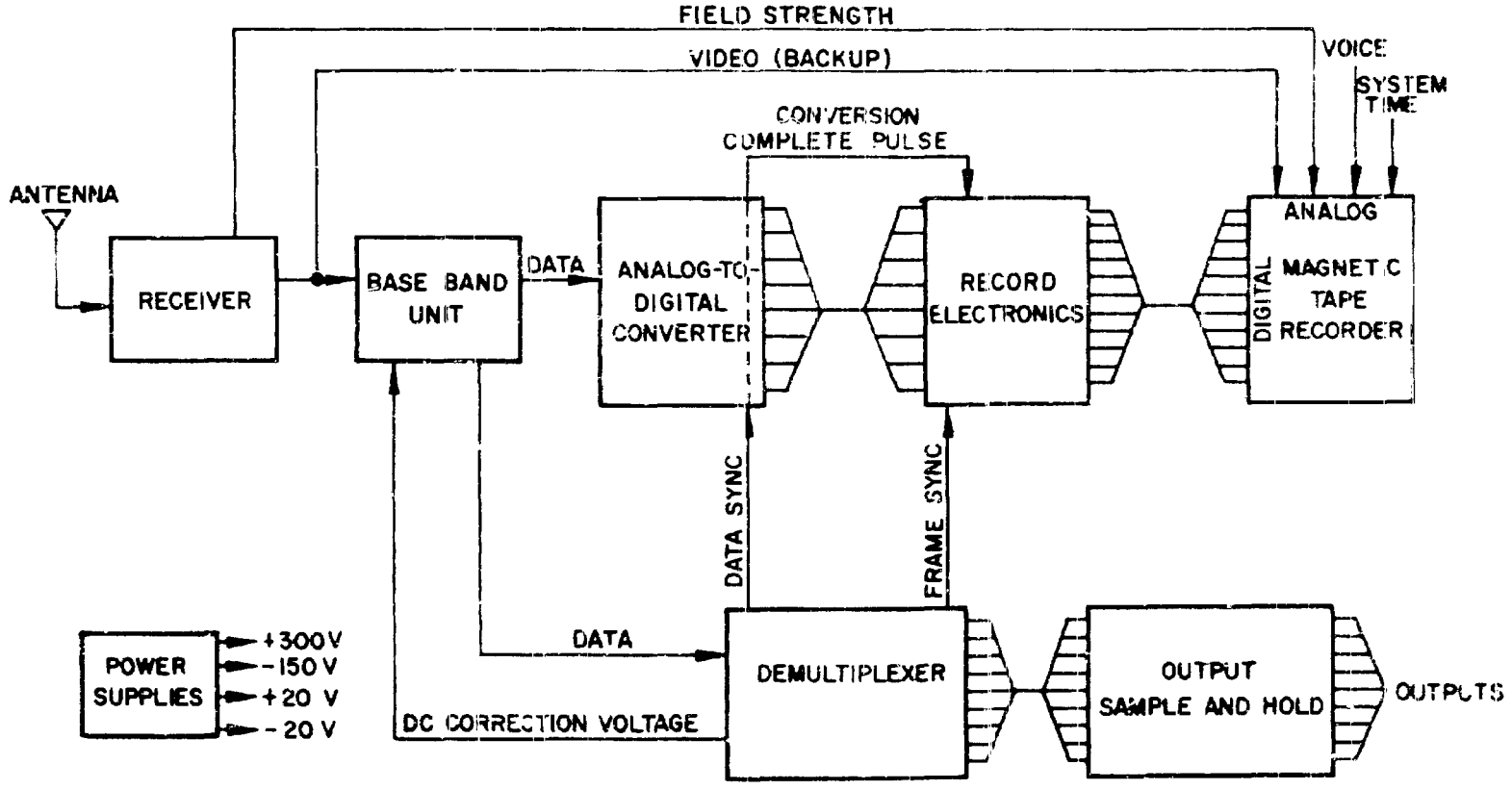


Fig. 7-3 G-A PAM-FM Ground Station, Record Mode

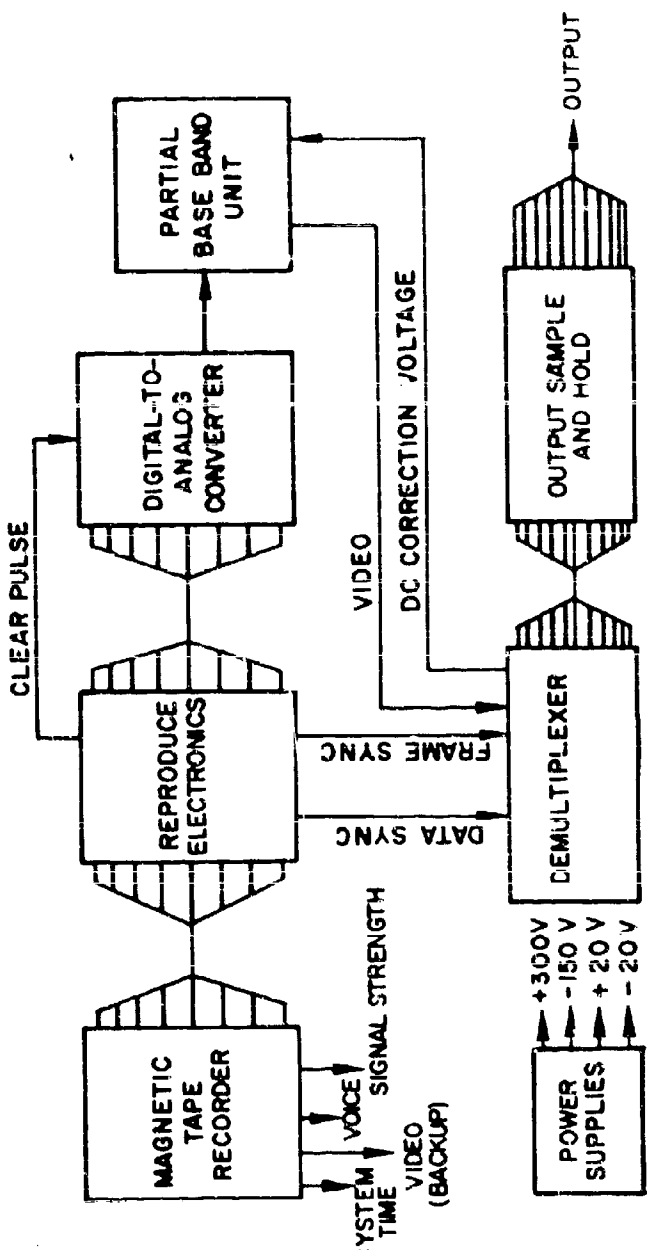


Fig. 7-4 C-A PAM-FM Ground Station, Reproduce Mode

channel will produce one bit of information at a rate of 625 samples per second, and each high-frequency channel will produce eight bits of information at a rate of 5000 samples per second. There are eight information pulses (one frame) every 200 microseconds. Each main channel is equally spaced in time, and each subcommutated channel is equally spaced in time.

A typical Vibration pulse train (Fig. 7-5) has these characteristics with respect to Demultiplexer input:

- Reference level of 0 volts (sync interval)
- Minimum data level of 1.5 volts (corresponding to -2.5-volt input to the vehicle multiplexer)
- Calibrate pulse level of 4.0 volts (corresponding to 0-volt input to the vehicle multiplexer)
- Maximum data level of 6.5 volts (corresponding to +2.5-volt input to the vehicle multiplexer)

7.1.2 G-A

The G-A data link is a PAM-FM communication system arranged to have 29 channels with a bandwidth of 200 cps each and seven channels with a bandwidth of 25 cps each. Two additional 200-cps channels and an additional 25-cps channel are used for synchronization. This PAM information has a composite sampling rate of 16,000 samples per second and a 50-percent duty cycle. By the use of a subcommutated channel, the G-A system handles 36 channels of information. Of these, 29 are high-frequency, or direct data channels, and seven are low-frequency, or subcommutated data channels.

With the basic clock rate of 16 kc, an information pulse occurs every 62.5 microseconds. A complete cycle, going through the eight permutations of the subchannel, requires 16,000 microseconds. During this .016-second period, each subcommutated channel will produce one bit of information at the rate of 62.5 samples per second,

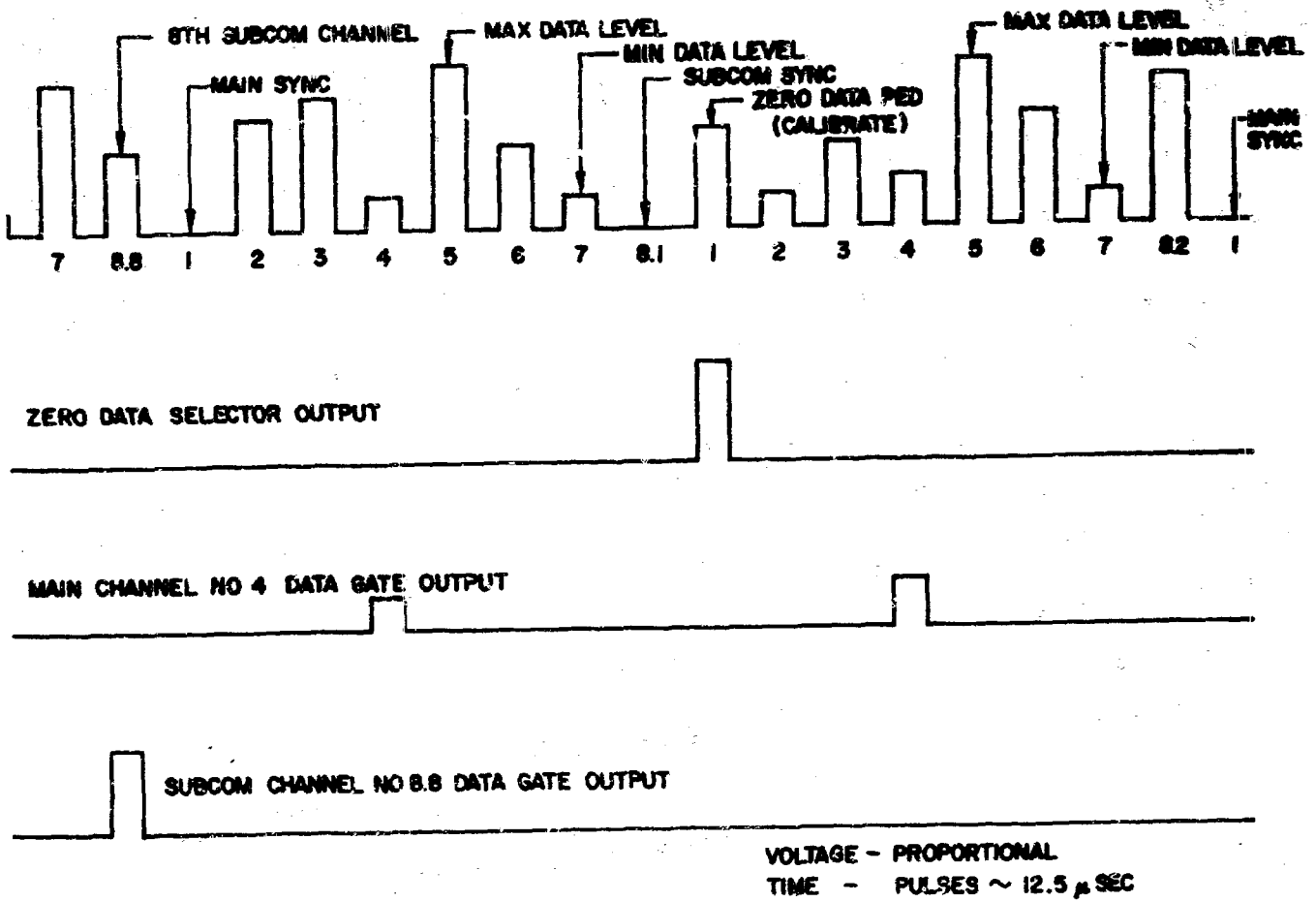


Fig. 7-5 Typical Vibration PAM Pulse Train (Idealized)

and each high-frequency channel will produce eight bits of information at a rate of 500 samples per second. There are 32 information pulses (one frame) every 2000 microseconds. Each main channel is equally spaced in time, and each subcommutated channel is equally spaced in time.

The 0- to 5-volt data is superimposed on a 1.5-volt pedestal. Thus, the peak data amplitude is approximately three-quarters of the peak PAM signal amplitude. Synchronization channels have no pedestal, but appear at the baseline level.

Channels 1 and 9 are reserved for main channel sync intervals. Channel 32 is subcommutated into eight channels. Of these, Channel 32.1 is the subcommutated sync interval and Channels 32.2 through 32.8 are subcommutated data channels.

The composite pulse train is band-limited in the vehicle equipment to 35.2 kc by a single-pole filter and is further band-limited on the ground (in the Noise Filter) by another single-pole filter with a cutoff frequency of 35.2 kc.

A typical G-A composite pulse train (Fig. 7-6) has these characteristics with respect to Demultiplexer input:

- Reference level of 0 volts (sync interval)
- Minimum data level of 1.5 volts (corresponding to 0-volt input to the vehicle multiplexer)
- Maximum data level of 6.5 volts (corresponding to a +5-volt input to the vehicle multiplexer)

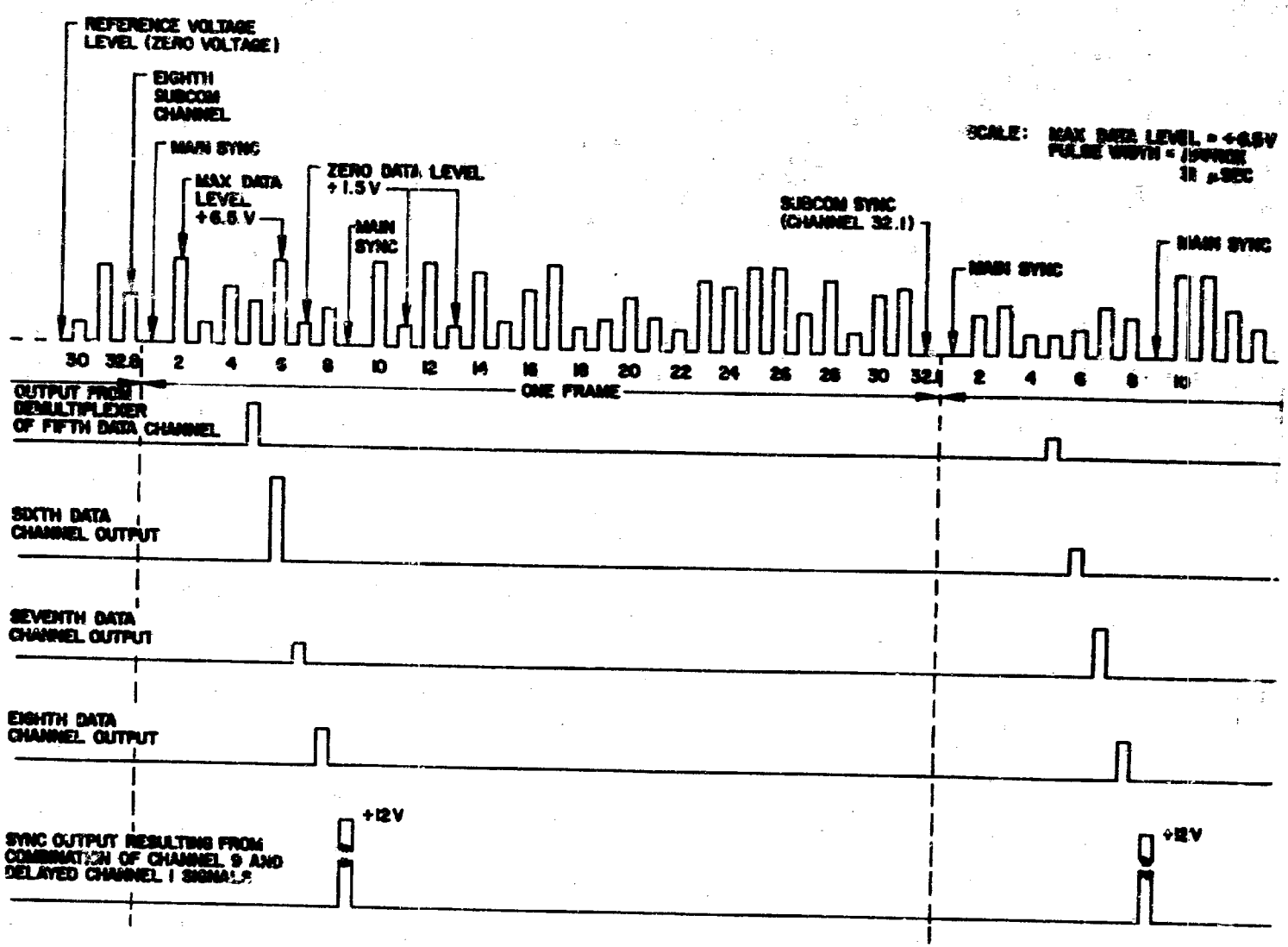


Fig. 7-6 Typical G-A PAM Pulse Train (Idealized)

7.2 VIBRATION

7.2.1 Receiver

Input to the Vibration Ground Station is received at a modified Nems-Clarke 1412 Telemetry Receiver as a PAM-FM signal. After the FM signal has been demodulated, three signals are delivered to other equipment at the station. A dc-coupled PAM signal is delivered to the Base Band Unit at an average level of approximately +6 volts. A field strength signal is delivered directly from the receiver to the FM electronics of the Magnetic Tape Recorder for recording on analog track 14. An ac-coupled signal, to be used as a backup for the digital recording, is delivered through an auxiliary jack to the analog electronics of the Magnetic Tape Recorder for recording on analog track 11. The modifications to the Nems-Clarke 1412 Telemetry Receiver provide a dc-coupled output near ground potential and were made to achieve compatibility with the PAM-FM Ground Station in the following manner:

- To provide dc-coupled and ac-coupled video with the phase opposite to that provided by the unmodified receiver
- To provide video with a level independent of any readily accessible adjustment

This modification was accomplished by bypassing the video amplifier and obtaining an output signal directly from the cathode of the FM discriminator amplifier (V101). A schematic diagram of the modifications is shown in Fig. A-1. Theory of operation and operating and maintenance procedures are described in Instruction Manual for Model 1412 Telemetry Receiver, Nems-Clarke, Inc., Silver Spring, Maryland.

7.2.2 Base Band Unit, Record Mode

The purpose of the Base Band Unit is to

- Amplify the signal from the receiver and provide three separate output signals, each of a different level and isolated from one another

- Insert correct d-c reference level into two of the three output signals
- Limit the bandwidth of the PAM output signals without introducing excessive crosstalk

A block diagram of the Vibration Base Band Unit in the record mode is shown in Fig. 7-7.

The three output signals of the Base Band Unit are (1) a 19-volt peak-to-peak signal for the Analog-to-Digital Converter (Datrac), (2) a 7-volt peak-to-peak signal for the Demultiplexer data gates, and (3) a 15-volt peak-to-peak signal for the Demultiplexer sync circuits.

The 19-volt peak-to-peak signal for the Datrac must be referenced so that the minimum peak is -9.5 volts. The 7-volt peak-to-peak signal for the data gates is referenced so that zero output of the interpolation filters of the display circuitry corresponds to zero data, i.e., the minimum peak is approximately -1.5 volts. The 15-volt peak-to-peak signal for the sync circuits is not referenced and is a-c coupled.

Since the Vibration PAM signal has a 40-kc pulse repetition rate, it must be considered a high-speed system. Accuracy requirements approach two percent. The high repetition rate and accuracy requirements dictate the use of a finite memory type of filter. Finite memory filters can be adjusted so that practically zero crosstalk is introduced into the system. The filter is adjusted so that the output reaches full amplitude of the input pulse during the time of the pulse and decays to zero by the time the peak value of the succeeding pulse is reached. The accuracy of the adjustment determines the amount of crosstalk introduced by the finite memory filter.

Two signals flow through the Base Band Unit. One is the PAM pulse train, the other is the d-c reference feedback correction voltage that is derived from a portion of the pulse train.

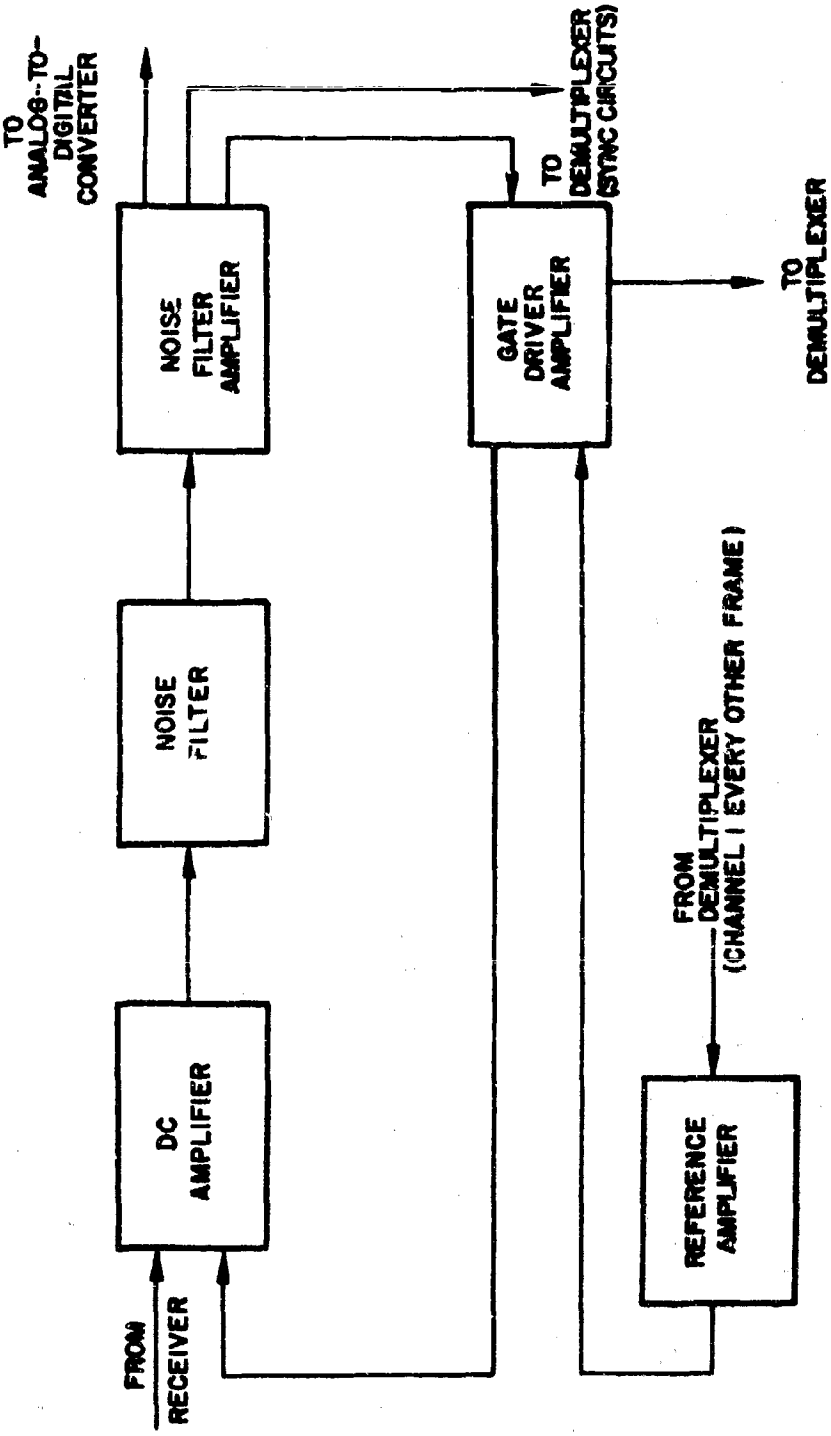


Fig. 7-7 Vibration Base Band Unit, Record Mode

The signal from the receiver, which is approximately 1.4 volts peak-to-peak in amplitude, enters the DC Amplifier where it is amplified approximately 10 times without being inverted. This amplifier is composed of direct-coupled circuits. A suitable means of offsetting positive bias voltage from the receiver is included.

The output of the DC Amplifier, now at a level of approximately 14 volts peak-to-peak, is fed into the Noise Filter described above. Here the signal-to-noise ratio of the PAM pulse train is improved, and approximately 3 volts of negative offset voltage are added to the output signal.

This signal is delivered to the Noise Filter Amplifier at approximately 4 volts peak-to-peak because of attenuation in the Noise Filter. The signal is then amplified so that the Noise Filter Amplifier output to the Datrac is 19 volts peak-to-peak. An adjustment called the Overall Gain is included in this amplifier to set the desired level. An additional adjustment to correct the d-c level to -9 ($\pm$ 0.25) volts is also included in the Noise Filter Amplifier. This signal can be routed through the Reference Voltage Optical Clamp circuit if the Demultiplexer should fail to deliver the correct d-c reference level voltage.

At this point the PAM pulse train is divided into three outputs. One output is the 19-volt peak-to-peak signal to the Datrac, another is the 15-volt peak-to-peak signal to the Demultiplexer sync circuits, and the third is the dc-coupled signal to the Gate Driver Amplifier.

The Gate Driver Amplifier is used to attenuate the 19-volt peak-to-peak signal to a 7-volt signal and supply a low source impedance to drive the data gates. A d-c offset adjustment is incorporated to adjust the minimum peak (sync interval) to approximately -1.5 volts. Incorporated in the Gate Driver Amplifier is a relay activated by the Record-Reproduce switch in the Monitor Panel so that the input to the data gates by way of the Gate Driver Amplifier can be routed from the Datrac or the Noise Filter Amplifier, depending on the mode of operation.

The d-c reference correction voltage originates in the Demultiplexer where the calibrate pulse is sampled by the Zero Data Selector and smoothed through a 1-kc low-pass filter. This signal is then delivered to the Reference Amplifier of the Base Band Unit where the d-c error voltage is amplified approximately 2500 times and delivered to a single-pole, R-C section, low-pass filter with a cutoff frequency of 2 cps. This filter is physically located in the Gate Driver Amplifier. The d-c correction voltage is switched by a relay in the Gate Driver Amplifier to a differential input of the DC Amplifier in the record mode or to a differential input of the Gate Driver Amplifier in the reproduce mode.

7.2.2.1 DC Amplifier

The purpose of the DC Amplifier is to amplify the incoming PAM signal approximately 10 times and establish a d-c reference level of approximately -2 (± 2) volts. These functions are performed by using three dual-triode (6201) vacuum tubes and their associated components. The first two cathode-coupled triodes (V1 and V2) act as a comparison amplifier that amplifies the difference of the signals appearing on grids 2 and 7 of tube V1. The third cathode-coupled dual triode (V3) acts as a parallel cathode follower and furnishes a low output impedance to the Noise Filter. Zener diodes are used to correct the d-c offset throughout the amplifier. A schematic diagram of the DC Amplifier is shown in Fig. A-2.

Two inputs to the DC Amplifier are provided. One input is the PAM pulse train from the receiver; the second is the d-c reference level from the second low-pass filter in the d-c reference feedback loop.

The PAM signal from the receiver is picked up at jack J4 at a level of approximately +6 volts dc. It is passed through Zener coupling diode CR7 where the level is reduced to approximately zero volts dc. This signal is then applied to grid 2 of tube V1A. At the same time, the signal input from the Reference Amplifier, via the second low-pass filter, is applied to grid 7 of tube V1B through a network composed of resistors R9, R10, and R11.

In order to exercise adequate control over the d-c offset voltage, it is necessary to balance the plate current being applied to V1A and V1B, the first stage of the amplifier. This is accomplished by means of potentiometer R2 (DC Balance no. 1). While this adjustment is being made at R2, the input from the Reference Amplifier is disconnected at jack J5. Resistor R2 is adjusted so that the sync interval (absence of a data pulse) is approximately -2 (± 2) volts dc as observed at test point TP3.

The output of V1B is passed through an offset voltage control network composed of diodes CR1, CR2, and CR3 that reduces the d-c voltage by 180 volts (± 10 percent). The signal is then applied to grid 2 of V2A. The cathode of V2A is coupled to the cathode of V2B, which is next to receive the signal. At the same time, there appears on grid 7 of V2B the signal from the output of V3, a part of the amplifier's internal feedback circuit.

The output from the plate of V2B is passed through a second offset voltage control network composed of diodes CR4, CR5, and CR6 which reduces the d-c voltage by 180 volts (± 10 percent). Capacitors C2 and C3 are used to suppress the high-frequency noise generated in the two Zener diode strings CR1, CR2, and CR3; and CR4, CR5, and CR6.

The signal is then applied in parallel to grids 2 and 7 of V3A and V3B, the parallel cathode follower. The output of this parallel cathode follower is delivered through jack J6 to the Noise Filter. At the same time, this output is fed back to the grids of V2B and V1B by means of the feedback resistors R9, R10, R15, and R16. Feedback resistors R9 and R10 are used to control the overall gain of the DC Amplifier to approximately 10.

There are three test points in the DC Amplifier. Test point TP1 provides a sampling point for the input from the receiver after passing through the 6-volt Zener diode CR7. Test point TP2 provides a sampling point for the input from the Reference Amplifier. Test point TP3 provides a sampling point for the output of the amplifier. The input

from the receiver, after passing through the 6-volt Zener diode CR7, is also delivered to the Monitor Panel through jack J1 as the RCVR VIDEO DC position on Switch A and Switch B.

A jumper between jacks J2 and J3 is normally used with the DC Amplifier. Should an occasion arise when operation with the composite pulse train from some source other than the receiver is desired, however, the jumper could be removed and the input applied to jack J2, provided the d-c level is correct.

7.2.2.2 Noise Filter

The purpose of the Noise Filter is to improve the signal-to-noise ratio of the composite pulse train without introducing excessive crosstalk. It is composed of a time delay circuit, a summing junction, a d-c offset adjustment circuit, and an output circuit. Internal switching and separate plug-in output circuits permit use with both Vibration and G-A Ground Stations. Input to the Noise Filter from the DC Amplifier is at jack J7 and its output to the Noise Filter Amplifier is at jack J8. A schematic diagram of the Noise Filter, including circuits used in both Vibration and G-A operation, is shown in Fig. A-3.

With the SYSTEM switch on the Monitor Panel set at the VIB (Vibration) position, and a Vibration plug-in unit in place, all Noise Filter components are in operation. The output circuit is a single, series L-C section resonant at the composite pulse train pulse repetition frequency of 40 kc. The delay of the time-delay circuit is one-half of the repetition frequency period, or 12.5 microseconds. The filter is adjusted so that the output reaches full amplitude during the time of one pulse and decays to zero during the time the next pulse is sampled by the Datrac. The accuracy of this adjustment determines the amount of crosstalk introduced by the Noise Filter, which can approach zero.

The signal is delivered to grid 3 of a dual cathode follower composed of vacuum tube V1 and resistors R9 and R10. The signal is also applied to grid 8 of V1 after a

12.5-microsecond delay produced by delay line L2. Variable resistor R5 of the divider composed of resistors R5 and R6 is used to control the amplitude of the delayed signal to compensate for the attenuation of the undelayed signal introduced by resistors R2 and R3 and by the series-resonant output circuit. The signals present at grids 3 and 8 are then summed by resistors R7 and R8 and applied to the series-resonant circuit composed of L1 and the parallel combination of capacitors C1 and C3. Capacitor C3 is a small variable capacitor that is used to tune the series-resonant circuit to the pulse repetition frequency. The output of the Noise Filter is the voltage developed across capacitors C1 and C3.

D-C offset adjustment is accomplished by a circuit composed of tube V2 and associated components. By varying the operating point of tube V2 with the DC Offset no. 1 control, resistor R13, d-c current flowing out of the junction of resistors R7 and R8 can be changed, and the resulting I-R drop becomes offset voltage. This adjustment is made so that there is 3.5 ($\pm$0.5) volts offset between jacks J7 and J8. Offset conditions should always be checked when changing from one system (Vibration or G-A) to the other.

7.2.2.3 Noise Filter Amplifier

The purpose of the Noise Filter Amplifier is to amplify the signal delivered by the Noise Filter so that the peak-to-peak voltage with full modulation is 19 ($\pm$1) volts. The signal level must be such that the sync level (absence of data pulse) is -9.5 ($\pm$0.25) volts. These functions are performed by using two dual-triode (6201) vacuum tubes and one dual-triode (6463) vacuum tube, and their associated components. The first two cathode-coupled triodes (V1 and V2) act as a comparison amplifier that amplifies the difference of the signals appearing on grids 2 and 7 of V1. The third cathode-coupled triode (V3) acts as a parallel cathode follower and furnishes a low output impedance. Zener diodes are used to correct the d-c offset throughout the amplifier. A schematic diagram of the Noise Filter Amplifier is shown in Fig. A-4.

The signal is delivered to the Noise Filter Amplifier at jack J9 and applied to grid 2 of V1. At the same time, the signal appears at grid 7 of V1 as feedback from cathode follower V3. Plate current to V1 is balanced by means of DC Balance no. 2. In order to make this adjustment, it is necessary to disconnect the input signal at jack J9. Test point TP8 should go to ground potential when the adjustment is properly made.

The output of plate 6 of tube V1 is delivered to grid 2 of V2, the second cathode-coupled dual triode, through an offset voltage control network composed of diodes CR1, CR2, and CR3 which reduces the d-c voltage by 180 volts ($\pm$10 percent). Cathode 2 of V2 is coupled to cathode 8, which is next to receive the signal. At the same time, the signal from the output of V3, a part of the amplifier feedback circuit, appears on grid 7 of V2.

The output from plate 6 of V2 is passed through a second offset voltage control network composed of diodes CR4, CR5, and CR6 which reduces the d-c voltage by 180 volts ($\pm$10 percent). Capacitors C1 and C2 are used to suppress the high-frequency noise generated in the two Zener diode strings.

The signal is then applied to grid 3 of cathode follower V3. The output of this half of V3 appears on cathode 2. This output is delivered to grid 7 of V2 and grid 7 of V1 through resistors R7, R8, R9, and R13, which act as voltage dividers of a feedback circuit within the Noise Filter Amplifier. This output is also coupled to jacks J11 and J12. At the same time, a part of this output is delivered to grid 8 of V3 through resistor R17 and variable resistor R18. The output of this half of V3 appears on cathode 7 and is ac-coupled to the Sync Separator in the Demultiplexer through jack J10. Capacitor C4 acts as a blocking capacitor to prevent high voltage from entering the Demultiplexer.

There are two adjusting points in this circuit in addition to DC Balance no. 2, which was described earlier. Both of these points, resistors R8 and R18, are adjusted with the input from the Noise Filter connected to jack J9. Resistor R8 (Overall Gain) is

set so that the peak-to-peak voltage with full modulation is 19 ($\pm$1) volts at test point TP6. It is advisable to recheck the adjustment of DC Balance no. 2 after resistor R8 is adjusted to assure that ground potential is present without signal input. Variable resistor R18 (a-c gain) is adjusted so that the peak-to-peak voltage with full modulation is 15 ($\pm$2) volts at test point TP7.

The output at jack J11 is connected to the Reference Voltage Optional Clamp where a switch either delivers the signal directly to the Datrac and Gate Driver Amplifier or clamps it to a d-c reference voltage before delivery to the Datrac and Gate Driver Amplifier.

There are three test points in the Noise Filter Amplifier. Test point TP6 furnishes a sampling point for the input from the Noise Filter; test point TP7 furnishes a sampling point to the a-c video output to the Demultiplexer; and test point TP8 furnishes a sampling point to the d-c video output to the Reference Voltage Optional Clamp.

The Noise Filter Amplifier has three outputs. One output is delivered to the d-c coupled Analog-to-Digital Converter. The signal is also fed ac-coupled to the sync circuits in the Demultiplexer. Peak-to-peak amplitude of this output is 15 ($\pm$2) volts. The third output, which is identical to the output going to the Datrac, is delivered to the Gate Driver Amplifier.

7.2.2.4 Reference Voltage Optional Clamp

A Reference Voltage Optional Clamp circuit is included in all Vibration and G-A Ground Stations with record capabilities. The purpose of the clamp is to increase the reliability of the station in the record mode by allowing the operator an optional method of restoring the correct d-c record level in case the main d-c correction circuit fails. A schematic diagram of the clamp is shown in Fig. A-5.

The clamp circuit is contained in a 2-3/4 in. by 2 in. box that is mounted on top of the case containing the Reference Amplifier in the Base Band Unit. The switch positions on the clamp box are labeled CLAMP and SERVO. When the switch is in the SERVO position, the clamp is eliminated from the circuit, and the reference level is furnished by the d-c correction circuit. When the switch is in the CLAMP position, the d-c correction circuit is eliminated and the clamp furnishes the appropriate d-c correction level.

The clamp level is fixed at -9 ($\pm$0.5) volts by an SV-9 Zener diode. In order that the d-c record levels remain approximately the same for the CLAMP or SERVO positions, the main d-c correction circuit must be set up to match the clamp level.

7. 2. 2. 5 Gate Driver Amplifier

The Gate Driver Amplifier furnishes a gain factor of approximately 0. 33 and a d-c voltage offset so that a zero signal at the vehicle multiplexer results in a zero signal at the output of the Demultiplexer. This unit delivers the signal to the Demultiplexer.

This amplifier is made up of a comparison amplifier, a positive peak limiter, a cathode follower, an offset control, and an output clipper. To facilitate switching between the record and reproduce modes of operation, the Reference Amplifier low-pass filter is included as a part of the Gate Driver Amplifier. A schematic diagram of this circuit is shown in Fig. A-6.

In the record mode of operation, the Noise Filter Amplifier furnishes the input to the Gate Driver Amplifier. In the reproduce mode of operation, the Datrac furnishes the input to the Gate Driver Amplifer. The input signal appears at jack J13 or J14, depending on the mode of operation, and is delivered to grid 2 of V1 (a dual-triode vacuum tube, 6201, which acts as a cathode-coupled comparison amplifier) through resistors R1, R2, and R3 which serve as a voltage divider and attenuator. The output of plate 6 of V1 is passed through diode CR1 for offset voltage control, causing the

voltage to drop 180 volts (*10 percent). Capacitor C3 suppresses the high-frequency noise generated by diode CR1. The signal is then passed through the positive peak limiter, composed of variable resistor R13 (limiter bias), diode CR2, and capacitor C4, and is delivered in parallel to grids 3 and 8 of cathode follower V2, a dual-triode (6463) vacuum tube. The output of V2 (cathodes 2 and 7) is passed through a voltage offset adjustment network composed of diodes CR3, CR4, and resistor R18 (DC Offset no. 2). The signal is then delivered to jack J17 through an output clipper composed of diodes CR5 and CR7. This clipper prevents the output to jack J17 from going beyond +10 or -5.6 volts.

Also included in the Gate Driver Amplifier is the second low-pass filter for the d-c reference feedback loop. This filter consists of resistor R4 and capacitors C1 and C2. The input to the filter is from the Reference Amplifier. In the record mode of operation, the filter output is delivered to the differential input of the DC Amplifier. In the reproduce mode of operation the DC Amplifier is not used and the filter output is delivered to the differential input (grid 7 of V1) of the Gate Driver Amplifier through resistors R11 and R14. This unit filters out unwanted frequencies and prevents hunting.

7.2.2.6 Reference Amplifier

The Reference Amplifier has a variable gain from 10 to 2500 to amplify the d-c correction voltage. A gain of 2500 is normally used during operation of the Ground Station in the Vibration mode. The output is delivered first to the second low-pass filter contained in the Gate Driver Amplifier and then to the differential input of the DC Amplifier in the record mode of operation, or to the Gate Driver Amplifier in the reproduce mode of operation.

The circuitry of this amplifier is described in detail in the Handbook of Operating and Maintenance Instructions, A-12 DC Amplifier, supplied with the Ground Station. A schematic diagram of the amplifier is shown in Fig. A-7.

The input to the Reference Amplifier is of a differential type with respect to ground in order to reduce ground loop problems. This input from the 1-kc Filter card in the Demultiplexer appears at jack J25 at approximately 0 volts (within a few millivolts) when the feedback loop is closed. If instability of the video base line is noted, the gain should be reduced until stability is achieved. This instability will be noted at test point TP11 in the Gate Driver Amplifier. Random noise may be present, but it is filtered out by the second low-pass filter in the Gate Driver Amplifier. The output at jack J23 should be 0 (± 5) volts and must never exceed ± 10 volts as this level would represent loss of operation of the d-c reference feedback loop. Although no damage to equipment would result with the output approaching these limits of ± 10 volts, data recovery accuracy of the Ground Station would suffer appreciably.

7.2.3 Demultiplexer, Record Mode

A functional diagram of the Vibration Demultiplexer in the record mode of operation is shown in Fig. 7-8. The three principal functions of the Demultiplexer are: (1) to separate the data sync pulse from the composite data signal for use as a clock pulse for the Demultiplexer and Analog-to-Digital Converter (Datrac) and to generate frame sync pulses from the composite data signal; (2) to open and close the analog gates in sequential fashion in order to separate the composite data signal into separate outputs; and (3) to sample the calibrate pulse that appears on Channel 1 alternately with the sync pulse and send it through a low-pass filter as a d-c correction voltage to the Base Band Unit.

Since the Ground Station is slaved to the vehicle clock, a clock signal must be recovered from the composite pulse train. This is done in the data sync generator where a pulse is generated for every data pulse and sync interval in the PAM pulse train. The phasing can be controlled to give the appropriate time relation between the clock signal thus generated and the analog data pulses from the Base Band Unit.

One output of the data sync generator is used to drive the binary countdown that produces the square-wave signals used for "ANDing" purposes in the matrices. The

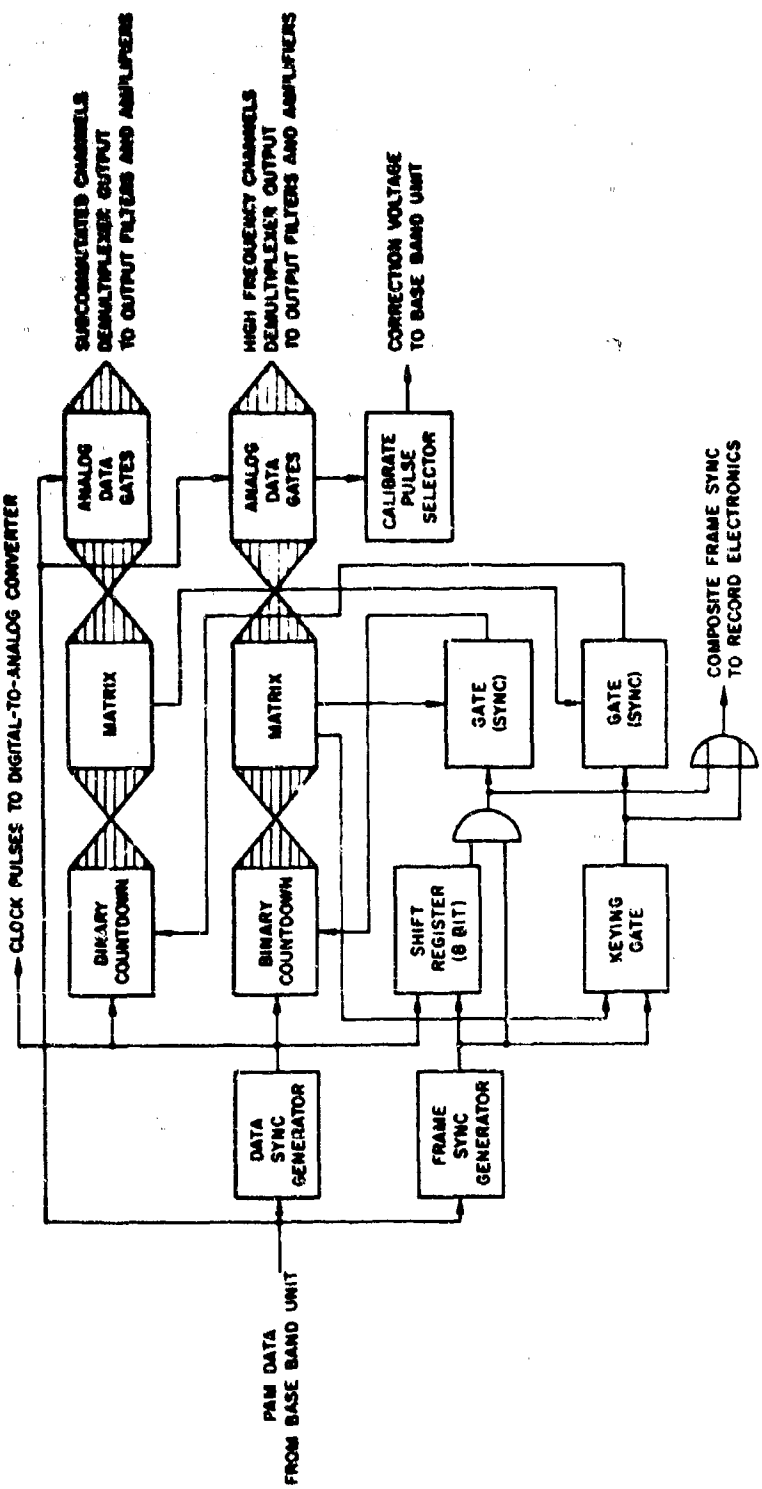


Fig. 7-8 Functional Diagram of Vibration Demultiplexer, Record Mode

outputs of the matrices are the keying signals for the analog data gates which receive their input in the form of the PAM analog pulse train from the Gate Driver Amplifier in the Base Band Unit. These sequential keying signals to the analog data gates are on separate lines and are connected to the appropriate analog data gates which open and close in correspondence with the keying signals. The "on" time of any one high-frequency data gate is the clock period, or 25 microseconds. The "off" time is one frame minus the clock period, or 175 microseconds. The "on" time for a subcommutated data gate is the same as the "on" for a high-frequency data gate, or 25 microseconds. The "off" time of the subcommutated data gate is eight frames minus one clock period, or 1575 microseconds.

To keep the Demultiplexer in synchronization with the PAM pulse train (that is, to open the appropriate analog data gate when each channel of the PAM pulse train is delivered from the Base Band Unit), a frame synchronization pulse is used. Frame synchronization pulses are generated in the frame sync generator which produces a pulse whenever a pulse is missing in the PAM pulse train. To ensure that this pulse is a valid sync pulse and not a stray pulse as might be generated in the presence of r-f noise interference or a faulty multiplexer, a certain amount of logic is incorporated into the circuitry.

True frame sync occurs on Channel 1 alternately with a calibrate pulse. Therefore, the train of potential sync pulses is delayed exactly eight channels by means of an eight-bit shift register and compared in a logic gate with the potential frame sync pulses being generated by the frame sync generator. This will produce a frame sync pulse output only when the potential frame sync pulse appears on alternate frames. Once apparent frame sync has been established, it is fed into a gate which opens to receive a sync pulse only when one is expected as determined by the high-frequency binary countdown and matrix. When the sync pulse arrives, it closes the gate and blocks any spurious pulses. If the sync pulse does not arrive as expected, the sync gate remains open until sync is again established. This circuit performs the function of blocking periodic and nonperiodic false sync pulses as well as the subcommutated

sync pulse, which appears as a nonperiodic sync pulse to the high-frequency binary countdown.

In addition, a subcommutated synchronization pulse is needed to control the subcommutated binary countdown and matrix. This pulse is derived by sampling the output of the frame sync generator only during Channel-8 time by way of a keyed gate that is controlled by the high-frequency binary countdown and matrix. The output of the keyed gate is delivered to a subcommutated sync gate which operates in the same fashion as the high-frequency gate except that it is controlled by the subcommutated countdown and matrix.

The two signals appearing at the output of the high-frequency and subcommutated sync gates are delivered to the Digital Record Electronics for recording on a single digital track. These signals are combined onto one line by means of an OR gate.

7.2.3.1 Data Sync Separator

The purpose of the Data Sync Separator is to extract the data sync or clock information from the composite pulse train (a-c video). The Data Sync Separator is composed of the following circuits: clamp and clipper, band-pass filter, pulse shaper, clipper amplifiers, one-shot, emitter follower, and blocking oscillator. A schematic diagram of the Data Sync Separator is shown in Fig. A-8.

Clock output occurs in the form of a square wave or pulse; data sync is in the form of a pulse only. Clock information is in time phase with data sync information. Data sync output is actually clock information which has been delayed so that keying pulses for the data gates occur at a time when interchannel crosstalk is at a minimum. The Q of the band-pass filter is such that clock and data sync outputs are present when as many as approximately 30 consecutive data pulses are missing. Operation of the Data Sync Separator ceases whenever more than approximately 30 consecutive data pulses are missing.

The composite pulse train input (a-c video) from the Noise Filter Amplifier appears at pin J. It then enters the clamp and clipper circuit, which is composed of diodes CR3 and CR4, transistors Q3 and Q6, and associated components. This circuit restores the d-c level to the a-c video and clips below minimum data level. Resistor R13 is adjusted so that positive peak clipping occurs at 1.5 ($\pm$0.2) volts. Test point TP1 - the junction of diode CR4 and resistor R13 - should be observed when this adjustment is being made.

The output from the clamp and clipper circuit passes through the emitter follower, composed of transistor Q6 and resistor R19, into the band-pass filter. This band-pass filter is a ringing, oscillator-type circuit in which the resonant frequency is that of the sampling rate of the composite pulse train. The output level control of the clamp-and-clipper circuit, resistor R19, is adjusted so that the peak-to-peak amplitude of the output sine wave at the junction of capacitor C14 and diode CR7 is 15 ($\pm$1) volts. Fine tuning of the tank circuit is made by adjusting capacitor C13A.

The signal is coupled into the pulse shaping network through capacitor C14. Transistors Q14 and Q17, diode CR7, and associated components act as a dual emitter follower and clamp circuit. Its output is fed into the clipper circuit composed of diodes CR9 and CR10, transistor Q19, and associated components. Silicon diodes CR9 and CR10 change the sine wave from the dual emitter follower into an approximately square wave.

This square wave is coupled into the clipper amplifiers through the emitter follower composed of transistor Q19 and resistor R52. There are two saturating-type amplifier stages and two emitter follower stages in the clipper amplifier circuitry. The two amplifiers are transistors Q2 and Q7 with their associated components; the two emitter follower stages are transistors Q5 and Q9 with their associated components. The signal is amplified but not inverted, and the output is fed into four succeeding emitter followers in parallel. Output of the clipper amplifiers, which is now a square wave, passes through the emitter follower composed of transistor Q8 and associated components to pin M and through the emitter follower transistor composed of transistor Q10 and associated

components to pin R. These two clipper amplifier outputs are then delivered as clock square waves to the Eight-Bit Shift Register at pin M and to the Frame Sync Separator at pin R. Output of the clipper amplifiers is also fed to the one-shot through the emitter follower composed of transistor Q12 and associated components. Positive-going portions of the square wave trigger the one-shot, which is composed of transistors Q15 and Q18 and their associated components. The variable delay of 4 to 25 microseconds is adjusted by resistor R39 in such a manner that the data gates are keyed when minimum interchannel crosstalk occurs. The one-shot output (monitored at the junction of capacitor C21 and resistor R51) is a series of positive pulses. These pulses fire a blocking oscillator composed of transistors Q13 and Q16, transformer T1, and associated components. The output of the blocking oscillator consists of data sync pulses which are fed to the Pulse Sequencer and Frequency Divider at pin b. Finally, the output from the clipper amplifiers passes through an emitter follower composed of transistor Q1 and its associated components; a differentiating circuit composed of capacitor C4, diode CR2, and resistor R8; and an emitter follower composed of transistor Q4 and associated components to pin T for delivery as a series of positive clock pulses to the Data Sync Delay Record.

7.2.3.2 Frame Sync Separator

The Frame Sync Separator produces a pulse whenever a data pulse is absent in the composite pulse train. This unit is adjusted so that whenever the level of a data pulse falls below a 0.5-volt level with reference to the base line, a pulse is produced. The unit is made up of the following functioning circuits: d-c restorer, positive peak clipper, adder, decision level inverting amplifier, one-shot, and three blocking oscillators. A schematic diagram appears in Fig. A-9.

The composite pulse train (a-c video) input is delivered to pin J. It is then clamped to a few tenths of a volt, positive d-c, by means of the d-c restorer composed of capacitors C2 and C4, diode CR2, diode CR11, and resistor R3.

The signal is then delivered to the positive peak clipper set to clip below minimum data level, which is approximately +2 volts as monitored at test point TP1. This clipper is composed of transistor Q1, diode CR3, and associated components. The clipping level is adjusted by varying resistor R8.

The clock square wave from the Data Sync Separator appears at pin R. It is delivered to the clock blocking oscillator composed of transistors Q6 and Q7, transformer T1, and associated components. The output of this blocking oscillator is delivered to pin S as reset pulses to the Eight-Bit Shift Register. It also is delivered to the one-shot composed of transistors Q8 and Q9 and associated components. This multivibrator introduces a variable time delay from 4 to 25 microseconds. The time delay is set by adjusting resistor R26. The output is delivered as clock pulses to a delayed blocking oscillator composed of transistors Q10 and Q11, transformer T3, and associated components.

The output of this blocking oscillator is delivered to the adder composed of resistor R10. This adder combines the clipped composite pulse train and delayed data sync. Resistor R26 in the one-shot circuit is adjusted so that the negative-going blocking oscillator pulses are centered on the data pulses as they are monitored at test point TP2.

The output of the adder is delivered to the decision level inverting amplifier composed of transistors Q2 and Q3, diode CR5, and associated components. This amplifier selects the blocking oscillator pulses which coincide with the absence of data pulses and provides a positive-going pulse to fire the output blocking oscillator composed of transistors Q4 and Q5, transformer T2, and associated components.

The output blocking oscillator provides sync pulses which are delivered to the Eight-Bit Shift Register and the Sync Selector at pin P. Resistor R10 is adjusted so that the blocking oscillator fires reliably whenever a data pulse is absent but will not fire under any other conditions. A good setting of R10 would be halfway between (1) the

setting that just begins to fire the output blocking oscillator at clock rate, and (2) the setting that just stops firing the output blocking oscillator at data pulse absence rate. This setting can be monitored at pins J and P.

7.2.3.3 Eight-Bit Shift Register

The purpose of the Eight-Bit Shift Register is to store data pulse absence or sync pulse information for eight clock periods (of time) and present to a succeeding AND gate direct sync pulse outputs and $\overline{\text{stored sync pulse}}$ outputs.

This unit is composed of a series string of nine delay-coupled flip-flops, four output emitter followers, and a clock driver. The schematic diagram is shown in Fig. A-10.

The first flip-flop acts as a buffer stage for the succeeding eight units in the shift register. It stores the sync pulses until the clock shifts this information into the first storage flip-flop.

Three inputs are provided: Reset (clock) pulses from the Frame Sync Separator appear at pin S; sync pulses from the Frame Sync Separator appear at pin P; and the clock square wave from the Data Sync Separator appears at pin M.

The reset pulse on pin S passes through diode CR1 and saturates transistor Q1. When a sync pulse is present at pin P, current passes through diode CR2 causing transistor Q3 to saturate and the collector of transistor Q1 to go to high potential. This allows capacitor C5 to charge through R10 because diode CR7 is back-biased when transistor Q2 of the clock driver is cut off with a negative clock pulse. When transistor Q2 is saturated with a positive clock pulse, diodes CR7 and CR8 conduct because of the previous charge on capacitor C5. This current flowing through diode CR8 cuts off transistor Q4 and saturates transistor Q5, thus setting up the first storage flip-flop.

In a like manner, the absence of a sync pulse will cause the first storage stage to be set up in the opposite way with transistor Q5 cut off and transistor Q4 saturated. This process continues through succeeding stages until the last stage is reached.

Two outputs are provided by the output emitter followers. The $\overline{\text{stored sync pulses}}$ are delivered to pin U for transfer to the Programmer, while the direct sync pulses are delivered to pin K for transfer to the Programmer.

7.2.3.4 Programmer

The purpose of the Programmer is to (1) provide a keying pulse to the sync gate every other frame at the Channel 1 position and (2) provide the ANDing logic associated with the Eight-Bit Shift Register. The Programmer is composed of an AND gate and a flip-flop. A schematic diagram is shown in Fig. A-11.

Inputs to the AND gate (pins K and U) are provided by the Eight-Bit Shift Register. Input at pin K corresponds to the absence of a data pulse, and input at pin U corresponds to the presence of a data pulse delayed for eight bits of time. Diodes CR1 and CR2 and the emitter follower composed of transistor Q1 and resistor R1 provide a pulse upon the time-coincidence of inputs at K and U.

The flip-flop, which is composed of transistors Q2 and Q3 and associated components, is triggered by the Channel 1 keying pulse from the data gate. This pulse appears at pin d. The flip-flop output, which is coupled through the emitter follower composed of transistor Q4 and resistor R12, constitutes a keying pulse to the sync gate and is delivered to pin a.

7.2.3.5 Sync Selector

The purpose of the Sync Selector is to combine sync pulses for recording purposes in such a manner that only sync gate and keyed gate circuitry need be used to produce

both main and subcommutated frame sync while in the reproduce mode. A schematic diagram of the Sync Selector is shown in Fig. A-12.

There are two inputs to the Sync Selector. Sync pulses from the Eight-Bit Shift Register AND gate appear on pin Z. Sync pulses from the Frame Sync Separator appear on pin P.

Sync pulses entering at pin P pass through an emitter follower composed of transistor Q1 and resistors R2 and R4. These pulses then enter the gate circuit, composed of transistors Q3, Q4, and Q5 and associated components, at the emitter of transistor Q4. Series switch Q4 and shunt switch Q5 are keyed by a pulse amplifier composed of transistor Q3 and resistors R3 and R7. This pulse amplifier is operated by subcommutated keying pulses, which appear on pin K in such a manner that the presence of a keying pulse opens the gate and the absence of a keying pulse closes the gate. Output pulses from the gate are passed through the emitter follower composed of transistor Q7 and resistor R12 for delivery to pin d as the subcommutated sync pulse to the sync gate. Output pulses from the gate are also passed through the emitter follower composed of transistor Q6 and resistor R11 and are coupled through capacitor C4 for delivery to the blocking oscillator that is composed of transistors Q8 and Q9, transformer T1, and associated components.

Sync pulses also enter at pin Z and pass through an emitter follower composed of transistor Q2 and resistor R6 and are then coupled through capacitor C3 for delivery to the blocking oscillator.

The blocking oscillator is fired by current pulses from either capacitor C3 or capacitor C4. The positive output pulses of the blocking oscillator are delivered to pin f as composite frame sync for the Digital Record Electronics.

7.2.3.6 Sync Gate

The purpose of the Sync Gate is to permit frame sync pulses to be generated only when such pulses are anticipated. Sync pulses which are not true sync pulses are sometimes produced by preceding sync separation circuits because of r-f interference. Therefore, if a pulse can be supplied to arrive at a time when frame sync is expected and this pulse keys a gate that follows the frame sync logic circuitry, the chance of producing false frame sync is greatly reduced. The Sync Gate is made up of two one-shots, two blocking oscillators, a flip-flop, a dual emitter follower, and a gate. The schematic diagram for the Sync Gate is shown in Fig. A-13.

There are two inputs to the Sync Gate. Keying pulses are delivered to pin a. Sync pulses are delivered to pin Z. Frame sync output is on pin f.

The keying pulse from pin a resets the flip-flop composed of transistors Q3 and Q5 and associated components so that the output on the emitter follower composed of transistor Q1 and resistor R2 (TP2) turns on the gate composed of transistor Q13 and resistors R36 and R37.

The anticipated sync pulse appears on pin Z. It is a positive pulse and is differentiated by capacitor C1, diode CR1, and resistor R1 so that the positive-going portion of the pulse triggers the one-shot composed of transistors Q2 and Q4 and associated components. This one-shot fires blocking oscillator no. 1, composed of transistors Q6 and Q7, transformer T1, and associated components, at a time several microseconds after the initial generation of the sync pulse in the Frame Sync Separator. The reason for this delay is that sync pulses generated in the Frame Sync Separator are approximately in time phase with the data sync and that resetting of the pulse sequencers by the output of the Sync Gate (pin f) must occur slightly after triggering by the data sync. This delay can be varied between 4 and 25 microseconds by adjusting resistor R3, but the delay is usually of the order of 3 (± 1) microseconds.

The positive-going output pulses of blocking oscillator no. 1 are delivered to the dual emitter follower composed of transistors Q9 and Q11 and associated components. The output level of the dual emitter follower is seen at test point TP1, and is adjusted by means of variable resistor R36 to 10 ($\pm$2.5) volts peak-to-peak.

The gate composed of transistor Q12 and resistors R36 and R37, which was opened by the action of the flip-flop, passes a positive pulse that fires blocking oscillator no. 2 composed of transistors Q13 and Q14, transformer T2, and associated components.

The output of blocking oscillator no. 2 is delivered to pin f as frame sync and to one-shot no. 2, composed of transistors Q8 and Q10 and associated components. One-shot no. 2 introduces a delay just long enough to insure that the gate will pass anticipated frame sync pulses. Variable resistor R34 should be adjusted so that the flip-flop closes the gate approximately 3 microseconds after the generation of a frame sync pulse on pin f.

Essentially, the Sync Gate is a gate which is keyed "on" by the arrival of a pulse which just precedes the anticipated sync pulse. It is keyed "off" if the anticipated sync pulse passes through the Sync Gate. If no anticipated sync pulse arrives, the Sync Gate remains open until an apparent sync pulse arrives.

7.2.4.7 Zero Data Selector

The Zero Data Selector selects the pedestal levels from the composite pulse train which contains alternating pedestal levels and sync levels on Channel 1. The pedestal levels are fed to the first low-pass filter in the DC reference feedback loop. A schematic diagram of the Zero Data Selector is shown in Fig. A-14.

Channel 1 keying pulses from the Data Gate enter on pin d into an emitter follower composed of transistor Q1 and resistor R4. It is coupled through capacitor C4 to the trigger input of the flip-flop composed of diodes CR1, CR2, and CR3; transistors Q2 and Q3; and associated components.

The main frame sync from the Sync Gate enters on pin f and resets the flip-flop so that the output at the emitter follower composed of transistor Q4 and resistor R21 is positive only when pedestal pulses appear in the pulse train. The output of this emitter follower is "ANDed" with the output of the emitter follower composed of transistor Q1 and resistor R4 by means of an AND gate composed of diode CR4 and resistor R17. The output of this AND gate turns transistor Q7 on only during alternate frames. The output at the collector of transistor Q7 keys the keyed gate composed of transistors Q5 and Q6 and associated components. The keyed gate permits only alternate Channel 1 data (pedestal pulses) to be applied to the d-c reference feedback loop. The output of this keyed gate is delivered to pin V.

7.2.3.8 Frequency Divider

The purpose of the Frequency Divider is to divide the repetition rate, or frequency, of pulses by factors of two, four, or eight. Reset and set inputs are available for each of the three cascaded flip-flops, or binary counters, so that outputs can be phased in any desired manner. A schematic diagram of the Frequency Divider is shown in Fig. A-15.

When it is desired to operate pulse sequencers at rates below that of clock, a frequency divider is inserted between the source of clock pulses and a low-speed pulse sequencer. As the low-speed sequencers must sequence at certain times, reset pulses must be properly applied to the flip-flops in use. In the Vibration operation, the frequency is divided by eight.

All three flip-flop stages and associated output emitter followers in the Frequency Divider are similar. As shown in the schematic diagram, data sync pulses are delivered as trigger pulses for the Frequency Divider at pin b. Set and reset pulses are furnished for each of the three flip-flops. Output in the form of trigger pulses for the subcommutated pulse sequencer are delivered to pin P.

7. 2. 3. 9 Eight Channel Pulse Sequencer

The purpose of the Eight Channel Pulse Sequencer is to provide eight channels of pulses in time sequence. Seven flip-flops and eight AND gates are arranged to accomplish this purpose. A schematic diagram of the Eight Channel Pulse Sequencer is shown in Fig. A-16.

The output pulses of the pulse sequencer are used to key data gates. The trigger pulses determine the rate at which the output pulses advance. The reset pulses determine the phase of the output pulses in relation to the no. 1 output pulse.

The AND gates are driven by flip-flop outputs, which are isolated by individual emitter-follower stages.

7. 2. 3. 10 Data Gates

The purpose of the Data Gates is to provide eight data gates which are keyed by the outputs of a series of AND gates. These AND gates are in turn keyed by pulses from pulse sequencers. The Data Gates unit is made up of 12 emitter followers, eight AND gates, and eight data gates. A schematic diagram of this unit is shown in Fig. A-17.

For any one of the AND gates to produce an output pulse, two coincident input pulses must be present. For example, to produce an output from AND gate 3, input pulses must be present at pins j and V; for an AND gate 2 output, input pulses must be present at pins j and X.

All AND gates are composed of a single diode and a single resistor and possess two inputs and one output. The signal level appearing on Pin J is applied to one input of AND gates 1 through 4 through an emitter follower composed of transistor Q2 and resistor R3. The signal level appearing on pin M is applied to one input of AND gates 5 through 8 through an emitter follower composed of transistor Q7 and resistor R9.

The other input to AND gates 1 through 8 is supplied from appropriate pins and emitter followers. Outputs of AND gates 1 and 8 are coupled through emitter followers to pins d and K, respectively, as keying pulse outputs. These outputs key individual data gates 1 through 8.

All data gates are identical. Each data gate is composed of an inverting pulse amplifier, a shunt transistor switch, and a series transistor switch. Data gate 1 will serve as an example of circuit operation.

AND gate 1 output pulse rises and falls between -15 and -5 volts. When the voltage is greater than approximately -10 volts, transistor Q21 is turned on. The collector of this transistor, which serves as an inverting pulse amplifier, drops to approximately -10 volts. This voltage turns off transistor Q29 and turns on transistor Q13. Transistor Q29 is the shunt switch and Q13 is the series switch. When the output from the AND gate drops below approximately -10 volts, transistor Q13 turns off and turns on Q29.

Whenever an output from an AND gate appears, the data gate will open and d-c video from the Gate Driver Amplifier will appear. Whenever there is no AND gate output, the data gate output will present a short circuit with respect to ground.

The gated outputs from data gates 1 through 8 are delivered to appropriate pins for delivery to display electronics.

7.2.3.11 Data Sync Delay Record

The Data Sync Delay Record circuit delays the clock pulses so that sampling in the Datrac occurs at a time when crosstalk is at a minumum. At this time, the Data Sync Delay Record delivers a command pulse to the Datrac. A schematic diagram of this unit is shown in Fig. A-18.

This circuit is composed of a one-shot which provides variable delay, a blocking oscillator, and an emitter follower.

The input of positive clock pulses from the Data Sync Separator is at pin a . The pulses are delivered through an emitter follower, composed of transistor Q1 and resistor R3, to the one-shot, composed of transistors Q2 and Q3 and associated component, where a suitable delay is added to the clock information. Delays from 4 to 25 microseconds are obtained by adjusting resistor R5. The output of the one-shot is coupled through capacitor C8 to the blocking oscillator composed of transistors Q4 and Q5, transformer T1, and associated components.

Positive command pulses to the Digital-to-Analog Converter leave the blocking oscillator at pin N .

7.2.4 Output Filters and Amplifiers

The purpose of the Output Filters and Amplifiers (Fig. 7-9) is to take the demultiplexed series of pulses and smooth them out in such a fashion that the output can be reproduced continuously and proportional to the signals applied to the vehicle multiplexer.

Three Filter Boards (2 kc, 1 kc, and 250 cps) are provided to interpolate the data pulses from the main and subcommutated data gates. A schematic diagram of a Filter Board is shown in Fig. A-19. The filters have a cutoff frequency of approximately 0.4 times the pulse repetition rate per channel. This results in a 2-kc cutoff frequency for the high-frequency channels and a 250-cps cutoff frequency for the subcommutated channels. The filters pass all frequencies in the range of 0–2000 cps corresponding to the modulation frequencies and attenuate all higher frequencies, including the sampling frequency, at least 40 db. The filters used with the subcommutated channels pass all frequencies in the range of 0–250 cps corresponding to the modulation frequencies and attenuate all higher frequencies, including the sampling frequency, at least 40 db. The filters are connected by way of a patch panel to the output amplifiers which are capable

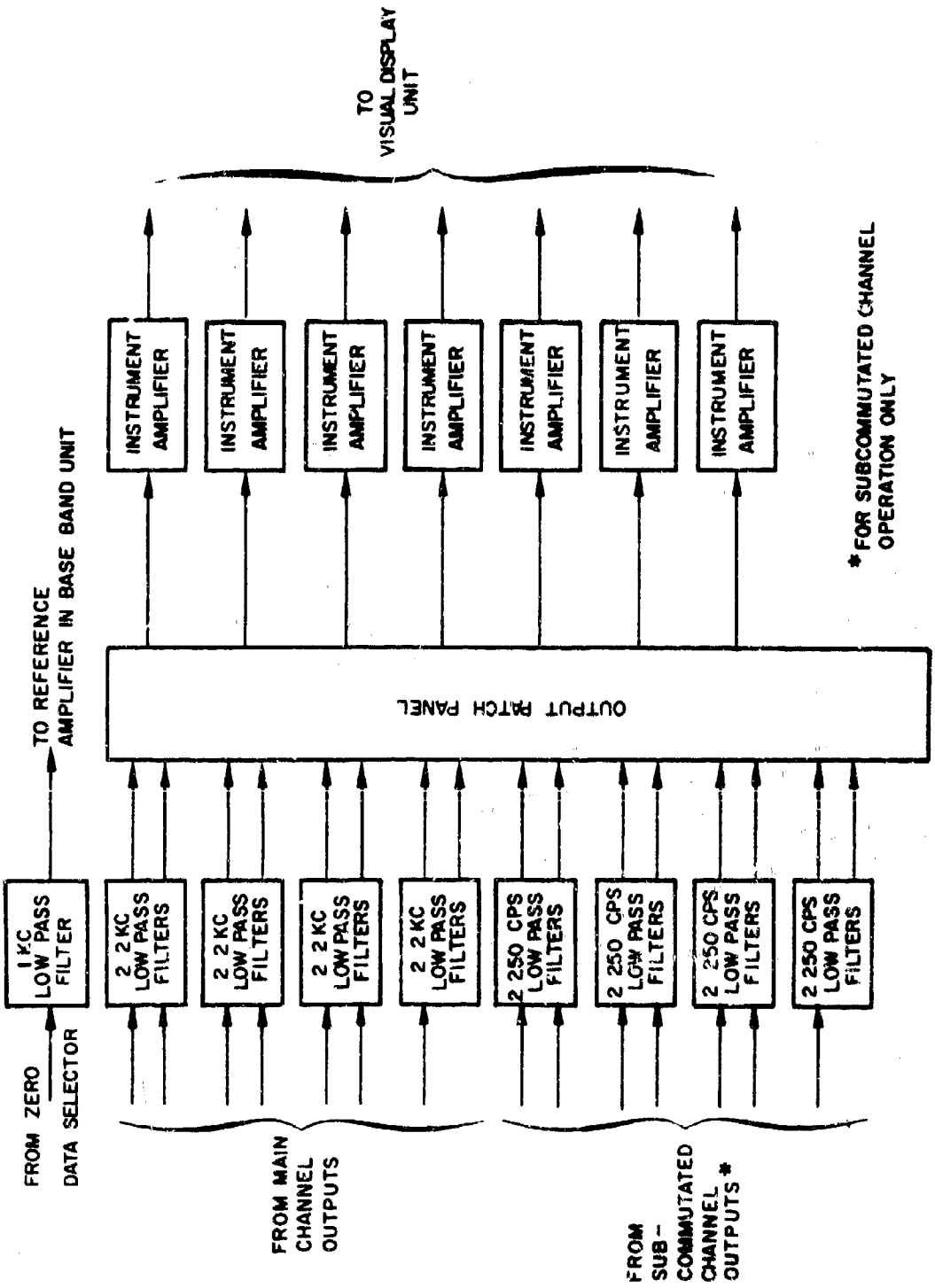


Fig. 7-9 Vibration Output Filters and Amplifiers

of delivering 100 ma to the galvanometers of the Visual Display Unit (Visicorder) or to an external load.

Characteristic impedance of both types of Filters is 10K, and two outputs per filter are provided, one being one-eighth the amplitude of the other, so that display circuit gains do not require adjustment when the duty factors are changed, as in the case of switching from main to subcommutated channels.

In addition to the 250-cps and 2-kc filters that are used only for interpolation, 1-kc filters are used in the d-c reference servo loop. Here, a 1-kc cutoff frequency adequately filters the 2.5-kc fundamental frequency component of the sampled input without causing instability in the servo loop. The Output Filters and Amplifiers perform the same function and operate in the same manner in both the record and reproduce modes of station operation.

7.2.5 Visual Display Unit

The Visual Display Unit (Visicorder) reproduces the outputs of the Output Filters and Amplifiers in oscillograph form and thus furnishes a simultaneous time history of the seven information channels of the Demultiplexer output. Adjustments on the Patch Panel allow the operator to select any or all of the channels of information for display on the Visicorder.

The theory of operation and maintenance procedures for the Visicorder are described in detail in a publication of the Heiland Division of Minneapolis-Honeywell titled Operation Manual – Honeywell Model 906B Visicorder Oscillograph, Publ. No. 850320, Denver, Colorado, Sep 1959.

7.2.6 Analog-to-Digital Converter

The Analog-to-Digital Converter (Datrac) converts every pulse of the PAM composite pulse train into a nine-bit digital word.

Included in the Analog-to-Digital Converter is a sample and hold circuit that samples the peak value of every pulse and holds it for digitization. This circuit, which is controlled by the data sync pulse from the Demultiplexer, is turned on for approximately 2 microseconds by the data sync pulse and holds for approximately 23 microseconds. After a short stabilizing interval, the converter operates at a rate of 2 microseconds per bit and converts the sample and hold signal into a nine-bit digital word in 18 microseconds. These nine bits are temporarily stored and applied to the Digital Record Electronics.

The theory of operation and maintenance procedures for the Datrac are described in detail in the instruction manual Datrac Analog-to-Digital Converter published by Epsco, Inc., Boston, Mass. Modifications made in the Datrac are described in this manual. Schematic diagrams of the modifications are shown in Figs. A-20, A-21, A-22, A-23, and A-24.

In performing the function of recording and reproducing information for the PAM-FM Ground Station, it is necessary to convert analog information into digital form for recording and to convert digital information into analog form for reproduction. The conversion process is accomplished by a device supplied by Epsco, Incorporated, under the trade name of Datrac. The model supplied for use in the Ground Station is the B-609SM2, modified for the special requirements of the Ground Station. The Datrac B-609SM2 (a modified version of Model B-611) is documented in an instruction manual for the Datrac Analog-to-Digital Converter, Models B-611 and B-613. The purpose here is to document those modifications made to the B-611 and the B-609SM2 for use in the PAM-FM Ground Station.

The modifications include:

- Addition of special high-speed sample and hold circuitry
- Addition of relays for converting between digital-to-analog and analog-to-digital modes

- Gain of analog output circuitry so that input and output level (±10) volts) is the same
- Reduction of noise interference during digital-to-analog operation
- Removal of first and second bits of the 11-bit total
- Addition of monitor points to all outputs to Record Amplifiers
- Addition of separate output connectors for the following signals:
  (1) Datrac command
  (2) Conversion complete
  (3) Serial pulse train
  (4) Analog output

A brief description of the two modes of operation of the modified Datrac will be included here.

In the analog-to-digital mode of operation, the first event to occur is the arrival of a Datrac command pulse. This pulse does three things: (1) it starts the sampling process by operating the sample and hold switch-driver circuitry, (2) it starts the digitization process which actually begins with the third of 11 bits approximately 6 microseconds later, and (3) it clears all digital data from the previous conversion. Bits one and two have been removed from the 11-bit converter in order to give nine-bit information and to allow stabilization of the sample and hold circuitry and the amplifier following the sample and hold. The sampling interval begins with the arrival of the Datrac command pulse and lasts approximately 1.5 microseconds. The memory of the sample and hold circuitry then holds data voltage for approximately 23.0 microseconds, at which time digitization is complete and a conversion complete pulse (used to clock data onto the magnetic tape) is produced. Digitization of nine bits, beginning with the third and ending with the eleventh, is performed at the rate of one bit for every 2 microseconds.

In the digital-to-analog mode of operation, conversion is completed in only 6 microseconds. In this process, the first event to occur is the arrival of a clear pulse from

the Delay Command Pulse circuit contained in the Record and Reproduce Electronics. The next event to occur is the application, in parallel, of nine bits of digital data from the Data Storage and Gate circuits. As the last event, approximately 2 microseconds later, analog data appears for delivery to the Demultiplexer.

Figure 7-10 illustrates the analog-to-digital conversion sequence. The externally applied command pulse initiates digitization and sampling and the timing of the digitization of nine individual bits of information. Completion of the conversion is marked by a conversion-complete pulse after a total elapsed time of approximately 24.5 microseconds.

The individual conversions necessary to make the Datrac B-611 compatible with the PAM-FM Ground Station are discussed in the following paragraphs.

In order to record the value of data pulses with a minimum of crosstalk and allow digitization time, this data must be sampled in as short a time as possible. The special high-speed sample and hold circuitry samples in only 1.5 microseconds and holds the data value for as long a time as is necessary to perform digitization, i.e., 24.5 microseconds. The sample and hold equipment is contained on two plug-in chassis. Chassis no. 1 contains an input amplifier composed of an operational amplifier and associated network. Chassis no. 2 contains a blocking oscillator, a switch driver, a switch, a holding capacitor, a bias current source, and an operational amplifier and associated network.

Analog voltage from the Base Band Unit appears on terminal 32 of Chassis no. 1 (Fig. A-20) for delivery to the operational amplifier and network composed of resistors R1, R2, R3, R4, R6, and R7. The operational amplifier is composed of one-half of vacuum tube V3, vacuum tubes V1 and V2, and associated components. The gain of this combination of operational amplifier and network is -1 as the ratio of R_2/R_1 is unity. Its output is delivered to the cathode follower composed of one-half of vacuum tube V3 and associated components. The output of this cathode follower is delivered

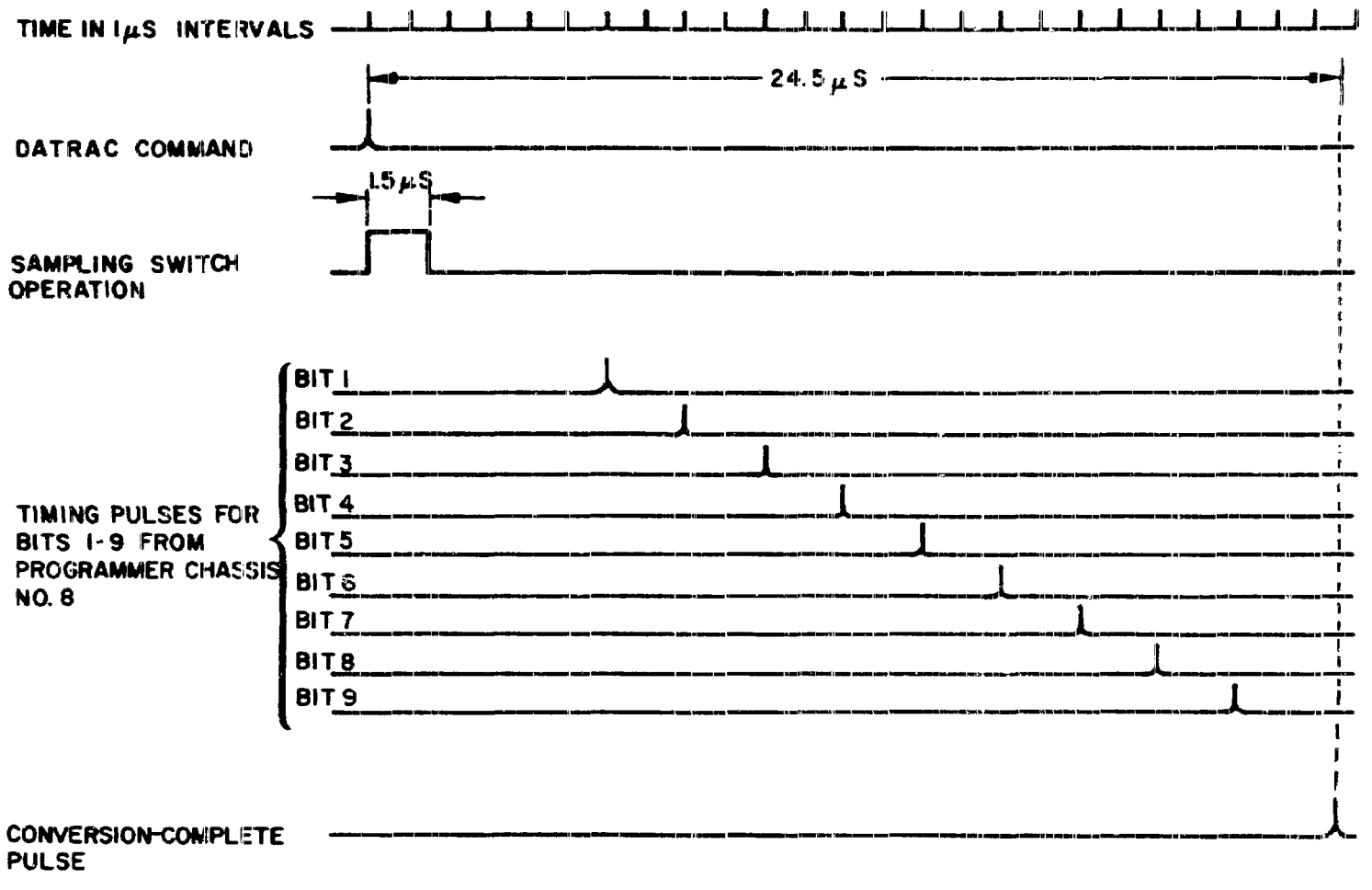


Fig. 7-10 Analog-to-Digital Conversion Process

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to terminal 24 and then to terminal 14 on Chassis no. 2 as input to a diode switch composed of vacuum tubes V4 and V5. The overall gain from terminal 32 to terminal 24 on Chassis no. 1 is approximately 0.85. The output at terminal 24 is between approximately +15 and -5 volts.

Datrac command pulses from Chassis no. 8 appear on terminal 12 of Chassis no. 2 for delivery to a blocking oscillator composed of vacuum tube V6, transformer T1, and associated components. These Datrac command pulses of +20 volts amplitude override the -15-volt bias on grid 2 of V6 and force current to flow from cathode 3 of V6 through capacitor C6 to produce positive voltage on grid 7 of V6. Current, now flowing through transformer T1 to plate 9 of V6, induces voltage across resistor R66, further increasing the positive voltage on grid 7 of V6. The right half of vacuum tube V6 conducts until the charge on capacitor C6 drops enough to return the tube to the cutoff state.

The resulting blocking oscillator pulse is delivered to transformer T2 of the switch-driver circuitry which is composed of transformer T2, and vacuum tubes V7, V8, and V9. Transformer T2 provides positive and negative pulses. The positive pulse is delivered to a cathode follower composed of vacuum tube V8 and resistor R32, and the negative pulse is delivered to a cathode follower composed of vacuum tube V7 and resistor R33. The network composed of resistors R34 and R35 and capacitor C7 provides approximately +37 volts of bias to vacuum tube V7. The network composed of resistors R36 and R37 and capacitor C8 provides approximately -30 volts of bias to vacuum tube V8.

If no pulses are being delivered to the switch-driver circuitry, sufficient current flows through resistor R20, diode vacuum tube V9, and cathode follower V8 to produce approximately -20 volts on the plates of vacuum tubes V4 and V5 of the diode switch. Likewise, sufficient current flows from cathode follower V7 and diode V9 and through resistor R39 to produce approximately +40 volts on the cathodes of V4 and V5 of the diode switch. Under these conditions, diodes V4 and V5 are nonconducting and holding capacitor C9 is effectively tied to the open grid 7 of vacuum tube V10.

When pulses are delivered to the switch-driver from the blocking oscillator, bias voltages for V7 and V8 are overridden so that the currents in both halves of diode V9 are interrupted for the duration of the sampling interval, i.e., for approximately 1.5 microseconds. This means that current flows from +300 volts at terminal 2 through resistor R38, both halves of diodes V4 and V5, and through resistor R39 to -300 volts on terminal 3. With the diode bridge conducting, data from Chassis no. 1 permits supply current to charge holding capacitor C9 to data level.

The voltage level which appears on holding capacitor C9 is delivered to the open grid 7 of vacuum tube V10 of the operational amplifier composed of vacuum tubes V10, V11, and V12, and associated components. Gain of this combination of operational amplifier and the network composed of resistors R61, R62, and R63 is adjusted by varying R63. Overall gain is adjusted to approximately 3 . The sampled output is delivered to terminal 25 of Chassis no. 2 as the input voltage to the Datrac summing junction.

7.2.7 Digital Record Electronics

Digital Record Electronics are used to record the digital word generated by the Datrac, the composite frame sync, and the clock signal in paralled in Non-Return-to-Zero (NRZ) form on the magnetic tape on command of the conversion complete pulse from the Datrac. Digital Record Amplifier, Frame Sync Storage Record, and Pulse Amplifier cards make up the record electronics. A functional diagram of the Digital Record Electronics is shown in Fig. 7-11.

The conversion complete pulse occurs approximately 0.5 microsecond after the digitization is complete. This pulse is amplified and delivered as a clock signal to all digital record amplifiers and is recorded on one of the digital tracks as the clock signal. It is also used to reset the Frame Sync Storage Record circuit.

Composite frame sync is applied to the frame sync storage circuit which, in turn, applies a "one" to the Digital Record Amplifier. The occurrence of a conversion complete pulse will clock this information onto the tape from the Digital Record Amplifier

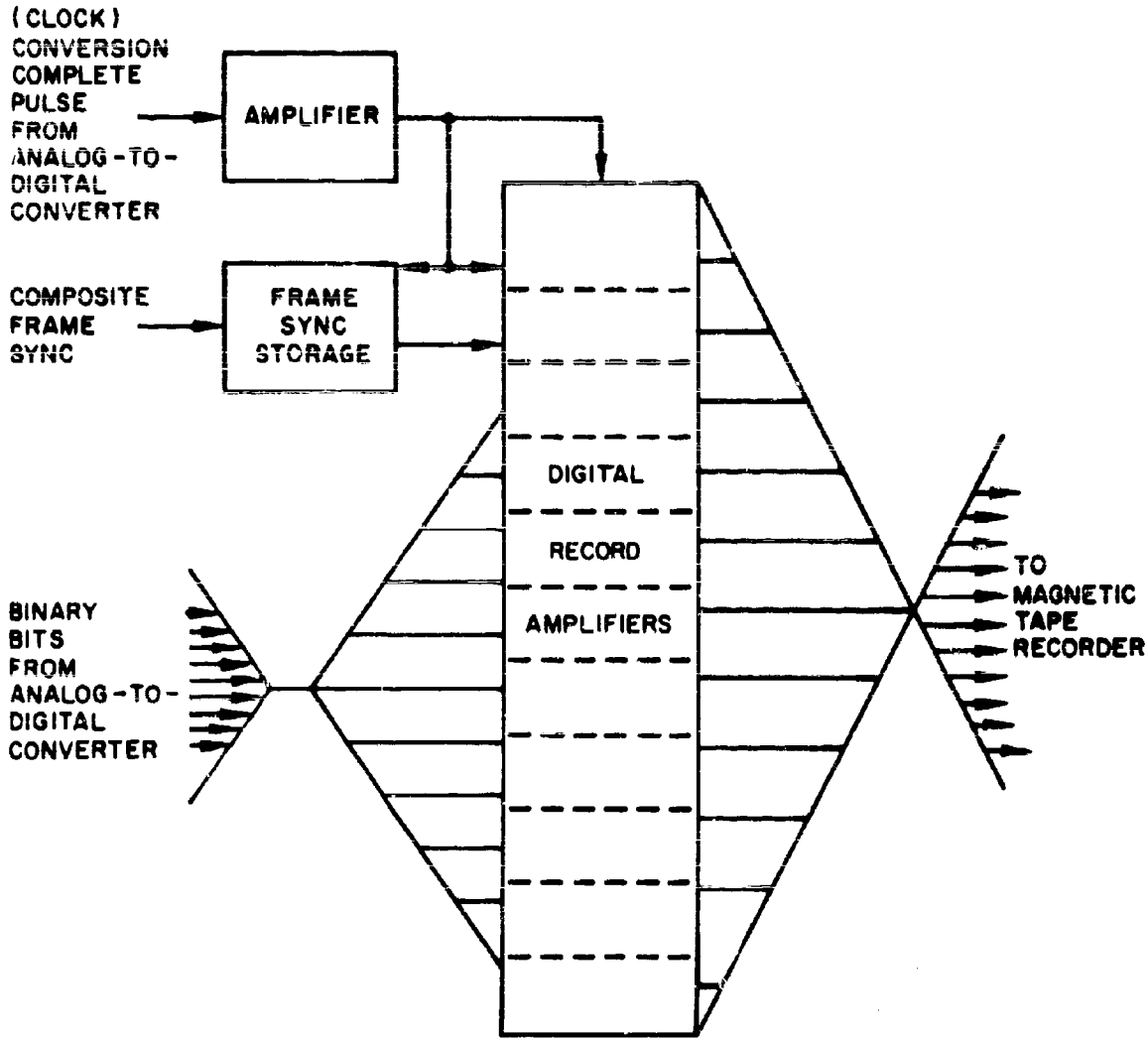


Fig. 7-11 Functional Diagram of Digital Record Electronics

and also reset the frame sync storage circuit to the "zero" state; thus, succeeding conversion complete pulses do not change the magnetization of the tape until a new composite frame sync pulse resets the frame sync storage to the "one" state.

The binary bits from the Datrac are delivered to the appropriate Digital Record Amplifier. The conversion complete pulse interrogates these inputs and causes a change in state of the magnetization of the tape if a "one" is presented to a Digital Record Amplifier and no change in state if a "zero" is presented. Thus, the binary word from the Datrac, the composite frame sync, and the clock signal are all recorded on digital tracks in parallel by the occurrence of a conversion complete pulse.

7.2.7.1 Frame Sync Storage Record

The purpose of the Frame Sync Storage Record is to convert composite frame sync pulses from the Demultiplexer to pulses that will be accepted by the Frame Sync Digital Record Amplifier. It should be remembered that information is recorded when the input to a digital record amplifier is more negative than the negative threshold level and a record pulse is received. Both of these conditions must be met for recording to be accomplished. The Frame Sync Storage Record is made up of an inverting pulse amplifier and a flip-flop. A schematic diagram of the Frame Sync Storage Record card is shown in Fig. A-25.

Positive composite frame sync pulses from the Demultiplexer appear at pin Z for delivery to the inverting pulse amplifier composed of transistor Q1 and associated components.

The negative-going leading edge of the output of the inverting pulse amplifier, which is in time phase with the positive-going leading edge of the pulses at pin Z, is coupled through capacitor C2 to turn off transistor Q3 of the flip-flop composed of transistors Q3 and Q4 and associated components. This action causes the collector of transistor Q4 to go negative, as well as the output of emitter follower composed of transistor Q5 and associated components which is delivered to pin K as output to the Frame Sync Digital Record Amplifier.

Positive record pulses from the Pulse Amplifier appear at pin T for delivery to the emitter follower composed of transistor Q2 and resistors R4 and R5. The emitter follower output is differentiated by a network composed of capacitor C4, diode CR4, and resistor R17 so that the negative-going trailing edge of a pulse on pin T turns off transistor Q4 of the flip-flop. The collector of transistor Q4 now goes positive as does the output on pin K. The delay of approximately one microsecond between the positive-going leading edge of the record pulses, which clock out data from the Digital Record Amplifiers, and the negative-going trailing edge of the record pulse, which resets the flip-flop, is necessary because data must be recorded before composite frame sync information is removed from the Frame Sync Digital Record Amplifier input.

7.2.7.2 Pulse Amplifier

The purpose of the Pulse Amplifier is to convert conversion complete pulses from the Datrac to a form suitable for clocking out the data from the Digital Record Amplifiers. It is made up of an inverting pulse amplifier and a blocking oscillator. A schematic diagram of the Pulse Amplifier is shown in Fig. A-26.

A conversion-complete pulse from the Datrac appears at pin M, where it enters the inverting pulse amplifier composed of transistor Q1 and associated components. The negative-going leading edge of the inverting pulse amplifier output, which is in time phase with the positive-going leading edge of the input pulse on pin M, is coupled through capacitor C2 to fire the blocking oscillator composed of transistors Q2 and Q3 and transformer T1. Positive-going output pulses are delivered to pin T as a record pulse to the Digital Record Amplifiers.

7.2.7.3 Digital Record Amplifier

The purpose of the Digital Record Amplifier is to accept digital "ones" from the Datrac and clock this information onto the magnetic tape in NRZ form in phase with the record

pulses from the Pulse Amplifier. There is one Digital Record Amplifier for each digital recording track. This circuit also provides sufficient power to operate the recording heads. It is made up of an inverting pulse amplifier, a flip-flop, two AND gates, and amplifiers and complementary emitter followers. A schematic diagram of a Digital Record Amplifier card is shown in Fig. A-27.

Digital information appears at pin K in the form of rising and falling levels and is delivered to the inverting pulse amplifier composed of transistors Q1, Q2, and Q3, diode CR1, and associated components. The operation of this inverting pulse amplifier is such that, for levels greater than approximately -11 volts, its output is approximately 0 volts. For levels less than approximately -11 volts, its output is approximately +20 volts.

The output of the inverting pulse amplifier, which is the emitter of transistor Q3, is delivered to two emitter followers, one composed of transistor Q4 and resistor R13, and the other composed of transistor Q9 and resistor R24. The outputs of each emitter follower are each ANDed with record pulses from the Pulse Amplifier, which appear at pin T. These AND gates are composed of diodes CR3, CR4, and CR7, and diodes CR5, CR9, and CR6.

The action of these AND gates causes the flip-flop composed of transistors Q6 and Q7 and associated components to change state whenever a binary "one" and a record pulse are present at the same time. A binary "one" is an input level on pin K of less than -11 volts.

A complementary emitter follower is coupled to each side of the flip-flop through a pulse amplifier. The collector of flip-flop transistor Q6 is associated with the pulse amplifier composed of transistors Q5 and Q14 and associated components and a complementary emitter follower composed of transistors Q11 and Q13. The collector of flip-flop transistor Q7 is associated with the pulse amplifier composed of transistors Q8 and Q15 and associated components and with the complementary emitter follower composed of transistors Q10 and Q12.

The output levels of the complementary emitter followers are out of phase and vary between approximately 0 and +10 volts. Resistor R31 serves to limit magnetic tape recorder head current to approximately 100 ma at all times. The output to the Magnetic Tape Recorder head is between pins a and c . An output monitor point of the head current is available at pin h .

7. 2. 8 Magnetic Tape Recorder

The Magnetic Tape Recorder is a special Ampex unit (FR-1100) that will accept 10-inch or smaller reels of magnetic tape. It is designed to permit the recording of 11 tracks of digital data and four tracks of analog data on one-inch wide tape. Nine of the digital tracks are used to record the digital words from the Datrac. The remaining two digital tracks are used to record the data sync pulse and the composite frame sync pulse. The four analog tracks are used to record video, field strength, voice comment, and system time signals. Normal operating speed of the recorder is 100 ips for Vibration data.

Distribution of tracks and the recording function for each track is as follows:

TRACK	RECORDING FUNCTION
Digital	
1	Bit 9
2	Bit 1
3	Bit 2
4	Bit 3
5	Bit 4
6	Data Sync
7	Bit 5
8	Bit 6
9	Bit 7
10	Bit 8
11	Composite Frame Sync
Analog	
11	Video Backup
12	System Time
13	Spare (Range time at AMR)
14	Signal Strength and Voice

The theory of operation of the Magnetic Tape Recorder and the Procedures for its maintenance are described in detail in the instruction handbook Series FR-1100 Recorder/Reproducer - Magnetic Tape Recorders for Instrumentation, Ampex Corporation, Redwood City, Calif., 1 Jul 1958. Special instructions for using this recorder with the PAM-FM Ground Station are included in appropriate paragraphs in this manual.

7.2.9 Digital Reproduce Electronics

The Vibration Ground Station in the reproduce mode of operation is illustrated in Fig. 7-2.

The Digital Reproduce Electronics (Fig. 7-12) amplifies the digital signals from the magnetic tape and temporarily stores and clocks the digital information into the Datrac. Clock pulses are delivered to the Datrac in the form of a clear pulse and are used to reset the Datrac to a state corresponding to all zero inputs. Clock pulses and the composite frame sync pulse are also delivered to the Demultiplexer.

Binary "ones" from the magnetic tape are amplified in the Digital Reproduce Amplifiers. These binary "ones," which represent the digital word and the composite frame sync, are used to set the storage circuits to the "one" state. Since no change of state is recorded on the magnetic tape for a binary "zero," no signal is produced for a "zero." The binary "ones," which represent the clock signal from the Digital Reproduce Amplifier, are delivered through a delay circuit to the storage circuits where they clock out the stored information in the storage circuits and reset the storage circuits to the "zero" state. Thus, binary "ones" representing digital information are clocked in parallel into the Datrac for conversion to analog form. The effects of any static head skew and dynamic "jitter" of the tape are reduced during this process. Binary "ones" representing composite frame sync are clocked into the Demultiplexer.

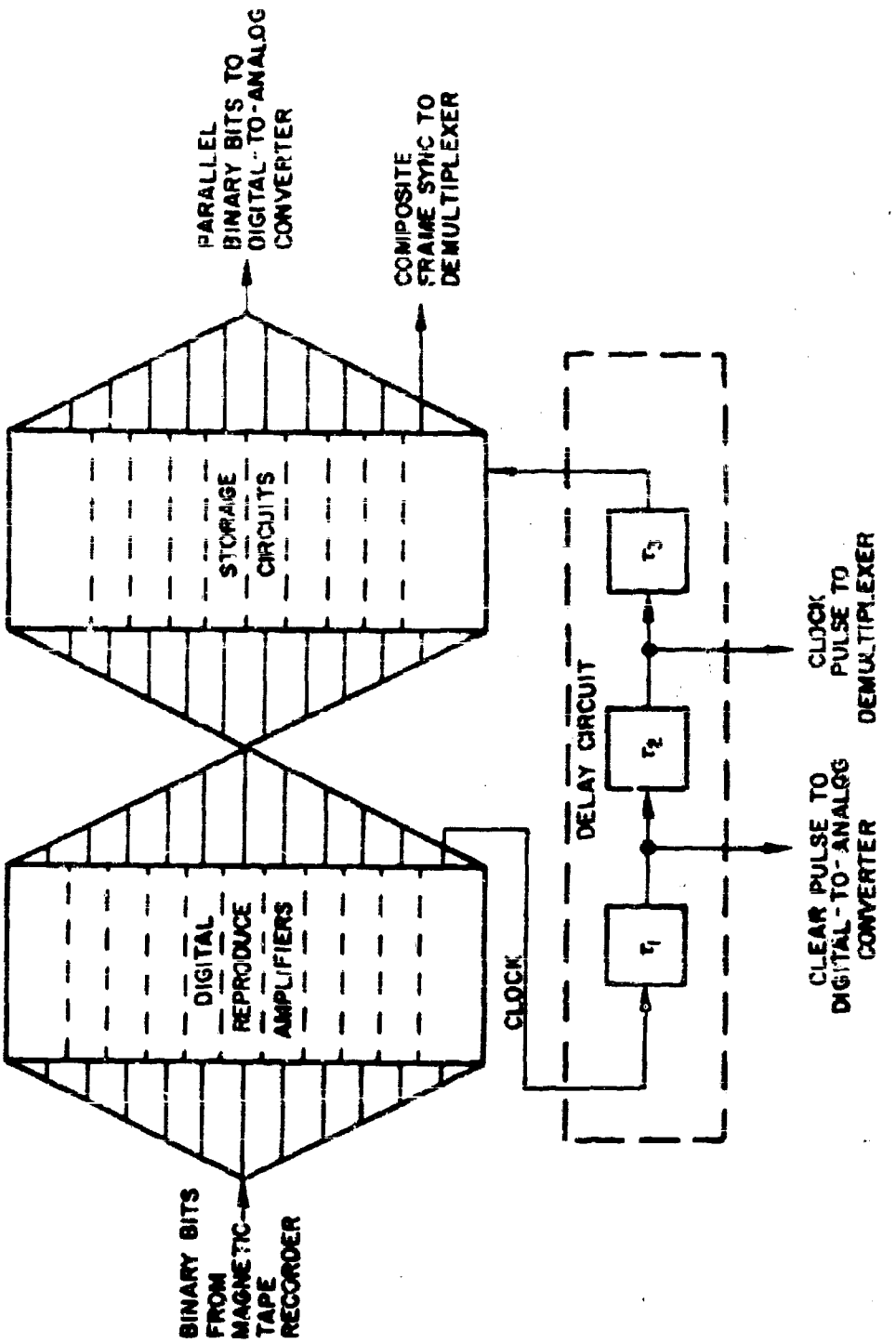


Fig. 7-12 Functional Diagram of Digital Reproduce Electronics

The delay circuit has three outputs, each output occurring 1.5 microseconds after the other. However, the initial output is delayed a suitable time to enable it to be used as a clock signal, but not so long that it becomes a part of the succeeding binary word. The first output is the clear pulse that is used to clear the Datrac. The second output, occurring 1.5 microseconds later, is used as a clock pulse to the Demultiplexer. The last output is used as the command pulse to the storage circuits.

7.2.9.1 Digital Reproduce Amplifier

The purpose of the Digital Reproduce Amplifier is to amplify the data from the digital reproduce heads of the Magnetic Tape Recorder and to produce appropriate data pulses for the Data Storage and Gate circuitry which follows. A schematic diagram of the Digital Reproduce Amplifier is shown in Fig. A-28.

The Digital Reproduce Amplifier contains a high-gain, four-stage, R-C coupled linear amplifier; a linear phase splitter; a full-wave rectifier; and an inverting pulse amplifier. Linear circuitry is used until the data can be brought up to a voltage level that is acceptable for pulse-type amplification. This is done so that the possibility of false generation of output pulses by noise is reduced to a minimum. A variable gain feature is included so that operation with various tape speeds is possible.

Data from the Magnetic Tape Recorder reproduce heads appears at pin L for delivery to the amplifier composed of transistors Q1 through Q5 and their associated components. This amplifier contains four common-emitter stages in cascade and an emitter follower output stage. A constant output level is maintained for various tape speeds by varying the gain. Gain is varied by the application of appropriate values of resistance across pins V and T. The resistances for this function are selected by means of the TAPE SPEED COMPENSATION switch located on the Record and Reproduce Monitor Panel. Gain can also be varied by adjusting variable resistor R19. Amplifier gain should be such that for any tape speed, output is 9 ($\pm$0.5) volts peak-to-peak.

The output of this amplifier is delivered to the phase splitter composed of transistor Q10 and resistors R10 and R43. Here, by adjusting variable resistor R43, two outputs of equal magnitude and 180 degrees out of phase with respect to each other are delivered to separate diodes CR2 and CR3 of the full-wave rectifier. This rectifier changes the positive and negative pulses of the phase splitter to a series of positive pulses. These positive pulses are held between the levels of approximately 0 and +3 volts.

One of the phase-splitter signals is transmitted through the emitter follower composed of transistor Q9 and resistor R38 for delivery to one side of the full-wave rectifier. The other phase-splitter signal, which appears on the emitter of transistor Q10, is transmitted directly to the full-wave rectifier.

The full-wave rectifier output pulses are delivered to the inverting pulse amplifier at the base of the emitter follower composed of transistor Q7 and resistor R32. Whenever the emitter-follower output goes positive, transistor Q8 is turned on and its collector goes to ground potential. Whenever the emitter-follower output reaches zero, or is negative, transistor Q8 is turned off and its collector goes to approximately +13 volts. The signal which appears at the collector of transistor Q8 is coupled through the emitter follower composed of transistor Q6 and resistor R30 for delivery to pin a as output to Data Storage and Gate.

Operation of the Digital Reproduce Amplifier is such that a negative-going output pulse is generated whenever a data pulse appears across the input terminals.

7. 2. 9. 2 Data Storage and Gate

The purpose of the Data Storage and Gate is to hold the digital information received from the Digital Reproduce Amplifier until all bits of information have been read out of the Magnetic Tape Recorder. This delay is necessary to compensate for skew and flutter in the Magnetic Tape Recorder. A command pulse clocks these bits into the

Datrac for conversion to analog voltage. Each Data Storage and Gate card can accommodate two bits of information. A schematic diagram of this unit is shown Fig. A-29.

Two separate but identical circuits are present on each card; each circuit stores one bit of information until the command pulse transmits it to the following circuit. Each circuit is made up of a blocking oscillator, a flip-flop, and an inverting pulse amplifier. Since all circuits are identical, only the operation of one circuit will be described.

Digital data from the Digital Reproduce Amplifier appears at pin K for delivery to the inverting pulse amplifier composed of transistor Q1, diode CR1, and associated components. If the level at pin K falls below approximately +9 volts, transistor Q1 is turned on, the collector of Q1 goes to approximately +9 volts, and a positive-going pulse appears at the junction of capacitor C3 and resistor R8. This positive pulse is then coupled through capacitor C4 so that it turns off transistor Q2 of the flip-flop composed of transistors Q2 and Q3 and associated components.

When a command pulse from Delay Command Pulse appears on pin T , transistor Q3 of the flip-flop will be turned off. This change of state of the flip-flop causes the collector of Q2 to go positive. The signal on the collector of transistor Q2 is coupled through the emitter follower composed of transistor Q4 and resistor R1[illegible] for delivery to the blocking oscillator composed of transistors Q5 and Q6, transformer T1, and associated components.

If the level on pin K rises above approximately +9 volts, no pulse will be delivered to the flip-flop and, consequently, no pulse will be available to fire the blocking oscillator upon the arrival of a command pulse.

7.2.9.3 Data Sync Delay Reproduce

The purpose of the Data Sync Delay Reproduce is to delay the pulses from the data sync Digital Reproduce Amplifier sufficiently so that all information delivered from the Digital Reproduce Amplifiers to the Data Storage and Gate gates has had time to arrive before being clocked out of the Data Storage and Gate gates into the Datrac. It is made up of an inverting pulse amplifier and a one-shot. A schematic diagram of the Data Sync Delay Reproduce card is shown in Fig. A-30.

Negative-going pulses from the data sync Digital Reproduce Amplifier appear at pin a . These pulses are delivered to the inverting pulse amplifier composed of transistors Q1 and Q2 and associated components.

Positive-going pulses are coupled through capacitor C1 to the one-shot composed of transistors Q3 and Q4. This one-shot is triggered by the negative-going leading edge of the pulses at pin a . The one-shot output is fed through the emitter follower composed of transistor Q5 and resistor R15 and delivered to pin N as output to the Delay Command Pulse.

A variable delay of from 4 to 25 microseconds is obtained by adjusting variable resistor R8. Its setting is adjusted so that the outputs from the following circuit, the Delay Command Pulse, properly clock out the data contained in the Data Storage and Gate circuits.

7.2.9.4 Delay Command Pulse

The purpose of the Delay Command Pulse is to provide clear pulses to the Datrac, data sync to the Demultiplexer, and command pulses for the Data Storage and Gate cards during the reproduce mode of operation. Delays of approximately 2 microseconds separate each of these pulses so that no interference can exist while generating video, frame sync, and data sync. This circuit is made up of three blocking

oscillators, two of them with delay capabilities. A schematic diagram of the Delay Command Pulse circuit is shown in Fig. A-31.

Pulses from the Data Sync Delay Reproduce enter at pin N and trigger the first blocking oscillator composed of transistors Q1 and Q2, transformer T1, and associated components. The positive-going portion of these pulses triggers this blocking oscillator. Output (which is essentially undelayed) leaves this blocking oscillator on pin f for delivery to Datrac as the clear pulse. This output pulse, which is approximately 2 microseconds wide, also passes into the delay and blocking oscillator. The negative-going portions of these pulses are extracted by capacitor C6, resistor R10, and diode CR3 and fire the blocking oscillator composed of transistors Q4 and Q5, transformer T2, and associated components. Output from this oscillator is then delivered to pin Z as data sync for delivery to the Demultiplexer. Output from this blocking oscillator is also fed into a second delay and blocking oscillator circuit. Again, the negative-going portions of the 2 -microsecond pulses are extracted by capacitor C9, resistor R18, and diode CR5 and fire the blocking oscillator composed of transistors Q7 and Q8, transformer T3, and associated components. Output of this third blocking oscillator is delivered to pin T as a command pulse to the storage cards.

Monitor points for the no. 1 and no. 3 outputs are at pins f and T respectively.

7. 2. 10 Digital-to-Analog Converter

The Digital-to-Analog Converter is the same converter (Datrac) that is used for analog-to-digital conversion, but operated in the digital-to-analog mode.

The Digital-to-Analog Converter accepts the nine-bit digital words from the Digital Reproduce Electronics and reconstructs the analog PAM composite pulse train. This composite pulse train is then delivered to the Gate Driver Amplifier of the Base Band Unit, which in turn delivers it to the Demultiplexer.

7. 2. 11 Base Band Unit, Reproduce Mode

In the reproduce mode of operation, only the Gate Driver Amplifier and the Reference Amplifier portions of the Base Band Unit (Fig. 7-13) are used.

Input to the Reference Amplifier is from the Zero Data Selector in the Demultiplexer. The Reference Amplifier output in the form of a d-c reference correction voltage is delivered by way of jack J16 to grid 7 of vacuum tube V1 in the Gate Driver Amplifier. The Reference Amplifier functions in the same manner in the reproduce mode as it does in the record mode.

The output of the Digital-to-Analog Converter in the form of an analog PAM composite pulse train provides the second input at jack J14 to the Gate Driver Amplifier. The output of the Gate Driver Amplifier is delivered to jack J17 as d-c video to the Demultiplexer. Except for the changes in input, the Gate Driver Amplifier functions in the same fashion in the reproduce mode as it does in the record mode.

7. 2. 12 Demultiplexer, Reproduce Mode

Although the Demultiplexer in the reproduce mode (Fig. 7-14) functions in much the same way as it does in the record mode, inputs are from different sources and a part of the synchronization logic is not used. Since clock pulses and composite frame sync pulses have been recorded, there is no need for a data sync generator, frame sync generator, or a shift register. Two additional circuits are used in the reproduce mode, however. These circuits are discussed in Paragraphs 7. 2. 12. 1 and 7. 2. 12. 2.

7. 2. 12. 1 Duty Cycle I

Duty Cycle I is a chopper which converts the analog pulse train from the Datrac into a serrated waveform (with a duty cycle of approximately 50 percent) for delivery to the analog data gates.

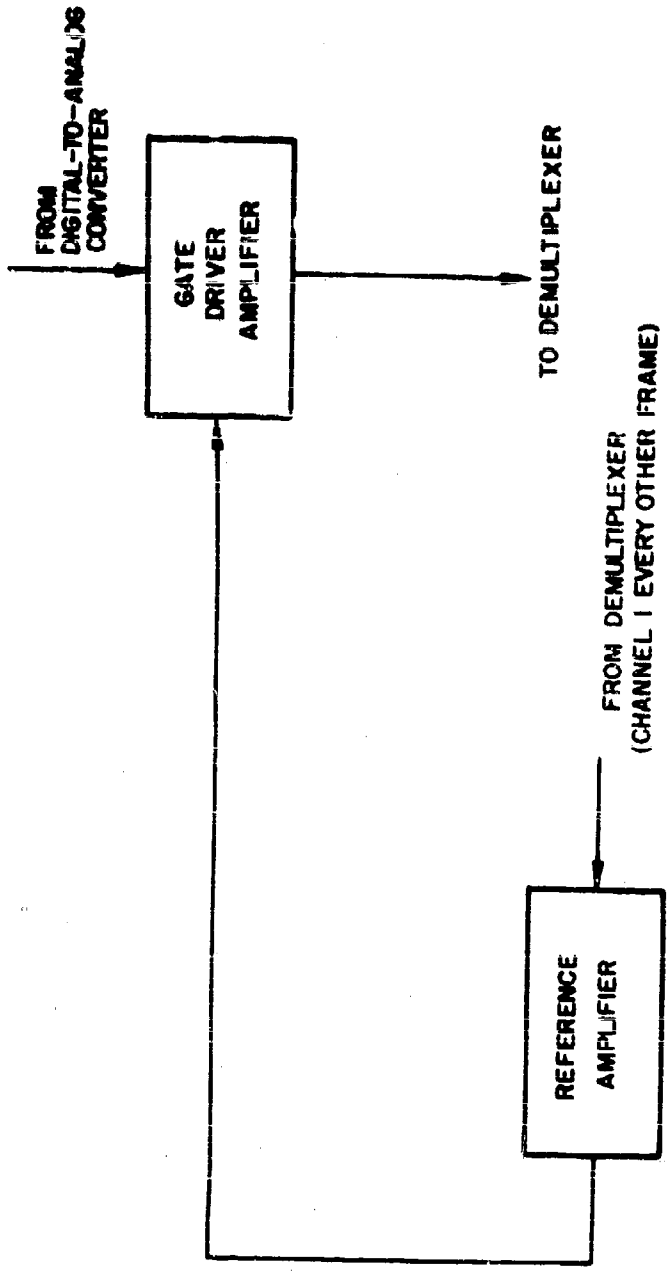


Fig. 7-13 Vibration Base Band Unit, Reproduce Mode

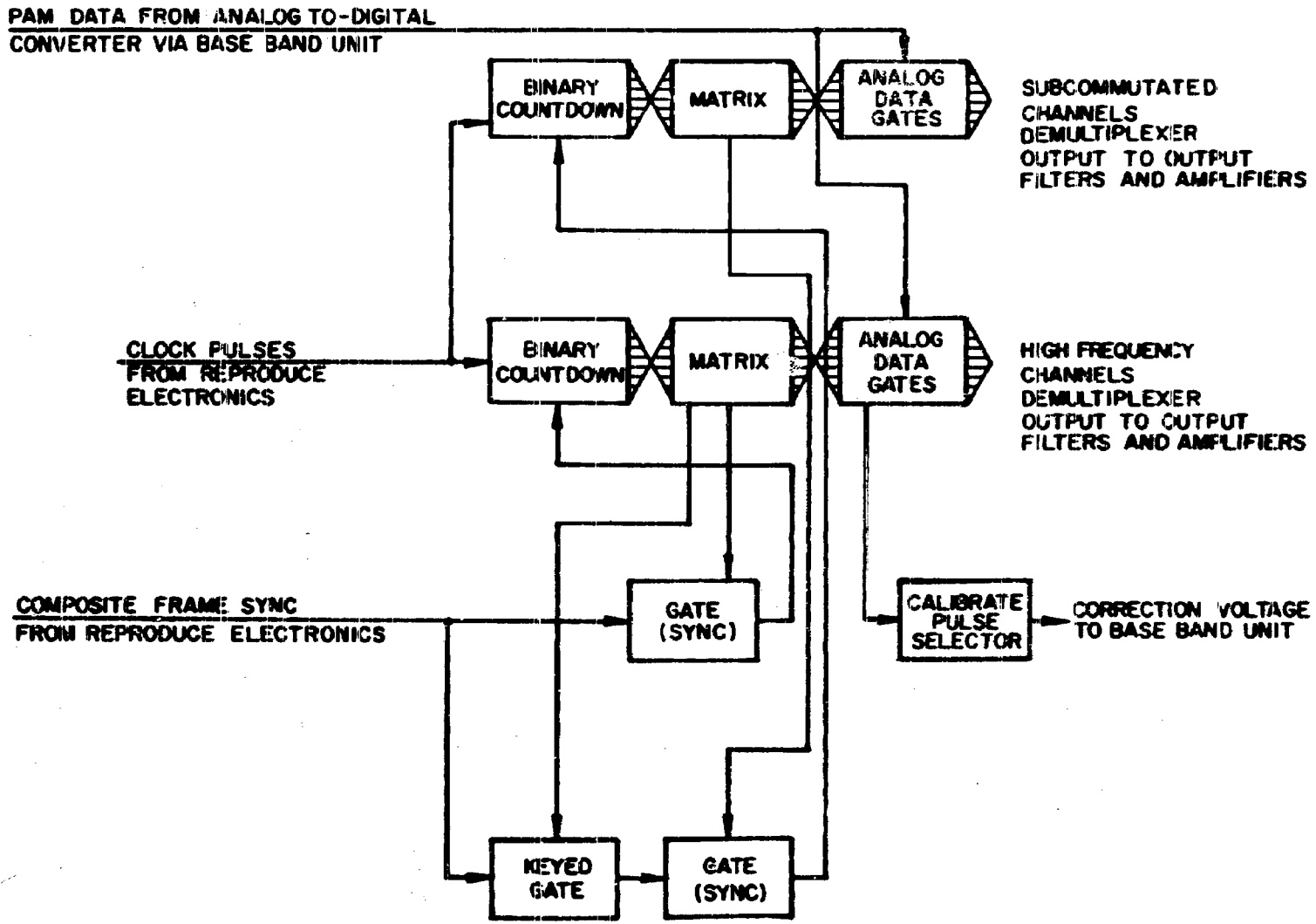


Fig. 7-14 Functional Diagram of Vibration Demultiplexer, Reproduce Mode

This 50 percent duty factor enables the gain of the analog signal to visual display equipment to be the same for record and reproduce modes. To prevent noise from being fed to the Demultiplexer and display circuits, serrations are placed where a minimum of switching noise will appear at the output of Duty Cycle I. Adjustment of the duty factor of the data pulses is possible by adjustments on this circuit. It is composed of two one-shots, a flip-flop, and a keyed gate. A schematic diagram of Duty Cycle I appears in Fig. A-32.

Positive data sync pulses from the Reproduce Electronics appear at pin b for delivery to one-shot no. 1 which is composed of transistors Q1 and Q2 and associated components. One output of one-shot no. 1 goes through the emitter follower composed of transistor Q3 and resistor R11 and turns off transistor Q9 in the flip-flop composed of transistors Q8 and Q9 and associated components. The other output of one-shot no. 1 passes through the emitter follower composed of transistor Q4 and resistor R12 and triggers one-shot no. 2 which is composed of transistors Q5 and Q6 and associated components.

The output of one-shot no. 2 passes through the emitter follower composed of transistor Q7 and resistor R22 and turns off transistor Q8. When this occurs, output of the emitter follower composed of transistor Q10 and resistor R33 will go positive from approximately -15 volts to approximately -5 volts. The output of the emitter follower composed of transistor Q10 and resistor R33 operates the inverting pulse amplifier composed of transistor Q11 and resistors R35 and R36 so that the signal at the junction of resistors R37, R38, and R39 will vary between +10 and -10 volts. These pulses will be out of phase with the output of emitter follower composed of transistors Q12 and Q13 and associated components. Video reproduce from the Gate Driver Amplifier appears at pin Z and is switched on and off by the action of the keyed gate.

The output of the keyed gate is delivered to pin H as serrated video to Data Gates. This output will be at ground potential whenever the gate is <u>not</u> keyed, and will be at data potential whenever the gate <u>is</u> keyed.

The delay produced by both one-shot no. 1 and one-shot no. 2 can be varied between approximately 4 and 25 microseconds. Delay of one-shot no. 1 is varied by adjusting variable resistor R4; its output determines when the keyed gate shall open. The delay of one-shot no. 2 is varied by adjusting variable resistor R15, its output determines when the keyed gate shall close.

7.2.12.2 Frame Sync Delay Reproduce

The Frame Sync Delay Reproduce is a delay network to delay the composite frame sync from the data sync pulses by approximately 5 to 10 microseconds. The composite frame sync pulse is also transformed to the correct impedance and amplitude for driving the Demultiplexer. A schematic diagram of the Frame Sync Delay Reproduce is shown in Fig. A-33. Since the circuit was developed from the sync gate, the flip-flop and one-shot no. 2 as shown on the schematic are not used.

Composite frame sync pulses from the Digital Reproduce Electronics appear on pin Z . This positive pulse is differentiated by capacitor C1, diode CR1, and resistor R1 so that the positive-going portion of the pulses triggers the one-shot composed of transistors Q2 and Q4 and associated components. This one-shot fires blocking oscillator no. 1 composed of transistors Q6 and Q7, transformer T1, and associated components at a time several microseconds after the initial arrival of the composite frame sync pulse. This delay can be varied between 4 and 20 microseconds by adjusting resistor R3, but the delay is usually from 5 to 10 microseconds.

The positive-going output pulses of blocking oscillator no. 1 are delivered to dual emitter follower composed of transistors Q9 and Q11 and associated components. The output level of the dual emitter follower is seen at test point TP1 and is adjusted by variable resistor R26 to 10 ($\pm$ 2.5) volts peak-to-peak.

The gate composed of transistor Q12 and resistors R36 and R37, which is normally open, passes a positive pulse that fires blocking oscillator no. 2 composed of transistors Q13 and Q14, transformer T2, and associated components. The output of blocking oscillator no. 2 is delivered to pin f as the delayed composite frame sync to be delivered to pin Z of the Sync Gate and to pin P of the Sync Selector.

7.2.13 Power Supply Interlock

The basic purpose of the Power Supply Interlock is to prohibit the application of power to any of the components of the PAM-FM Ground Station unless power from all four of the power supplies is present simultaneously. Other functions of this unit are: (1) to provide a time delay between the application of heater power and plate voltage to the Base Band Unit; (2) to provide a means of distributing power to units; and (3) to route various record/reproduce, Magnetic Tape Recorder interlock, and G-A/Vibration relay signals between major components in the Ground Station.

The Power Supply Interlock is composed of 15 relays (two of which are one-minute, thermal-delay relays), a 115-volt-ac isolation transformer which provides power for the 115-volt relays, and various connectors.

Special attention should be given the schematic diagram shown in Fig. A-34 as all controlling signals, their origins and destinations, and the routes of incoming and outgoing power cables are clearly labeled.

7.2.14 Relay Board

The purpose of the Relay Board is to make it possible to shift quickly between record and reproduce modes of Ground Station operation. Several circuit rearrangements among the component boards in the Demultiplexer and other units are required when station modes are switched. In the Demultiplexer, several cards with three DPDT relays each provide the necessary switching. For example, switching between the

Sync Separators and the Sync Reproduce Electronics, or between the Duty Cycle and the Base Band Unit, are all accomplished with Relay Boards, which are in turn driven by the Record/Reproduce controls of the Monitor Panel. A schematic diagram of the Relay Board is shown in Fig. A-35.

7.2.15 Main Monitor Panel

The functioning of main and sub monitor panels as a means of applying "scope probes" rapidly to critical points in the Ground Station is documented in Volume I and in Section 11 of this volume. It should be pointed out that the main monitor panel also performs, by means of nine DPDT relays, most of the switching necessary to change a Ground Station between G-A and Vibration operation. Also, control signals for POWER ON-OFF, RECORD-REPRODUCE, and G-A VIBRATION are initiated by a series of push buttons on the Monitor Panel. A schematic diagram of the Monitor Panel is shown in Fig. A-36.

7.2.16 Signal Strength and Voice Record and Reproduce Filters

The purpose of the Signal Strength and Voice Record and Reproduce Filters is to combine the receiver signal strength output and the voice signal for recording with FM record electronics and to separate the two signals on reproduce. This is done with simple passive filters and a resistive adder which limits the frequency response of the recorded signal strength from dc to approximately 100 cps and the voice signal from approximately 300 cps to 10 kc. A schematic diagram is in Fig. A-37.

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7.3 G-A

7.3.1 Receiver

Input to the G-A Ground Station is received at a modified Nems-Clarke 1412 Telemetry Receiver as a PAM-FM signal. After the FM signal has been demodulated, three signals are delivered to other equipment at the station. A dc-coupled PAM signal is delivered to the Base Band Unit at an average level of approximately +6 volts. A field strength signal is delivered directly from the receiver to the FM electronics of the Magnetic Tape Recorder for recording on an analog track. An ac-coupled signal, to be used as a backup for the digital recording, is delivered through an auxiliary jack to the analog electronics of the Magnetic Tape Recorder for recording on an analog track. The modifications to the Nems-Clarke 1412 Telemetry Receiver provide a dc-coupled output near ground potential and were made to achieve compatibility with the PAM-FM Ground Station in the following manner:

- To provide dc-coupled and ac-coupled video with the phase opposite to that provided by the unmodified receiver
- To provide video with a level independent of any readily accessible adjustment

The modifications were accomplished by bypassing the video amplifier and obtaining an output signal directly from the cathode of the FM discriminator amplifier (V101). A schematic diagram of the modifications is shown in Fig. A-1. Theory of operation and operating and maintenance procedures are described in Instruction Manual for Model 1412 Telemetry Receiver, Nems-Clarke, Inc., Silver Spring, Maryland.

7.3.2 Base Band Unit, Record Mode

The purpose of the Base Band Unit is to

- Amplify the signal from the receiver and provide three separate output signals, each of a different level and isolated from one another

- Insert correct d-c reference level into two of the three output signals
- Limi the bandwidth of the PAM output signals without introducing excessive crosstalk

A block diagram of the G-A Base Band Unit in the record mode is shown in Fig. 7-15.

The three output signals of the Base Band Unit are (1) a 19-volt peak-to-peak signal for the Datrac, (2) a 7-volt peak-to-peak signal for the Demultiplexer data gates, and (3) a 15-volt peak-to-peak signal for the Demultiplexer sync circuits.

The 19-volt peak-to-peak signal for the Datrac must be referenced so that the minimum peak is -9.5 volts. The 7-volt peak-to-peak signal for the data gates is referenced so that zero output of the interpolation filters of the display circuitry corresponds to zero data, i.e., the minimum peak is approximately -1.5 volts. The 15-volt peak-to-peak signal for the sync circuits is not referenced and is a-c coupled.

Since the G-A PAM signal is a 16-kc pulse repetition rate, it can be considered a relatively low-speed system.

The video output of the receiver is followed by a noise filter which limits the bandwidth to that required to pass the PAM signal and removes the excess noise. The characteristics of the noise filter are determined by the total sampling rate, the overall system accuracy, and the allowable crosstalk between successive samples. For the G-A Ground Station, an R-C filter is sufficient to accomplish this purpose.

Two signals flow through the Base Band Unit. One is the PAM pulse train, the other is the d-c reference feedback correction voltage that is derived from a portion of the pulse train.

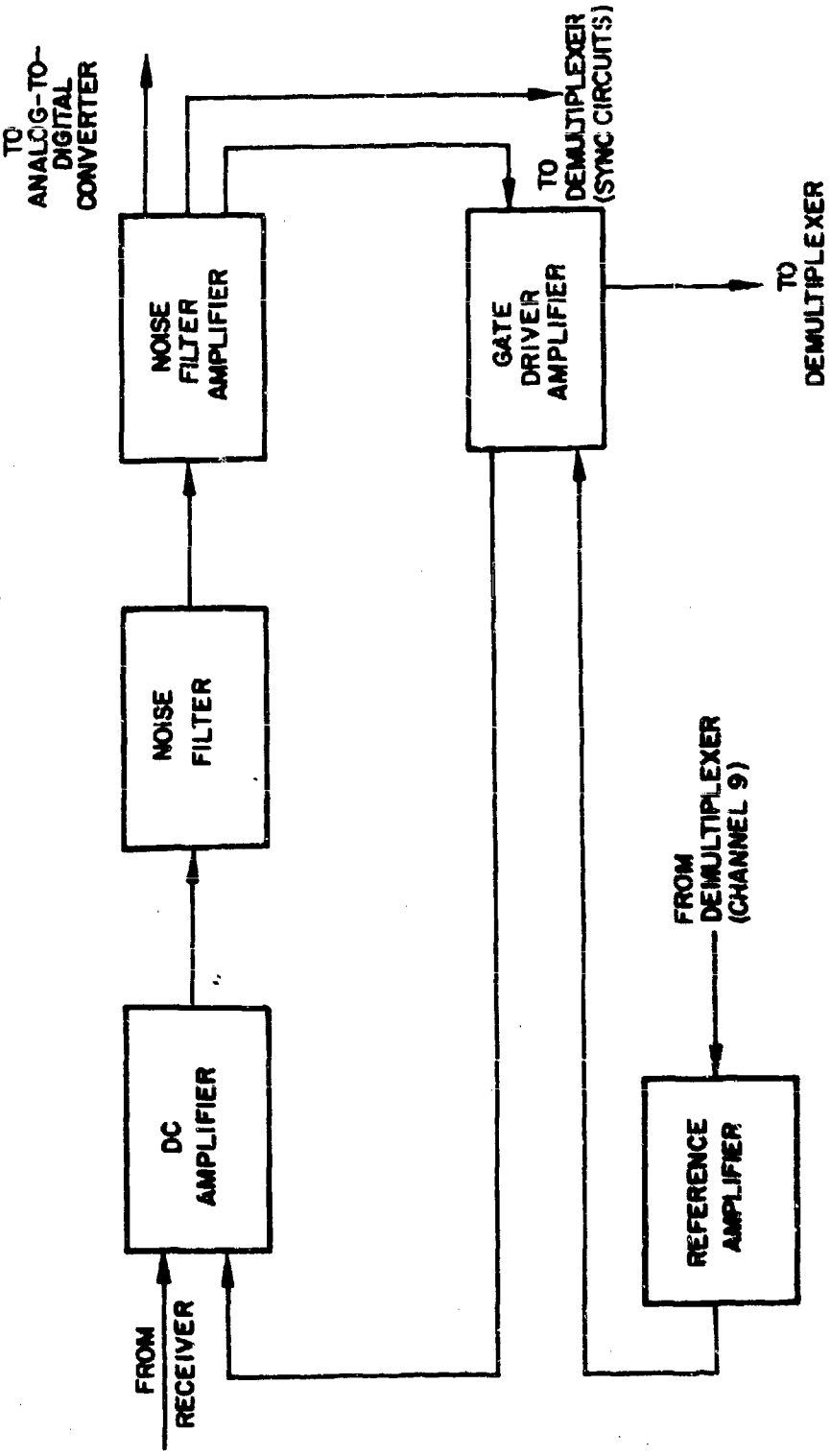


Fig. 7-15 G-A Base Band Unit, Record Mode

The signal from the receiver, which is approximately 1.4 volts peak-to-peak in amplitude, enters the DC Amplifier where it is amplified approximately 10 times without being inverted. This amplifier is composed of direct-coupled circuits. A suitable means of offsetting positive bias voltage from the receiver is included.

The output of the DC Amplifier, which is now at a level of approximately 14 volts peak-to-peak, is fed into the Noise Filter, a single-pole, R-C section. Here, the signal-to-noise ratio of the PAM pulse train is improved without the introduction of excessive crosstalk and approximately 3 volts of negative offset voltage are added to the output signal.

This signal is delivered to the Noise Filter Amplifier at a level of approximately 4 volts because of attenuation in the Noise Filter. The signal is then amplified so that the Noise Filter Amplifier output to the Datrac is 19 volts peak-to-peak. An adjustment, called the Overall Gain, is involved in this amplifier to achieve the desired amplification. An additional adjustment to correct the d-c level to -9 ($\pm$ 0.25) volts is also included in the Noise Filter Amplifier. This signal which is delivered to the Datrac can be routed through the Reference Voltage Optional Clamp circuit if the Demultiplexer should fail to deliver the correct d-c reference voltage.

At this point in the signal flow of the Base Band Unit, the PAM pulse train is divided into three outputs. One output is the 19-volt peak-to-peak signal to the Datrac, another is the 15-volt peak-to-peak signal to the Demultiplexer sync circuits, and the third is the dc-coupled signal to the Gate Driver Amplifier.

The Gate Driver Amplifier is used to attenuate the 19-volt peak-to-peak signal to a 7-volt signal and supply a low source impedance to drive the data gates. A d-c offset adjustment is incorporated to adjust the minimum peak (sync interval) to approximately -1.5 volts. Incorporated in the Gate Driver Amplifier is a relay activated by the Record-Reproduce switch in the Monitor Panel so that the input to the data gates by way of the Gate Driver Amplifier can be routed from the Datrac or the Noise Filter

Amplifier, depending on the mode of operation.

The d-c reference correction voltage originates in the Demultiplexer where the sync interval is sampled by the DC Reference Filter Board and smoothed through a 1-kc low-pass filter. This signal is then delivered to the Reference Amplifier of the Base Band Unit where the d-c error voltage is amplified approximately 500 times and delivered to a single-pole, R-C section, low-pass filter with a cutoff frequency of 2 cps. This filter is physically located in the Gate Driver Amplifier. The d-c correction voltage is switched by a relay in the Gate Driver Amplifier to a differential input of the DC Amplifier in the record mode or to a differential input of the Gate Driver Amplifier in the reproduce mode.

7.3.2.1 DC Amplifier

The purpose of the DC Amplifier is to amplify the incoming PAM signal approximately 10 times and establish a d-c reference level of approximately -2 (± 2) volts. These functions are performed by using three dual triode (6201) vacuum tubes and their associated components. The first two cathode-coupled triodes (V1 and V2) act as a comparison amplifier that amplifies the difference of the signals appearing on grids 2 and 7 of V1. The third cathode-coupled dual triode (V3) acts as a parallel cathode follower and furnishes a low output impedance to the Noise Filter. Zener Diodes are used to correct the d-c offset throughout the Amplifier. A schematic diagram of the DC Amplifier is shown in Fig. A-2.

Two inputs to the DC Amplifier are provided. One input is the PAM pulse train from the receiver; the second is the d-c reference level from the second low-pass filter in the d-c reference feedback loop.

The PAM signal from the receiver is picked up at jack J4 at a level of approximately +6 volts dc. It is passed through Zener coupling diode CR7 where the level is reduced to approximately zero volts dc. This signal is then applied to grid 2 of V1A. At

the same time, the signal input from the Reference Amplifier, by way of the second low-pass filter, is applied to grid 7 of V1B by way of a network composed of resistors R9, R10, and R11.

In order to exercise adequate control over the d-c offset voltage, it is necessary to balance the plate current being applied to V1A and V1B, the first stage of the amplifier. This is accomplished by means of potentiometer R2 (DC Balance no. 1). While this adjustment is being made at R2, the input from the Reference Amplifier is disconnected at jack J5. Resistor R2 is adjusted so that the sync interval (absence of a data pulse) is approximately -2 ($\pm$ 2) volts dc as observed at test point TP3.

The output of V1B is passed through an offset voltage control network composed of diodes CR1, CR2, and CR3 which reduces the d-c voltage by 180 volts ($\pm$ 10 percent). The signal is then applied to grid 2 of V2A. The cathode of V2A is coupled to the cathode of V2B, which is next to receive the signal. At the same time, there appears on grid 7 of V2B the signal from the output of V3, a part of the amplifier's internal feedback circuit.

The output from the plate of V2B is passed through a second offset voltage control network composed of diodes CR4, CR5, and CR6 which reduces the d-c voltage by 180 volts ($\pm$10 percent). Capacitors C2 and C3 are used to suppress the high-frequency noise generated in the two Zener diode strings CR1, CR2, and CR3; and CR4, CR5, and CR6.

The signal is then applied in parallel to grids 2 and 7 of V3A and V3B, the parallel cathode follower. The output of this parallel cathode follower is delivered through jack J6 to the Noise Filter. At the same time, this output is fed back to the grids of V2B and V1B by means of the feedback resistors R9, R10, R15, and R16. Feedback resistors R9 and R10 are used to control the overall gain of the DC Amplifier to approximately 10.

There are three test points in the DC Amplifier. Test point TP1 provides a

sampling point for the input from the receiver after passing through the 6-volt Zener diode CR7. Test point TP2 provides a sampling point for the input from the Reference Amplifier. Test point TP3 provides a sampling point for the output of the DC Amplifier. The input from the receiver, after passing through the 6-volt Zener diode CR7, is also delivered to the Monitor Panel through jack J1 as the RCVR VIDEO DC position on Switch A and Switch B.

A jumper between jacks J2 and J3 is normally used with the DC Amplifier. Should an occasion arise when operation with the composite pulse train from some source other than the receiver is desired, however, the jumper could be removed and the input applied to jack J2.

7.3.2.2 Noise Filter

The purpose of the Noise Filter is to improve the signal-to-noise ratio of the composite pulse train without introducing excessive crosstalk. It is composed of a time delay circuit, a summing junction, a d-c offset adjustment circuit, and an output circuit. Internal switching and separate plug-in output circuits permit use with both Vibration and G-A Ground Stations. Input to the Noise Filter from the DC Amplifier is at jack J7 and its output to the Noise Filter Amplifier is at jack J8. A schematic diagram of the Noise Filter, including circuits used in both Vibration and G-A operation, is shown in Fig. A-3.

With the SYSTEM switch on the Monitor Panel set at the G-A position and a G-A plug-in unit in place, all Noise Filter components needed in the G-A system are in operation. In G-A operation, the Noise Filter is a single-pole, R-C section with a cutoff frequency of 2.2 times the sampling rate, or about 35 kc. No adjustment of the delay attenuator or tuning capacitor controls is required with the Noise Filter in the G-A mode of operation, because no delays or tuned circuits are used; both the time delay and summing junction circuits are inoperative. Bandlimiting of the composite pulse train is accomplished with the R-C filter alone, and the

resulting crosstalk is held to a tolerable level.

The signal is delivered through resistors R2 and R3 to both grids 3 and 8 of tube V1 which acts as a parallel cathode follower. Output to the R-C filter is delivered to the junction of resistors R7 and R8, and output to the Noise Filter Amplifier is the voltage developed across capacitor C2 of the plug-in unit.

D-C offset adjustment is accomplished by a circuit composed of tube V2 and its associated components. By varying the operating point of V2 with the DC Offset no. 1 control, resistor R13, d-c current flowing out of the junction of resistors R7 and R8 can be changed, and the resulting I-R drop becomes offset voltage. This adjustment is made so that there is 3.5 ($\pm$ 0.5) volts offset between jacks J7 and J6. Offset conditions should always be checked when changing from one system (Vibration or G-A) to the other.

7.3.2.3 Noise Filter Amplifier

The purpose of the Noise Filter Amplifier is to amplify the signal delivered by the Noise Filter so that the peak-to-peak voltage with full modulation is 19 ($\pm$ 1) volts. The signal level must be such that the sync level (absence of data pulse) is -9.5 ($\pm$ 0.25) volts. These functions are performed by using two 6201 dual-triode vacuum tubes and one 6463 dual-triode vacuum tube, and their associated components. The first two cathode-coupled triodes (V1 and V2) act as a comparison amplifier that amplifies the difference of the signals appearing on grids 2 and 7 of V1. The third cathode-coupled triode (V3) acts as a parallel cathode follower and furnishes a low output impedance. Zener diodes are used to correct the d-c offset throughout the amplifier. A schematic diagram of the Noise Filter Amplifier is shown in Fig. A-4.

The signal is delivered to the Noise Filter Amplifier at jack J9 and applied to grid 2 of V1. At the same time, the signal appears at grid 7 of V1 as feedback from

cathode follower V3. Plate current to V1 is balanced by means of DC Balance no. 2. In order to make this adjustment, it is necessary to disconnect the input signal at jack J9. Test point TP3 should go to ground potential when the adjustment is properly made.

The output of plate 6 of V1 is delivered to grid 2 of V2, the second cathode-coupled dual triode, through an offset voltage control network composed of diodes CR1, CR2, and CR3 which reduces the d-c voltage by 180 volts ($\pm$ 10 percent). Cathode 2 of V2 is coupled to cathode 8, which is next to receive the signal. At the same time, the signal from the output of V3, a part of the amplifier feedback circuit, appears on grid 7 of V2.

The output from plate 6 of V2 is passed through a second offset voltage control network composed of diodes CR4, CR5, and CR6 which reduces the d-c voltage by 180 volts ($\pm$10 percent). Capacitors C1 and C2 are used to suppress the high-frequency noise generated in the two Zener diode strings.

The signal is then applied to grid 3 of cathode follower V3. The output of this half of V3 appears on cathode 2. This output is delivered to grid 7 of V2 and grid 7 of V1 through resistors R7, R8, R9, and R13 which act as voltage dividers of a feedback circuit within the Noise Filter Amplifier. This output is also coupled to jacks J11 and J12. At the same time, a part of this output is delivered to grid 8 of V3 through resistor R17 and variable resistor R18. The output of this half of V3 appears on cathode 7 and is ac-coupled to the Sync Separator the Demultiplexer through jack J10. Capacitor C4 acts as a blocking capacitor to prevent high voltage from entering the Demultiplexer.

There are two adjusting points in this circuit in addition to DC Balance no. 2, which was described earlier. Both of these points, resistors R8 and R18, are adjusted with the input from the Noise Filter connected to jack J9. Resistor R8 (Overall Gain) is set so that the peak-to-peak voltage with full modulation is

19 ($\pm$ 1) volts at test point TP8. It is advisable to recheck the adjustment of DC Balance no. 3 after resistor R8 is adjusted to assure that ground potential is present without signal input. Variable resistor R18 (a-c gain) is adjusted so that the peak-to-peak voltage with full modulation is 15 ($\pm$ 2) volts at test point TP7.

The output at jack J11 is connected to the Reference Voltage Optional Clamp where a switch delivers the signal directly to the Datrac and the Gate Driver Amplifier or may be clamped to a d-c reference voltage before delivery to the Datrac and Gate Driver Amplifier.

There are three test points in the Noise Filter Amplifier. Test point TP6 furnishes a sampling point for the input from the Noise Filter; test point TP7 furnishes a sampling point to the a-c video output to the Demultiplexer; and test point TP8 furnishes a sampling point to the d-c video output to the Reference Voltage Optional Clamp.

The Noise Filter Amplifier has three outputs. One output is delivered to the dc-coupled Analog-to-Digital Converter. The signal is also fed ac coupled to the sync circuits in the Demultiplexer. Peak-to-peak amplitude of this signal is 15 ($\pm$ 2) volts. The third output of this unit, which is identical to the output going to the Analog-to-Digital Converter, is delivered to the Gate Driver Amplifier.

7.3.2.4 Reference Voltage Optional Clamp

An optional Clamp circuit is included in all Vibration and G-A Ground Stations with record capabilities. The purpose of the Clamp is to increase the reliability of the station in the record mode by allowing the operator an optional method of restoring the correct d-c record level in case the main d-c correction circuit fails. A schematic diagram of the Reference Voltage Optional Clamp is in Fig. A-5.

The Clamp circuit is contained in a 2-3/4 in. by 2 in. box that is mounted on top

of the case containing the Reference Amplifier in the Base Band Unit. The switch position on the clamp box is labeled CLAMP - SERVO. When the switch is in the SERVO position, the clamp is eliminated from the circuit, and the reference level is furnished by the d-c correction circuit. When the switch is in the CLAMP position, the d-c correction circuit is eliminated and the clamp furnishes the appropriate d-c correction level.

The clamp level is fixed at -9 ($\pm$ 0.5) volts by an SV-9 Zener diode. In order that the d-c record levels remain approximately the same for the CLAMP or SERVO positions, the main d-c correction circuit must be set up to match the clamp level.

7.3.2.5 Gate Driver Amplifier

The Gate Driver Amplifier furnishes a gain factor of approximately 0.33 and a d-c voltage offset so that a zero signal at the vehicle multiplexer results in a zero signal at the output of the Demultiplexer. This unit delivers the signal to the Demultiplexer.

This amplifier is made up of a comparison amplifier, a positive peak limiter, a cathode follower, an offset control, and an output clipper. To facilitate switching between the record and reproduce modes of operation, the Reference Amplifier low-pass filter is included as a part of the Gate Driver Amplifier. A schematic diagram of this circuit is shown in Fig. A-6.

In the record mode of operation, either the Reference Voltage Optional Clamp or the Noise Filter Amplifier furnishes the input to the Gate Driver Amplifier. In the reproduce mode of operation, the Datrac furnishes the input to the Gate Driver Amplifier. The input signal appears at jacks J13 or J14, depending on the mode of operation, and is delivered to grid 2 of V1 (a dual-triode vacuum tube 6201 which acts as a cathode-coupled comparison amplifier) through the resistors R1, R2,

and R3 which serve as a voltage divider and attenuator. The output of plate 6 of V1 is passed through diode CR1 for offset voltage control, causing the voltage to drop 180 volts (± 10 percent). Capacitor C3 suppresses the high-frequency noise generated by diode CR1. The signal is then passed through the positive peak limiter, composed of variable resistor R13 (limiter bias), diode CR2, and capacitor C4, and is delivered in parallel to grids 3 and 8 of cathode follower V2, a 6463 dual-triode vacuum tube. The output of V2 (cathodes 2 and 7) is passed through a voltage offset adjustment network composed of diodes CR3, CR4, and resistor R18 (DC Offset no. 2). The signal is then delivered to jack J17 through an output clipper composed of diodes CR5 and CR7. This clipper prevents the output to jack J17 from going beyond +10 or -5.6 volts.

Also included in the Gate Driver Amplifier is the second low-pass filter for the d-c reference feedback loop. This filter consists of resistor R4 and capacitors C1 and C2. Input to the filter is from the Reference Amplifier. In the record mode of operation, the filter output is delivered to the differential input of the DC Amplifier. In the reproduce mode of operation, since the DC Amplifier is not used in this mode, the filter output is delivered to the differential input (grid 7 of V1) of the Gate Driver Amplifier through resistors R11 and R14. This unit filters out unwanted frequencies and prevents hunting.

7.3.2.6 Reference Amplifier

The Reference Amplifier has a variable gain from 10 to 2500 to amplify the d-c correction feedback voltage. A gain of 500 is normally used during operation of the Ground Station in the G-A mode. The output is delivered first to the second low-pass filter contained in the Gate Driver Amplifier and then to the differential input of the DC Amplifier in the record mode of operation, or to the Gate Driver Amplifier in the reproduce mode of operation.

The circuitry of this amplifier is described in detail in the Handbook of Operating

and Maintenance Instructions, A-12 DC Amplifier, supplied with the Ground Station. A schematic diagram of the amplifier is shown in Fig. A-7, Sheets 1 through 3.

The input to the Reference Amplifier is of a differential type with respect to ground in order to reduce ground loop problems. This input from the DC Reference Filter Board in the Demultiplexer appears at jack J25 at approximately 0 volts (within a few millivolts) when the feedback loop is closed. If instability of the video base line is noted, the gain should be reduced until stability is achieved. This instability will be noted at test point TP11 in the Gate Driver Amplifier. Random noise may be present, but it is filtered out by the low-pass filter in the Gate Driver Amplifier. The output at jack J23 should be 0 ($\pm$ 5) volts and must never exceed $\pm$10 volts as this level would represent loss of operation of the d-c reference feedback loop. Although no damage to the equipment would result with the output approaching these limits of $\pm$ 10 volts, data recovery accuracy of the Ground Station would suffer appreciably.

7.3.3 Demultiplexer, Record Mode

A functional diagram of the G-A Demultiplexer in the record mode of operation is shown in Fig. 7-16. The three principal functions of the Demultiplexer are: (1) to separate the data sync pulse from the composite data signal for use as a clock pulse for the Demultiplexer and the Analog-to-Digital Converter (Datrac) and to generate frame sync pulses from the composite data signal; (2) to supply keying signals for the Sample and Hold circuitry; and (3) to sample the sync interval that appears on Channels 1 and 9 and send it through a high-gain Reference Amplifier in the Base Band Unit as a d-c correction voltage fed into the differential DC Amplifier.

Since the Ground Station is slaved to the vehicle clock, a clock signal must be recovered from the composite pulse train. This is done in the data sync generator where a pulse is generated for every analog pulse and sync interval in the PAM

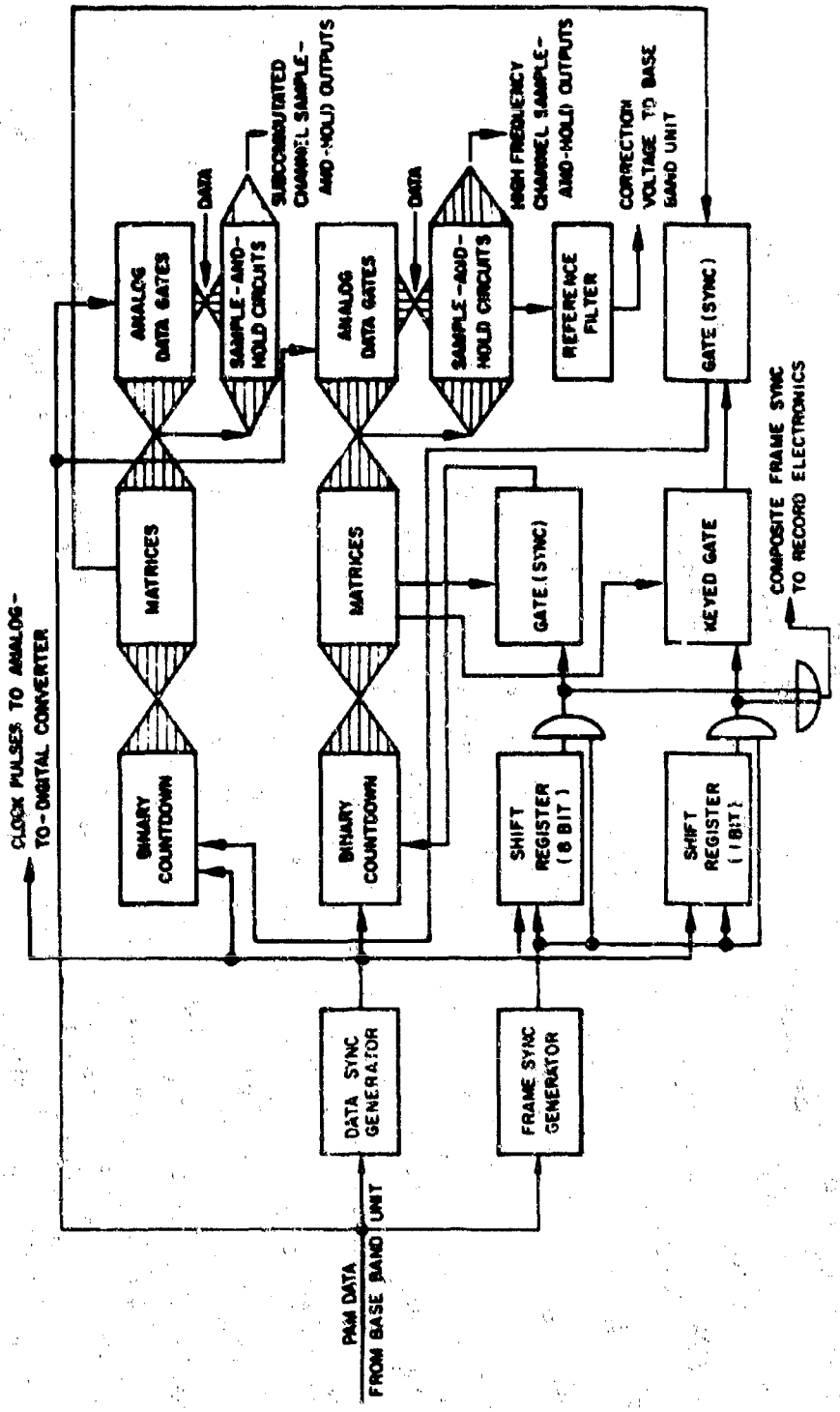


Fig. 7-16 Functional Diagram of G-A Demultiplexer, Record Mode

pulse train. The phasing can be controlled to give the appropriate time relation between the clock signal thus generated and the analog data pulses from the Base Band Unit.

One output of the data sync generator is used to drive the binary countdown that produces the square-wave signals used for "ANDing" purposes in the matrices. The output of the matrices are keying signals for the analog data gates and the Sample and Hold Circuits which receive their input in the form of the PAM analog pulse train from the Gate Driver Amplifier in the Base Band Unit. These sequential keying signals to the analog data gates are on separate lines and are connected to the appropriate analog data gates which open and close in correspondence with the keying signals. The "on" time of any one high-frequency data gate is the clock period, or 62.5 microseconds. The "off" time is one frame minus the clock period, or 1937.5 microseconds. The "on" time for a subcommutated data gate is the same as the "on" time for a high-frequency data gate, or 62.5 microseconds. The "off" time of the subcommutated data gate is eight frames minus one clock period, or 15,937.5 microseconds.

To keep the Demultiplexer in synchronization with the PAM pulse train (i.e., to open analog data gate no. 1 when each channel of the PAM pulse train is delivered from the Base Band Unit), a frame synchronization pulse is used. Frame synchronization pulses are generated in the frame sync generator which produces a pulse whenever a pulse is missing in the PAM pulse train. To ensure that this pulse is a valid sync pulse and not a stray pulse as might be generated in the presence of r-f noise interference or a faulty multiplexer, a certain amount of logic is incorporated into the circuitry.

Frame sync occurs on Channels 1 and 9. Therefore, any potential sync pulse is delayed exactly eight channels by means of an eight-bit shift register and compared in a logic gate with other potential frame sync pulses being generated. This will produce a frame sync pulse output only when missing pulses occur exactly eight channels apart. This provides protection against the generation of spurious frame

sync pulses by faulty data pulses. Once apparent frame sync has been established, a sync gate is triggered, which opens to receive a sync pulse only when one is expected as determined by the high-frequency binary countdown and matrix. When the sync pulse arrives, it closes the gate and blocks any spurious pulses. If the sync pulse does not arrive as expected, the sync gate remains open until sync is again established. This logic performs the function of blocking periodic and nonperiodic false sync pulses as well as the subcommutated sync pulse, which appears as a nonperiodic sync pulse to the high-frequency binary countdown.

Subcommutate frame sync occurs on Channel 32. Therefore, the train of potential sync pulses is delayed exactly one channel by a one-bit shift register and compared in a logic gate with potential frame sync pulses being generated by the Frame Sync Separator. This will produce a frame sync pulse output only when missing pulses occur exactly one channel apart. These pulses are fed into a keyed gate that is triggered by the Channel 1 keying pulse from the matrix. Thus, after the main-channel pulse sequencer has been synchronized, the keyed gate allows subcommutated sync pulses to pass through the keyed gate only during Channel 1 time. The output of the keyed gate is delivered to a subcommutated sync gate which operates in the same fashion as the high-frequency gates except that it is controlled by the subcommutated countdown and matrix.

The two signals appearing at the input of the high-frequency and subcommutated sync gates are delivered to the Digital Record Electronics for recording on a digital track. These signals are combined into one line by means of an OR gate.

7.3.3.1 Data Sync Separator

The purpose of the Data Sync Separator is to extract data sync and clock information from the composite pulse train (a-c video). The Data Sync Separator is composed of the following circuits: clamp and clipper, band-pass filter, pulse shaper, clipper amplifiers, one-shot, emitter follower, and blocking oscillator. (For a

schematic diagram, see Fig. A-38). Clock output occurs in the form of a square wave or pulses; data sync is in the form of pulses only. Clock information is in time phase with data sync information. Data sync output is actually clock information which has been delayed so that keying pulses for the data gates occur at a time when interchannel crosstalk is at a minimum. The Q of the band-pass filter is such that clock and data sync outputs are present when as many as approximately 30 consecutive data pulses are missing. Operation of the Data Sync Separator ceases whenever more than approximately 30 consecutive data pulses are missing.

The composite pulse train input (a-c video) from the Noise Filter Amplifier appears at pin J. It then enters the clamp and clipper circuit, which is composed of diodes CR3 and CR4, transistors Q3 and Q6, and associated components. This circuit restores the d-c level to the a-c video and clips it below minimum data level. Resistor R13 is adjusted so that positive peak clipping occurs at minimum data level, 1.5 ($\pm$ 2) volts. Test point TP1 - the junction of diode CR4 and resistor R-13 - should be observed when this adjustment is being made.

The output from the clamp and clipper circuit passes through the emitter follower composed of transistor Q6 and resistor R19 into the band-pass filter. This band-pass filter is a ringing, oscillator-type circuit in which the resonant frequency is that of the sampling rate of the composite pulse train. The output level control of the clamp-and-clipper circuit resistor R19 is adjusted so that the peak-to-peak amplitude of the output sine wave at the junction of capacitor C14 and diode CR7 is 15 ($\pm$ 1) volts. Fine tuning of the tank circuit is made by adjusting capacitor C13A.

The signal is coupled into the pulse shaping network through capacitor C14. Transistors Q14 and Q17, diode CR7, and associated components are a dual emitter follower and clamp circuit. Its output is fed into the clipper circuit composed of diodes CR9 and CR10, transistor Q19, and associated components.

Silicon diodes CR9 and CR10 change the sine wave from the dual emitter follower into an approximately square wave.

This square wave is coupled into the clipper amplifiers through the emitter follower transistor Q19 and resistor R52. There are two saturating-type amplifier stages and two emitter follower stages in the clipper amplifier circuitry. The two amplifiers are transistors Q8 and Q7 with their associated components; the two emitter follower stages are transistors Q 5 and Q 9 with their associated components. The signal is amplified but not inverted, and the output is fed into four succeeding emitter followers in parallel. Output of the clipper amplifiers, which is now a square wave, passes through the emitter follower transistor Q8 and associated components to pin M and through the emitter follower transistor Q10 and associated components to pin R. These two clipper amplifier outputs are then delivered as a clock square wave to the eight-bit shift register (pin M) and to the frame sync separator (pin R). Output of the clipper amplifiers is also fed to a one-shot through the emitter follower transistor Q12 and associated components. Positive-going portions of the square wave trigger the one-shot, which is composed of transistors Q15 and Q18 and associated components. The variable delay of approximately 4 to 25 microseconds is adjusted by resistor R39 in such a manner that the data gates are keyed when minimum interchannel crosstalk occurs. One-shot output (monitored at the junction of capacitor C21 and resistor R51) is a series of positive pulses. These pulses fire a blocking oscillator composed of transistors Q13 and Q16, transformer T1, and associated components. Output of the blocking oscillator consists of data sync pulses which are fed to the pulse sequencer and frequency divider at pin b. Finally, the output from the clipper amplifiers passes through emitter follower composed of transistor Q1 and associated components, differentiating circuit capacitor C4, diode CR2, resistor R8, emitter follower transistor Q4, and associated components to pin T. This output is then delivered as a series of positive clock pulses to the Data Sync Relay Record.

7.3.3.2 Frame Sync Separator

The Frame Sync Separator produces a pulse whenever a data pulse is absent in the composite pulse train. This unit is adjusted so that whenever the level of a data pulse falls below a 0.5-volt level with reference to the base line, a pulse is produced. The unit is made up of the following functioning circuits: d-c restorer, positive peak clipper, adder, decision level inverting amplifier, one-shot, and three blocking oscillators. (For schematic diagram see Fig. A-39.)

The composite pulse train (a-c video) input is delivered to pin J. It is then clamped to a few tenths of a volt, positive d-c, by means of the d-c restorer composed of capacitors C2 and C4, diode CR2, diode CR11, and resistor R3.

The signal is then delivered to the positive peak clipper set to clip below minimum data level, which is approximately +2 volts as monitored at test point TP1. This clipper is composed of transistor Q1, diode CR3, and associated components. The clipping level is adjusted by varying resistor R8.

Clock square wave from the Data Sync Separator appears at pin R. It is delivered to the clock blocking oscillator composed of transistors Q6 and Q7, transformer T1, and associated components. The output of this blocking oscillator is delivered to pin S as reset pulses to the Eight-Bit Shift Register. It also is delivered to the one-shot composed of transistors Q8 and Q9 and associated components. This multivibrator introduces a variable time delay from 4 to 25 microseconds. The time delay is set by adjusting resistor R26. The output is delivered as clock pulses to a delayed blocking oscillator composed of transistors Q10 and Q11, transformer T3, and associated components.

The output of this blocking oscillator is delivered to the adder composed of resistor R10. This adder combines the clipped composite pulse train and delayed data sync. Resistor R26 in the one-shot circuit is adjusted so that the negative-going

blocking oscillator pulses (Fig. 3-3) are centered on the data pulses as they are monitored at test point TP2.

The output of the adder is delivered to the decision level inverting amplifier composed of transistors Q3 and Q4, diode CR5, and associated components. This amplifier selects the blocking oscillator pulses which coincide with the absence of data pulses and provides a positive-going pulse to fire the output blocking oscillator composed of transistors Q4 and Q5, transformer T2, and associated components.

The output blocking oscillator provides composite frame sync pulses which are delivered to the Eight-Bit Shift Register and the Sync Selector at pin P. Resistor R10 is adjusted so that the blocking oscillator fires reliably whenever a data pulse is absent and does not fire under any other conditions. A good setting of R10 would be halfway between (1) the setting that just begins to fire the output blocking oscillator at clock rate, and (2) the setting that stops firing the output blocking oscillator at data pulse absence rate. This setting can be monitored at pins J and P.

7.3.3.3 Eight-Bit Shift Register

The purpose of the Eight-Bit Shift Register is to store data pulse absence or sync pulse information for eight clock periods (of time) and present to a succeeding AND gate direct and stored sync pulse outputs.

This unit is composed of a series string of nine delay-coupled flip-flops, four output emitter followers, and a clock driver. The schematic diagram is shown in Fig. A-40.

The first flip-flop acts as a buffer stage for the succeeding eight units in the shift register. It stores the sync pulses until the clock shifts this information into the first storage flip-flop.

Three inputs are provided: reset (clock) pulses from the Frame Sync Separator

appear at pin S; sync pulses from the Frame Sync Separator appear at pin P; and the clock square wave from the Data Sync Separator appears at pin M.

The reset pulse on pin S passes through diode CR1 and saturates transistor Q1. When a sync pulse is present at pin P, current passes through diode CR2 causing Q3 to saturate and the collector of transistor Q1 to go to high potential. This allows capacitor C5 to charge through R10 because diode CR7 is back-biased when transistor Q2 of the clock driver is cut off with a negative clock pulse. When transistor Q2 is saturated with a positive clock pulse, diodes CR7 and CR8 conduct because of the previous charge on capacitor C5. This current flowing through diode CR8 cuts off transistor Q4 and saturates transistor Q5, thus setting up the first storage flip-flop.

In a like manner, the absence of a sync pulse will cause the first storage stage to be set up in the opposite way with transistor Q5 cut off and transistor Q4 saturated. This process continues through succeeding stages until the last stage is reached.

Two outputs are provided by the output emitter followers. One output represents stored sync pulses at pin U for delivery to the One-Bit Shift Register. The other output represents direct sync pulses at pin K for delivery to the One-Bit Shift Register.

7.3.3.4 One-Bit Shift Register

The purpose of the One-Bit Shift Register is to extract subcommutated sync pulses from the Frame Sync Separator sync pulses and to combine them with sync pulses from the Eight-Bit Shift Register. A schematic diagram of the One-Bit Shift Register is shown in Fig. A-41.

This unit is composed of two delay-coupled flip-flops. The first flip-flop acts as a buffer stage and the second as a storage stage. Also included are two AND gates, an OR gate, and a blocking oscillator.

Five inputs are provided. Reset pulses from the Frame Sync Separator appear at pin S. Sync pulses from the Frame Sync Separator appear at pin P. Direct sync pulses from the Eight-Bit Shift Register appear at pin K. Stored sync pulses from the Eight-Bit Shift Register appear at pin X. The clock square wave from the Data Sync Separator appears at pin M.

The single output consists of sync pulses for delivery to the main frame Sync Gate and to the Sync Selector. These pulses appear at pin f.

The reset pulse on pin S passes through diode CR2 and causes transistor Q2 to saturate. When a sync pulse is present at pin P, current passes through diode CR3 causing Q3 to saturate and the collector of transistor Q2 to go to a high potential. This allows capacitor C5 to charge through R11 because diode CR6 is back-biased when transistor Q1 is cut off with a negative clock pulse. When transistor Q1 is saturated with a positive clock pulse, diodes CR6 and CR9 conduct because of the previous charge on capacitor C5. This current flowing through diode CR9 cuts off transistor Q4 and saturates transistor Q5, thus setting up the storage flip-flop. In a like manner, the absence of a sync pulse will cause the storage stage to be set up in the opposite way, with transistor Q5 cut off and transistor Q4 saturated.

The output of the storage flip-flop now passes through an emitter follower composed of transistor Q6 and resistor R16 into an AND gate composed of diodes CR12 and CR13 and resistor R8. This output corresponds to the presence of a sync pulse on pin P delayed for one bit of time.

An output from the buffer flip-flop is taken from the collector of transistor Q2 and corresponds to the presence of a sync pulse on pin P. It passes to the AND gate through the emitter follower composed of transistor Q7 and resistor R17, where it is ANDed with the information from the storage flip-flop. The output of the AND gate (junction of CR12, CR13, and R8) is a positive pulse which corresponds to the presence of two sync pulses on pin P one bit of time apart.

This output now passes into an OR gate composed of transistors Q8 and Q9, and resistor R20. The second AND gate, composed of diodes CR14 and CR15 and resistor R19, ANDs direct and stored sync pulses from the Eight-Bit Shift Register. The output of the second AND gate, which corresponds to the presence of sync pulses eight bits of time apart on pin P, also passes to the OR gate. The output of the OR gate is coupled through capacitor C6 to the blocking oscillator composed of transistors Q10 and Q11, transformer T1, and associated components.

The output of the blocking oscillator is delivered to pin f as sync pulses to the main frame Sync Gate and to the Sync Selector.

7.3.3.5 Sync Selector

The purpose of the Sync Selector is to combine sync pulses for recording purposes in such a manner that only sync gate and keyed gate circuitry need be used to produce both main and subcommutated frame sync while in the reproduce mode. A schematic diagram of the Sync Selector is shown in Fig. A-42.

In G-A, main frame sync pulses from the high-frequency sync gate appear on pin Z and sync pulses from the One-Bit Shift Register appear on pin P.

Sync pulses enter at pin P and pass through an emitter follower composed of transistor Q1 and resistors R2 and R4. These pulses then enter the gate circuit, which is composed of transistors Q3, Q4, and Q5 and associated components, at the emitter of Q4. Series switch Q4 and shunt switch Q5 are keyed by a pulse amplifier composed of transistor Q3 and resistors R3 and R7. This pulse amplifier is operated by subcommutated keying pulses, which appear on pin K in such a manner that the presence of a keying pulse opens the gate and the absence of a keying pulse closes the gate. Output pulses from the gate are passed through the emitter follower composed of transistor Q7 and resistor R12 for delivery to pin d as the subcommutated sync pulse to sync gate. Output pulses from the gate are also passed through the

emitter follower composed of transistor Q6 and resistor R11 and are coupled through capacitor C4 for delivery to the blocking oscillator, which is composed of transistors Q8 and Q9 and transformer T1.

Sync pulses also enter at pin Z and pass through emitter follower composed of transistor Q2 and resistor R6 and are coupled through capacitor C3 for delivery to the blocking oscillator.

The blocking oscillator is fired by current pulses from either capacitor C3 or C4. The positive output pulses of the blocking oscillator are delivered to pin f as Composite Frame Sync for the Record Electronics.

7.3.3.6 Sync Gate

The purpose of the Sync Gate is to permit frame sync pulses to be generated only when such pulses are anticipated. Sync pulses which are not true sync pulses are sometimes produced by preceding sync separation circuits because of r-f interference. Therefore, if a pulse can be supplied to arrive at a time when frame sync is expected and this pulse keys a gate that follows the frame sync logic circuitry, then the chance of producing false frame sync is greatly reduced. This card is made up of two one-shots, two blocking oscillators, a flip-flop, a dual emitter follower, and a gate. The schematic diagram for the Sync Gate is shown in Fig. A-43.

There are two inputs to the Sync Gate. Keying pulses are delivered to pin a. Sync pulses from a shift register AND gate are delivered to pin Z. Frame sync output is on pin f. The following is a description of a series of events which take place in the Sync Gate circuitry.

The keying pulse from pin a resets the flip-flop composed of transistors Q3 and Q5 and associated components so that the output on the emitter follower composed of transistor Q1 and resistor R2 (TP2) turns on the gate composed of transistor Q12 and resistors R36 and R37.

Next, the anticipated sync pulse appears on pin Z. It is a positive pulse and it is differentiated by capacitor C1, diode CR1, and resistor R1 so that the positive-going portion of the pulse triggers the one-shot composed of transistors Q2 and Q4 and associated components. This one-shot fires blocking oscillator no. 1, composed of transistors Q6 and Q7, and transformer T1 at a time several microseconds after the initial generation of the sync pulse in the Frame Sync Separator. The reason for this delay is that sync pulses generated in the Frame Sync Separator are approximately in time phase with the data sync and that resetting of the pulse sequencers by the output of the Sync Gate (pin f) must occur slightly after triggering by data sync. This delay can be varied between 4 and 25 microseconds by adjusting resistor R3, but the delay is usually on the order of 3 (± 1) microseconds.

The positive-going output pulses of blocking oscillator no. 1 are delivered to the dual emitter follower composed of transistors Q9 and Q11 and associated components. The output level of the dual emitter follower is seen at test point TP1, and is adjusted by means of variable resistor R28 to 10 (± 2.5) volts peak-to-peak.

The gate composed of transistor Q12 and resistors R36 and R37, which was opened by the action of the flip-flop, passes a positive pulse that fires blocking oscillator no. 2, composed of transistors Q13 and Q14 and transformer T2.

The output of blocking oscillator no. 2 is delivered to pin f as frame sync and to one-shot no. 2, composed of transistors Q8 to Q10 and associated components. One-shot no. 2 introduces a delay just long enough to insure that the gate will pass anticipated frame sync pulses. Variable resistor R34 should be adjusted so that the flip-flop closes the gate approximately 3 microseconds after the generation of a frame sync pulse at pin f .

Essentially the Sync Gate is a gate which is keyed "on" by the arrival of a pulse which just precedes the anticipated sync pulse. It is keyed "off" if the anticipated sync pulse passes through the Sync Gate. If no anticipated sync pulse arrives, the Sync Gate remains open until an apparent sync pulse arrives.

7.3.3.7 Frequency Divider

The purpose of the Frequency Divider is to divide the repetition rate, or frequency, of pulses by factors of two, four, or eight. Reset and set inputs are available for each of the three cascaded flip-flops, or binary counters, so that outputs can be phased in any desired manner.

When it is desired to operate pulse sequencers at rates below that of clock, a frequency divider is inserted between the source of clock pulses and a low-speed pulse sequencer. As the low-speed sequencers must sequence at certain times, reset pulses must be properly applied to the flip-flops in use. In the G-A operation, the frequency is divided by four.

All three flip-flop stages and associated output emitter followers in the Frequency Divider are similar. A schematic diagram is shown in Fig. A-44. Special attention should be given the block diagrams because they can best describe the phasing of the output in relation to the Frame Sync Reset pulse from the Sync Gate.

7.3.3.8 Eight-Channel Pulse Sequencer

The purpose of the Eight-Channel Pulse Sequencer is to provide eight channels of pulses in time sequence. Seven flip-flops and eight AND gates are arranged to accomplish this purpose. A schematic diagram is shown in Fig. A-45.

The output pulses of the pulse sequencer are used to key data gates. The trigger pulses determine the rate at which output pulses advance. The reset pulses determine the phase of the output pulses in relation to the no. 1 output pulse.

The AND gates are driven by flip-flop outputs, which are isolated by individual emitter follower stages.

7.3.3.9 Matrix

The purpose of the Matrix is to AND eight pairs of pulses from the Pulse Sequencers to produce eight keying pulses for sample and hold circuits. A schematic diagram is shown in Fig. A-46. The Matrix is composed of 16 emitter followers and eight diode-type AND gates. Because all gates are identical, only the operation of the first AND gate is described.

Positive pulses between the levels of approximately -15 and -5 volts appear on pins j and Z and are coupled through emitter followers composed of transistor Q1, resistor R3, and transistor Q2 and resistor R5, respectively. Outputs of these emitter followers pass to diodes CR1 and CR2. The coincidence of two positive pulses produces a positive pulse at pin k as a keying pulse to the Sample and Hold circuitry.

7.3.3.10 Data Gates

The purpose of the Data Gates is to provide eight data gates which are keyed by the outputs of a series of AND gates. These AND gates are in turn keyed by pulses from pulse sequencers. The Data Gate unit is made up of 12 emitter followers, eight AND gates, and eight data gates. A schematic diagram of this unit is shown in Fig. A-47.

For any one of the AND gates to produce an output pulse, two coincident input pulses must be present. For example, to produce an output from AND gate 3, input pulses must be present at pins j and V. Likewise, for an AND gate 2 output, input pulses must be present at pins j and X.

All AND gates are composed of a single diode and a single resistor and possess two inputs and one output. One input on each AND gate 1 through 4 are tied together and receive input from pin j through the emitter follower composed of transistor Q2 and resistor R3. In a like manner, one input on each AND gate 5 through 8 are tied together and receive input from pin M through the emitter follower composed of transistor Q7 and resistor R9. The other input on each AND gate 1 through 8 receive

inputs from appropriate pins and emitter followers. Outputs of AND gates 1 and 8 are coupled through emitter followers to pins d and K, respectively, as keying pulse outputs. These outputs key individual data gates 1 through 8.

All data gates are identical. Each data gate is composed of an inverting pulse amplifier, a shunt transistor switch, and a series transistor switch. Data gate 1 will serve as an example of circuit operation.

AND gate 1 output pulse rises and falls between -15 and -5 volts. When the voltage is greater than approximately -10 volts, transistor Q21 is turned on. The collector of this transistor, which serves as an inverting pulse amplifier, drops to approximately -10 volts. This voltage turns off transistor Q29 and turns on transistor Q13. Transistor Q29 is the shunt switch and Q13 is the series switch. When the output from the AND gate drops below approximately -10 volts, transistor Q13 turns off and turns on Q29.

Whenever an output from an AND gate appears, the data gate will open and d-c video from the Gate Driver Amplifier will appear. Whenever there is no AND gate output, the data gate output will present a short circuit with respect to ground.

The gated outputs from data gates 1 through 8 are delivered to appropriate pins for delivery to display electronics.

7.3.3.11 Pulse Set

The purpose of the Pulse Set circuit is to convert three sets of input pulses into three sets of output pulses in the proper form to operate the flip-flop circuitry of succeeding pulse sequencers. A schematic diagram is shown in Fig. A-48. The three inputs are the clock square wave from the Data Sync Separator, the square wave from the Frequency Divider, and the subcommutated pulses from the Low-Speed Sequencer. The clock square wave from the Data Sync Separator has a variable delay added. The other two inputs remain essentially undelayed.

The clock square wave input appears on pin M for delivery to the pulse-shaping circuit composed of transistors Q1, Q2, Q3, and associated components. The positive-going portions of the square wave are converted into positive pulses which are fed through capacitor C3 to the one-shot composed of transistors Q4, Q5, Q6, and associated components. Positive one-shot output pulses, which are delayed by an amount determined by an adjustment of resistor R20, appear at the junction of capacitor C7 and resistor R15. This delay is set so that the keying pulses for succeeding sample and hold circuitry arrive at a time which produces minimum crosstalk.

These one-shot pulses fire a blocking oscillator composed of transistors Q7 and Q8, transformer T1, and associated components. Blocking oscillator output pulses are delivered to pin b as data sync.

Input from the 4:1 Frequency Divider appears at pin K for delivery to emitter follower Q9 and associated components. Its output is differentiated by capacitor C11, resistor R26, and diode CR8 so that positive-going portions of the square wave become positive pulses at the junction of capacitor C11, resistor R26, and diode CR8.

The blocking oscillator composed of transistors Q10 and Q11 and transformer T3, and associated components is fired by the pulses from the differentiating circuit. The output of the blocking oscillator is delivered to pin d as trigger pulses to Low-Speed Sequencer.

Subcommutated pulses from the Low-Speed Sequencer appear at pin R for delivery to an emitter follower composed of transistor Q12 and associated components. Positive-going portions of emitter follower output pulses are differentiated by capacitor C17, resistor R34, and diode CR11 and fire the blocking oscillator composed of transistors Q13 and Q14, transformer T2, and associated components. Blocking oscillator pulses are delivered to pin h as trigger pulses to the subcommutated pulse sequencer.

7.3.3.12 Duty Cycle II

The purpose of Duty Cycle II is to provide gate keying pulses with the proper duty factor to be used as ANDing pulses with signals from the sequencers or matrices. The Duty Cycle II is used in record and reproduce modes of operation. A schematic diagram is shown in Fig. A-49.

Positive pulses from the sequencers appear at pin b for delivery to one-shot no. 1 composed of transistors Q1 and Q2 and associated components. The output of one-shot no. 1 goes through an emitter follower compos d of transistor Q3 and resistor R12. One output of the emitter follower turns off transistor Q9 in the flip-flop composed of transistors Q8 and Q9 and associated components. The second output of this emitter follower passes through emitter follower composed of transistor Q4 and resistor R13 to trigger one-shot no. 2 composed of transistors Q5 and Q6 and associated components. The output of one-shot no. 2 passes through emitter follower composed of transistor Q7 and resistor R23 and turns off transistor Q8 of the flip-flop. Between the times that transistors Q8 and Q9 are turned off, the collector of transistor Q8 and the output of emitter follower composed of transistor Q10 and resistor R33 will go positive from approximately -15 volts to approximately -5 volts.

The output of emitter follower Q10 is delivered to pin e as gate keying pulses to the Matrix boards.

The delay of one-shot no. 1 is varied by adjusting variable resistor R7; its output determines the time of the positive rise of the gate keying pulse on pin e. The delay of one-shot no. 2 is varied by adjusting variable resistor R18; its output determines the negative fall of the gate keying pulse on pin e.

7.3.3.13 Data Sync Delay Record

The Data Sync Delay Record circuit delays the clock pulses so that sampling in the Datrac occurs at a time when crosstalk is at a minimum. At this time, the Data Sync

Delay Record delivers a command pulse to the Datrac. A schematic diagram of the Data Sync Delay Record circuit is shown in Fig. A-50.

This circuit is composed of a one-shot which provides variable delay, a blocking oscillator, and an emitter follower.

The input of positive clock pulses from the Data Sync Separator is at pin a. The pulses are delivered through an emitter follower, composed of transistor Q1 and resistor R3, to the one-shot where a suitable delay is added to the clock information. Delays from approximately 4 to 25 microseconds are obtained by adjusting resistor R5. The output of the one-shot is coupled through capacitor C8 to the blocking oscillator.

Positive Datrac command pulses leave the blocking oscillator at pin N.

7.3.3.14 DC Reference Filter

The purpose of the DC Reference Filter is to provide filtered error voltage to the Reference Amplifier whenever there is a tendency for the d-c level of the data pulses to depart from the preset level. A schematic diagram of this circuit is shown in Fig. A-51. It is composed of an AND gate, a zero voltage adjust, a 250-cycle low-pass filter, and a sample and hold circuit made up of a dual emitter follower, a bilateral charging circuit, a keying circuit, and cascaded emitter followers.

The sync level from Channel 9 appears on pin H for delivery to the sample and hold circuit which is described in Paragraph 7.3.4.

The sync level is stretched so that a nonserrated waveform appears at the output of the sample and hold circuit for delivery to the zero-voltage adjust network composed of resistors R18, R19, R20, and R21.

Keying pulses for the sample and hold circuit which coincide with the Channel 9 sync level are produced by the AND gate composed of diodes CR3 and CR4 and resistor R3. The AND gate receives its input from pulse sequencers or matrices on pins d and e.

The zero-voltage adjust network injects a small adjustable reference voltage into the sample and hold output. This reference voltage is adjusted by means of variable resistor R20.

The output of the zero-voltage adjust network is delivered to a 250-cps low-pass filter, where the voltage is smoothed.

The output of the 250-cps low-pass filter is delivered to pin f as an error voltage to the Reference Amplifier.

7.3.4 Sample and Hold Output Circuits

The Sample and Hold circuitry (Fig. 7-17) is used to sequentially sample the demultiplexed series of pulses from the analog data gates in the Demultiplexer and provide a low output impedance to drive the external equipment. Keying signals to control these sample and hold circuits are derived from the binary countdown and matrices in the Demultiplexer.

Data pulses appearing on the various output lines of the data gates are sampled at peak level and the resulting potential is stored in a capacitor until the next data pulse is sampled, at which time the potential on the capacitor rises or falls to the new level. The direct and subcommutated data are treated in a like manner. A set of cascaded emitter followers is driven by the potential of each capacitor so that sufficient current is supplied to drive a 600-ohm load without excessive deterioration of the capacitor potential.

These circuits perform the same function and operate in the same fashion when the Ground Station is in the record or reproduce modes of operation.

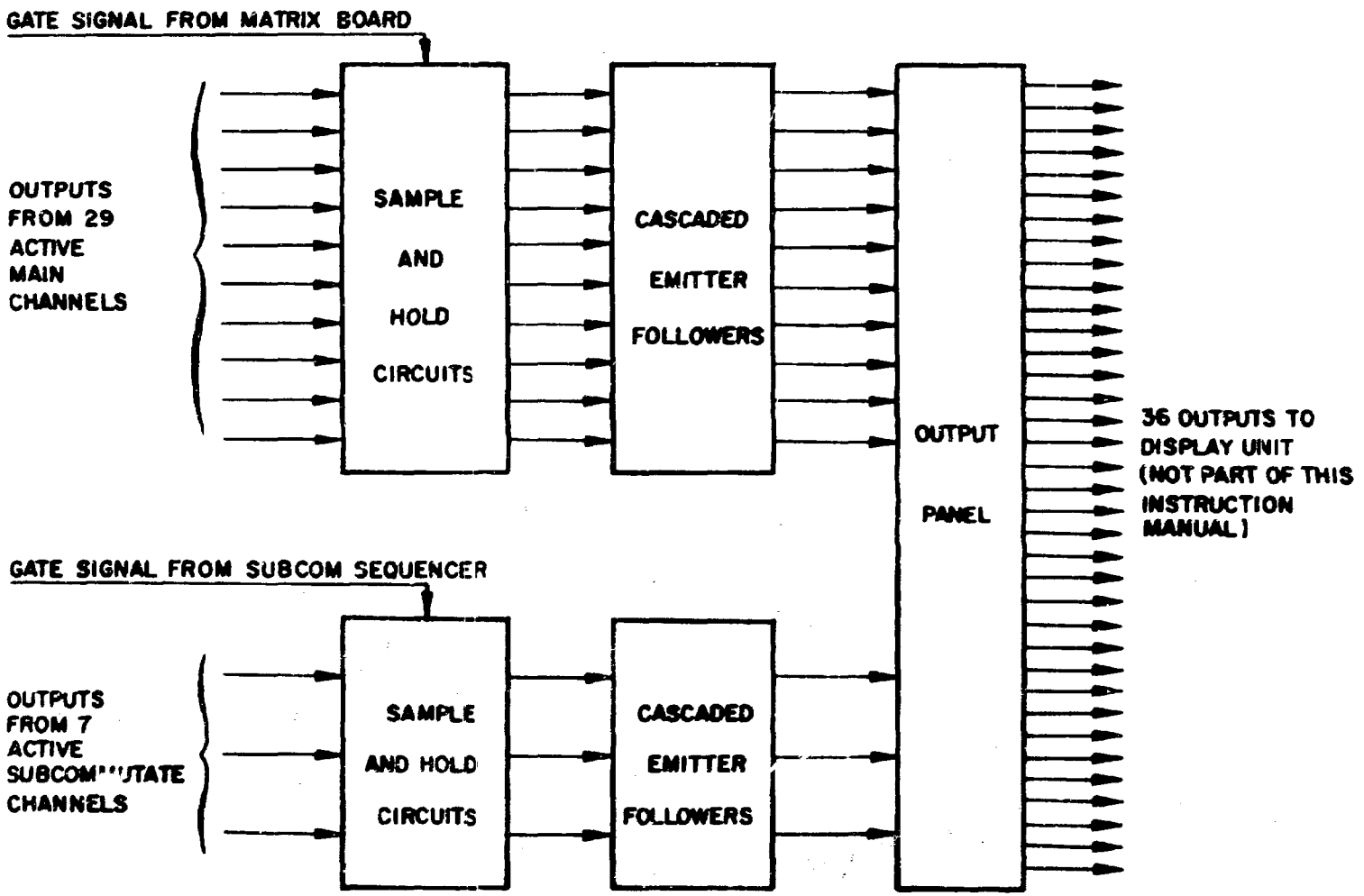


Fig. 7-17 G-A Sample and Hold Output Circuits

7.3.4.1 Sample and Hold

The specific purpose of the Sample and Hold circuit is to sample the data voltage over a brief interval of time and then, through memory, to retain this level until a new sample is made. Upon the arrival of a keying pulse that initiates another sampling, the output of the Sample and Hold changes to the new data level and remains at that level until the next sampling is performed.

Three identical sample and hold circuits are contained on each card. Therefore, only one sample and hold circuit will be discussed. A schematic diagram of the Sample and Hold is shown in Fig. A-52. Each sample and hold circuit is composed of a dual emitter follower, a keying circuit, a bilateral charging circuit, and cascaded emitter followers.

Two states exist in the sample and hold circuit. One is the memory state when output is constant with its level determined by the value of the data during a preceding sampling interval. The other state is the sampling state and is of very short duration when compared with the duration of the memory state. The sampling state exists whenever the level on pin k rises above -10 volts. The memory state exists whenever the level on pin k falls below -10 volts. Keying pulses from the Matrix are positive and between the levels of approximately -15 and -5 volts.

In the sampling state, when voltage on pin k is greater than -10 volts, it turns on transistor Q3. With transistor Q3 turned on, the junction of resistors R4, R6 and R7 goes to approximately -10 volts. This voltage turns off transistors Q4 and Q5. When transistor Q5 is off, the junction of resistors R10 and R11 goes to approximately +20 volts and transistor Q6 is turned off. With transistors Q4 and Q6 off, the data input from pin h is permitted to flow through an emitter follower composed of transistor Q1 and resistor R1 and transistor Q7 of the bilateral charging circuit and also through emitter follower transistor Q2 and resistor R3, and transistor Q8 of the bilateral charging circuit. If the initial charge voltage on capacitor C1 is less than

the data voltage on the base of transistor Q7, current will flow through resistor R12 and transistor Q7 until the voltage on capacitor C1 is approximately equal to the base voltage of transistor Q7. If, on the other hand, the charge voltage on capacitor C1 is greater than the data voltage on transistor Q8, current will flow from capacitor C1 through transistor Q8 and resistor R13 until the voltage on capacitor C1 is approximately equal to the base voltage of transistor Q8.

In storage state, when the voltage on pin k is less than approximately -10 volts, transistor Q3 is turned off. With transistor Q3 off, the junction of resistors R4, R6, and R7 goes positive and transistors Q4 and Q5 are turned on. When transistor Q5 is turned on, the junction of resistors R10 and R11 falls to 0 volts and turns transistor Q6 on. With transistor Q4 and Q6 on, the base of transistor Q7 drops to approximately -7 volts and the base of transistor Q8 rises to approximately +10 volts. Transistors Q7 and Q8 are now turned off and transistors Q1 and Q2 emitter-to-base junctions are back-biased provided that the data on pin h does not exceed the limits of approximately +7 and -5 volts. Effectively, the charge voltage on capacitor C1 is now isolated from the effects of discharge resistance.

Output is taken through cascaded emitter followers composed of transistors Q9, Q10, and Q11, and resistors R14 and R43 and delivered to pin T as Sample and Hold output to the display unit.

Complimentary type circuitry, used for the dual emitter followers and the bilateral charging circuits, provide low input to output voltage drops and high charging currents to the holding capacitor C1. The value of capacitor C1 is laboratory selected to best match the holding interval required of the application.

7.3.4.2 Plus/Minus 10-Volt Regulator

The purpose of the Plus/Minus 10-Volt Regulator is to provide +10 and -10 volts at approximately 5 amperes maximum to the Sample and Hold circuitry. Two 50-watt Zener diodes and appropriate heat sinks are required for each board. A schematic diagram is shown in Fig. A-53.

7.3.5 Analog-to-Digital Converter

The Analog-to-Digital Converter (Datrac) converts every pulse of the PAM composite pulse train into a nine-bit digital word.

Included in the Analog-to-Digital Converter is a sample and hold circuit that samples the peak value of every pulse and holds it for digitization. This circuit, which is controlled by the data sync pulses from the Demultiplexer, is turned on for approximately 2 microseconds by the data sync pulse and holds for approximately 23 microseconds. After a short stabilizing interval, the converter operates at a rate of 2 microseconds per bit and converts the sample and hold signal into a nine-bit digital word in 18 microseconds. These nine bits are temporarily stored and applied to the Digital Record Electronics.

The theory of operation and maintenance procedures for the Datrac are described in detail in the instruction manual Datrac Analog-to-Digital Converter published by Epsco, Inc., Boston, Mass. Modifications made in the Datrac are described in this manual. Schematic diagrams of the modifications are shown in Figs. A-20, A-21, A-22, A-23, and A-24.

In performing the function of recording and reproducing information for the PAM-FM Ground Station, it is necessary to convert analog information into digital form for recording and to convert digital information into analog form for reproduction. The conversion process is accomplished by a device supplied by Epsco, Inc., under the trade name of Datrac. The model supplied for use in the Ground Station is the B-609SM2, modified for the special requirements of the Ground Station. The Datrac B609SM2 (a modified version of Model B-611) is documented in an instruction manual for the Datrac Analog-to-Digital Converter, Models B-611 and B-613. The purpose here is to document those modifications made to the B-611 and the B609SM2 for use in the PAM-FM Ground Station.

The modifications include:

- Addition of special high-speed sample and hold circuitry
- Addition of relays for converting between digital-to-analog and analog-to-digital modes
- Increase in gain of analog output circuitry so that input and output level (±10 volts) is the same
- Reduction of noise during digital-to-analog operation
- Removal of first and second bits of the 11-bit total
- Addition of monitor points to all outputs to Record Amplifiers
- Addition of separate output connectors for the following signals:
  (1) Datrac command
  (2) Conversion complete
  (3) Serial pulse train
  (4) Analog output

A brief description of the two modes of operation of the modified Datrac will be included here.

In the analog-to-digital mode of operation, the first event to occur is the arrival of a Datrac Command pulse. This pulse does three things: (1) starts the sampling process by operating the sample and hold switch-driver circuitry, (2) starts the digitization process which actually begins with the third of 11 bits approximately 6 microseconds later, and (3) clears all digital data from the previous conversion. Bits 1 and 2 have been removed from the 11-bit converter in order to give nine-bit information and to allow stabilization of the sample and hold circuitry and the amplifier following the sample and hold. The sampling interval begins with the arrival of the Datrac command pulse and lasts approximately 1.5 microseconds. The memory of the sample and hold circuitry then holds data voltage for approximately 23.0 microseconds, at which time digitization is complete and a conversion complete pulse (used to clock data on to the magnetic tape) is produced. Digitization of nine bits, beginning with the third and ending with the eleventh, is performed at the rate of one bit for every 2 microseconds.

In the digital-to-analog mode of operation, conversion is completed in only 6 microseconds. In this process, the first event to occur is the arrival of a clear pulse from the Delay Command Pulse circuit contained in the Digital Record and Reproduce Electronics. The next event to occur is the application, in parallel, of nine bits of digital data from the Data Storage and Gate circuits. As the last event, approximately 2 microseconds later, analog data appears for delivery to the Demultiplexer.

Figure 7-10 illustrates the analog-to-digital conversion sequence. The externally applied command pulse initiates digitization and sampling and the timing of the digitization of nine individual bits of information. Completion of the conversion is marked by a conversion-complete pulse after a total elapsed time of approximately 34.5 microseconds.

The individual conversions necessary to make the Datrac B-611 compatible with the PAM-FM Ground Station are discussed in the following paragraphs.

In order to record the value of data pulses with a minimum of crosstalk, this data must be sampled in as short a time as possible. The special high-speed sample and hold circuitry samples in only 1.5 microseconds and holds data value for as long a time as is necessary to perform digitization, i.e., for 24.5 microseconds. The sample and hold equipment is contained on two plug-in chassis. Chassis no. 1 contains an input amplifier composed of an operational amplifier and associated network. Chassis no. 2 contains a blocking oscillator, a switch driver, a switch, a holding capacitor, a bias current source, and an operational amplifier and associated network.

Analog voltage from the Base Band Unit appears on terminal 32 of Chassis no. 1 (Fig. A-20) for delivery to the operational amplifier and network composed of resistors R1, R2, R3, R4, R6, and R7. The operational amplifier is composed of one-half of vacuum tube V3, vacuum tubes V1 and V2, and associated components. The gain of this combination of operational amplifier and network is -1 as the ratio

of R_2/R_1 is unity. Its output is delivered to the cathode follower composed of one-half of vacuum tube V3 and associated components. The output of this cathode follower is delivered to terminal 24 and then to terminal 14 on Chassis no. 2 as input to a diode switch composed of vacuum tubes V4 and V5. The overall gain from terminal 32 to terminal 24 on Chassis no. 1 is approximately 0.85. The output at terminal 24 is between approximately +15 and -5 volts.

Datrac command pulses from Chassis no. 8 appear on terminal 12 of Chassis no. 2 for delivery to a blocking oscillator composed of vacuum tube V6, transformer T1, and associated components. These Datrac command pulses of +20 volts amplitude override the -15-volt bias on grid 2 of V6 and force current to flow from cathode 3 of V6 through capacitor C6 to produce positive voltage on grid 7 of V6. Current, now flowing through transformer T1 to plate 9 of V6, induces voltage across resistor R66, further increasing the positive voltage on grid 7 of V6. The right half of vacuum tube V6 conducts until the charge on capacitor C6 drops enough to return the tube to the cutoff state.

The resulting blocking oscillator pulse is delivered to transformer T2 of the switch-driver circuitry which is composed of transformer T2 and vacuum tubes V7, V8, and V9. Transformer T2 provides positive and negative pulses. The positive pulse is delivered to a cathode follower composed of vacuum tube V8 and resistor R32, and the negative pulse is delivered to a cathode follower composed of vacuum tube V7 and resistor R33. The network composed of resistors R34 and R35 and capacitor C7 provides approximately +37 volts of bias to vacuum tube V7. The network composed of resistors R36 and R37 and capacitor C8 provides approximately -30 volts of bias to vacuum tube V8.

If no pulses are being delivered to the switch-driver circuitry, sufficient current flows through resistor R20, diode vacuum tube V9, and cathode follower V8 to produce

approximately -20 volts on the plates of vacuum tubes V4 and V5 of the diode switch. Likewise, sufficient current flows from cathode follower V7 and diode V9 and through resistor R39 to produce approximately +40 volts on the cathodes of V4 and V5 of the diode switch. Under these conditions, diodes V4 and V5 are nonconducting and holding capacitor C9 is effectively tied to the open grid 7 of vacuum tube V10.

When pulses are delivered to the switch-driver from the blocking oscillator, bias voltages for V7 and V8 are overridden so that the currents in both halves of diode V9 are interrupted for the duration of the sampling interval, i.e., for approximately 1.5 microseconds. This means that current flows from +300 volts at terminal 2 through resistor R38, both halves of diodes V4 and V5, and through resistor R39 to -300 volts on terminal 3. With the diode bridge conducting, data from Chassis no. 1 permits supply current to charge holding capacitor C9 to data level.

The voltage level which appears on holding capacitor C9 is delivered to the open grid 7 of vacuum tube V10 of the operational amplifier composed of vacuum tubes V10, V11, and V12, and associated components. Gain of this combination of operational amplifier and the network composed of resistors R61, R62, and R63 is adjusted by varying R63. Overall gain is adjusted to approximately 3.0. The sampled output is delivered to terminal 25 of Chassis no. 2 as the input voltage to the Datrac summing junction.

7.3.6 Digital Record Electronics

Digital Record Electronics (Fig. 7-11) are used to record the digital word generated by the Datrac, the composite frame sync, and the clock signal in parallel in Non-Return-to-Zero (NRZ) form on the magnetic tape on command of the conversion-complete pulse from the Datrac.

The conversion-complete pulse occurs approximately 0.5 microseconds after the digitization is complete. This pulse is amplified and delivered as a clock signal to all digital record amplifiers. This signal is also recorded on one of the digital tracks as the clock signal. In addition, it is used to reset the frame sync storage circuit.

Composite frame sync is applied to the frame sync storage circuit which, in turn, applies a "one" to the Digital Record Amplifier. The occurrence of a conversion-complete pulse will clock this information onto the tape from the Digital Record Amplifier and also reset the frame sync storage circuit to the "zero" state; thus, succeeding conversion-complete pulses do not change the magnetization of the tape until a new composite frame sync pulse resets the frame sync storage to the "one" state.

The binary bits from the Datrac are applied and held to the appropriate Digital Record Amplifier. The conversion-complete pulse interrogates these inputs and causes a change in the state of the magnetization of the tape if a "one" is presented to a Digital Record Amplifier and no change in state if a "zero" is presented. Thus, the binary word from the Datrac, the composite frame sync, and the clock signal are all recorded on digital tracks in parallel by the occurrence of a conversion-complete pulse.

7.3.6.1 Frame Sync Storage Record

The purpose of the Frame Sync Storage Record is to convert composite frame sync pulses from the Demultiplexer to pulses that will be accepted by the Frame Sync

Digital Record Amplifier. It should be remembered that information is recorded when the input to a Digital Record Amplifier is more negative than the negative threshold level and a record pulse is received. Both of these conditions must be met for recording to be accomplished. The Frame Sync Storage Record is made up of an inverting pulse amplifier and a flip-flop. A schematic diagram of the Frame Sync Storage Record card is shown in Fig. A-23.

Positive composite frame sync pulses from the Demultiplexer appear at pin Z for delivery to the inverting pulse amplifier composed of transistor Q1 and associated components.

The negative-going leading edge of the output of the inverting pulse amplifier, which is in time phase with the positive-going leading edge of the pulses at pin Z, is coupled through capacitor C2 to turn off transistor Q3 of the flip-flop composed of transistors Q3 and Q4 and associated components. This action causes the collector of transistor Q4 to go negative as well as the output of emitter follower Q5, which is delivered to pin K as output to the Frame Sync Digital Record Amplifier.

Positive record pulses from the Pulse Amplifier appear at pin T for delivery to the emitter follower composed of transistor Q2 and resistors R4 and R5. Emitter follower output is differentiated by a network composed of capacitor C4, diode CR4, and resistor R17 so that the negative-going trailing edge of a pulse on pin T turns off transistor Q4 of the flip-flop. The collector of transistor Q4 now goes positive, as does the output on pin K. The delay of approximately 1 microsecond between the positive-going leading edge of the record pulses, which clock out data from the Digital Record Amplifiers, and the negative-going trailing edge of the record pulse, which resets the flip-flop, is necessary because data must be recorded before composite frame sync information is removed from the Frame Sync Digital Record Amplifier input.

7.3.6.2 Pulse Amplifier

The purpose of the Pulse Amplifier is to convert conversion-complete pulses from the Datrac to a form suitable for clocking out the data from the Digital Record Amplifiers.

It is made up of an inverting pulse amplifier and a blocking oscillator. A schematic diagram of the Pulse Amplifier is shown in Fig. A-26. A conversion-complete pulse from the Datrac appears at pin M, where it enters the inverting pulse amplifier composed of transistor Q1 and associated components. The negative-going leading edge of the inverting pulse amplifier output, which is in time phase with the positive-going leading edge of the input pulse on pin M, is coupled through capacitor C2 to fire the blocking oscillator composed of transistors Q2 and Q3 and transformer T1. Positive-going output pulses are delivered to pin T as record pulses to the Digital Record Amplifiers.

7.3.6.3 Digital Record Amplifier

The purpose of the Digital Record Amplifier is to accept digital "ones" from the Datrac and clock this information onto the magnetic tape in NRZ form in phase with the record pulses from the Pulse Amplifier. There is one Digital Record Amplifier for each digital recording track. This circuit also provides sufficient power to operate the recording heads. It is made up of an inverting pulse amplifier, a flip-flop, two AND gates, and amplifiers and complementary emitter followers. A schematic diagram of a Digital Record Amplifier card is shown in Fig. A-27.

Digital information appears at pin K in the form of rising and falling levels and is delivered to the inverting pulse amplifier composed of transistors Q1, Q2, and Q3, diode CR1, and associated components. The operation of this inverting pulse amplifier is such that, for levels greater than approximately -11 volts, its output is approximately 0 volts. For levels less than approximately -11 volts, its output is approximately +20 volts.

The output of the inverting pulse amplifier, which is the emitter of transistor Q3, is delivered to two emitter followers, one being transistor Q4 and resistor R13, the other being transistor Q9 and resistor R24. The outouts of each emitter follower are each ANDed with record pulses from the Pulse Amplifier, which appear at pin T. These AND gates are composed of diodes CR3, CR4, and CR7, and diodes CR5, CR9, and CR8.

The action of these AND gates causes the flip-flop composed of transistors Q6 and Q7 and associated components to change state whenever a binary "one" and a record pulse are present at the same time. A binary "one" is an input level on pin K of less than -11 volts.

A complementary emitter follower is coupled to each side of the flip-flop through a pulse amplifier. The collector of flip-flop transistor Q6 is associated with the pulse amplifier composed of transistors Q5 and Q14 and associated components and a complementary emitter follower composed of transistors Q11 and Q13. The collector of flip-flop transistor Q7 is associated with the pulse amplifier composed of transistors Q8 and Q15 and associated components and with the complementary emitter follower composed of transistors Q10 and Q12.

The output levels of the complementary emitter followers are out of phase and vary between approximately 0 and +10 volts. Resistor R31 serves to limit magnetic tape recorder head current to approximately 100 ma at all times. The output to the Magnetic Tape Recorder head is between pins a and c. An output monitor point of the head current is available at pin h.

7.3.7 Magnetic Tape Recorder

The Magnetic Tape Recorder is a special Ampex unit (FR-1100) that will accept 19-inch or smaller reels of magnetic tape. It is designed to permit the recording of 11 tracks of digital data and four tracks of analog data on one-inch wide tape. Nine of the digital tracks are used to record the digital words from the Datrac. The remaining two digital tracks are used to record the data sync pulse and the composite frame sync pulse. The four analog tracks are used to record video, field strength, voice comment, and system time signals. Normal operating speed of the recorder is 50 ips for G-A data.

Distribution of tracks and the recording function for each track is as follows:

TRACK	RECORDING FUNCTION
Digital	
1	Bit 9
2	Bit 1
3	Bit 2
4	Bit 3
5	Bit 4
6	Data Sync
7	Bit 5
8	Bit 6
9	Bit 7
10	t 8
11	Composite Frame Sync
Analog	
11	Video Backup
12	System Time
13	Spare (Range Time at AMR)
14	Signal Strength and Voice

The theory of operation of the Magnetic Tape Recorder and the procedures for its maintenance are described in detail in the instruction handbook Series FR-1100 Recorder/Reproducer – Magnetic Tape Recorders for Instrumentation, Ampex Corp., Redwood City, Calif., 1 Jul 1958. Special instructions for using this recorder with the PAM-FM Ground Station are included in appropriate paragraphs in this manual.

7.3.8 Digital Reproduce Electronics

The G-A Ground Station in the reproduce mode of operation is illustrated in Fig. 7-4.

The Digital Reproduce Electronics (Fig. 7-12) amplifies the digital signals from the magnetic tape and temporarily stores and clocks the digital information into the Datrac. Clock pulses are delivered to the Datrac in the form of a clear pulse and are used to reset the Datrac to a state corresponding to all zero inputs. Clock pulses and the composite frame sync pulse are also delivered to the Demultiplexer.

Binary "ones" from the magnetic tape are amplified in the Digital Reproduce Amplifiers. These binary "ones," which represent the digital word and the composite frame sync, are used to set the storage circuits to the "one" state. Since no change of state is recorded on the magnetic tape for a binary "zero," no signal is produced for a "zero." The binary "ones," which represent the clock signal from the Digital Reproduce Amplifier, are delivered through a delay circuit to the storage circuits where they clock out the stored information in the storage circuits and reset the storage circuits to the "zero" state. Thus, binary "ones" representing digital information are clocked in parallel into the Datrac for conversion to analog form. The effects of any static head skew and dynamic "jitter" of the tape are reduced during this process. Binary "ones" representing composite frame sync are clocked into the Demultiplexer.

The delay circuit has three outputs, each output occurring 1.5 microseconds after the other. However, the initial output is delayed a suitable time to enable it to be used as a clock signal, but not so long that it becomes a part of the succeeding binary word. The first output is the clear pulse that is used to clear the Datrac. The second output, occurring 1.5 microseconds later, is used as a clock pulse to the Demultiplexer. The last output is used as the command pulse to the storage circuits.

7.3.8.1 Digital Reproduce Amplifier

The purpose of the Digital Reproduce Amplifier is to amplify the data from the digital reproduce heads of the Magnetic Tape Recorder and to produce appropriate data pulses for the Data Storage and Gate circuitry which follows. A schematic diagram of the Digital Reproduce Amplifier is shown in Fig. A-28.

The Digital Reproduce Amplifier contains a high-gain, four-stage, R-C coupled linear amplifier; a linear phase splitter; a full-wave rectifier; and an inverting pulse amplifier. Linear circuitry is used until the data can be brought up to a voltage level that is acceptable for pulse-type amplification. This is done so that the possibility of false generation of output pulses by noise is reduced to a minimum. A variable gain feature is included so that operation with various tape speeds is possible.

Data from the Magnetic Tape Recorder reproduce heads appears at pin L for delivery to the amplifier composed of transistors Q1 through Q5 and associated components. This amplifier contains four common-emitter stages in cascade and an emitter follower output stage. A constant output level is maintained for various tape speeds by varying the gain. Gain is varied by the application of appropriate values of resistance across pins V and T. The resistances for this function are selected by means of the TAPE SPEED COMPENSATION switch located on the Record and Reproduce Monitor Panel. Gain can also be varied by adjusting variable resistor R19. Amplifier gain should be such that for any tape speed, output is 9 (±0.5) volts peak-to-peak.

The output of this amplifier is delivered to the phase splitter composed of transistor Q10 and resistors R10 and R43. Here, by adjusting variable resistor R43, two outputs of equal magnitude and 180 degrees out of phase with respect to each other are fed to separate diodes CR2 and CR3 of the full-wave rectifier. This rectifier changes the positive and negative pulses of the phase splitter to a series of positive pulses. These positive pulses are held between the levels of approximately 0 and +3 volts.

One of the phase-splitter signals is transmitted through the emitter follower composed of transistor Q9 and resistor R38 for delivery to one side of the full-wave rectifier. The other phase-splitter signal, which appears on the emitter of transistor Q10, is transmitted directly to the full-wave rectifier.

The full-wave rectifier output pulses are delivered to the inverting pulse amplifier at the base of the emitter follower composed of transistor Q7 and resistor R32. Whenever the emitter follower output goes positive, transistor Q8 is turned on and its collector goes to ground potential. Whenever the emitter follower output reaches zero, or is negative, transistor Q8 is turned off and its collector goes to approximately +13 volts. The signal which appears at the collector of Q8 is coupled through the emitter follower composed of transistor Q6 and resistor R30 for delivery to pin a as output to Data Storage and Gate.

Operation of the Digital Reproduce Amplifier is such that a negative-going output pulse is generated whenever a data pulse appears across the input terminals.

7.3.8.2 Data Storage and Gate

The purpose of the Data Storage and Gate card is to hold the digital information received from the Digital Reproduce Amplifier until all bits of information have been read out of the Magnetic Tape Recorder. This delay is necessary to compensate for skew and flutter in the Magnetic Tape Recorder. A command pulse clocks these bits into the Datrac for conversion to analog voltage. Each Data Storage and Gate card can accommodate two bits of information. A schematic diagram of this unit is shown in Fig. A-29.

Two separate but identical circuits are present on each card; each circuit stores one bit of information until the command pulse transmits it to the following circuit. Each circuit is made up of a blocking oscillator, a flip-flop, and an inverting pulse amplifier. Since all circuits are identical, only the operation of one circuit will be described.

Digital data from the Reproduce Amplifier appears at pin K for delivery to the inverting pulse amplifier composed of transistor Q1 and diode CR1 and associated components.

If the level at pin K falls below approximately +9 volts, transistor Q1 is turned on, the collector of Q1 goes to approximately +9 volts, and a positive-going pulse appears at the junction of capacitor C3 and resistor R8. This positive pulse is then coupled through capacitor C4 so that it turns off transistor Q2 of the flip-flop composed of transistors Q2 and Q3 and associated components.

When a command pulse from Delay Command Pulse appears on pin T, transistor Q3 of the flip-flop will be turned off. This change of state of the flip-flop causes the collector of transistor Q2 to go positive. The signal on the collector of transistor Q2 is coupled through the emitter follower composed of transistor Q4 and resistor R18 for delivery to the blocking oscillator composed of transistors Q5 and Q6, transformer T1 and associated components.

If the level on pin K rises above approximately +9 volts, no pulse will be delivered to the flip-flop and, consequently, no pulse will be available to fire the blocking oscillator upon the arrival of a command pulse.

7.3.8.3 Data Sync Delay Reproduce

The purpose of the Data Sync Delay Reproduce is to delay the pulses from the Data Sync Digital Reproduce Amplifier sufficiently so that all information delivered from the Digital Reproduce Amplifiers to the Data Storage and Gate gates has had time to arrive before being clocked out of the Data Storage and Gate gates into the Datrac. It is made up of an inverting pulse amplifier and a one-shot. A schematic of the Data Sync Delay Reproduce card is in Fig. A-30.

Negative-going pulses from the Data Sync Digital Reproduce Amplifier appear at pin a. These pulses are delivered to the inverter pulse amplifier composed of transistors Q1 and Q2 and associated components.

Positive-going pulses are coupled through capacitor C1 to the one-shot composed of transistors Q3 and Q4. This one-shot is triggered by the negative-going leading edge

of the pulses at pin a. The one-shot output is fed through the emitter follower composed of transistor Q5 and resistor R15 and delivered to pin N as output to the Delay Command Pulse.

A variable delay of from approximately 4 to 25 microseconds is obtained by adjusting variable resistor R8. Its setting is adjusted so that the outputs from the following circuit, the Delay Command Pulse, properly clock out the data contained in the Data Storage and Gate circuits.

7.3.8.4 Delay Command Pulse

The purpose of the Delay Command Pulse circuit is to provide clear pulses to the Datrac, data sync to the Demultiplexer, and command pulses for the Data storage and Gate cards during the reproduce mode of operation. Delays of approximately 2 microseconds separate each of these pulses so that no interference can exist while generating video, frame sync, and data sync. A schematic diagram of the Delay Command Pulse circuit is shown in Fig. A-3[1].

Pulses from the Data Sync Delay Reproduce enter at pin N and trigger the blocking oscillator composed of transistors Q1 and Q2, transformer T1, and associated components. The positive-going portion of these pulses triggers this blocking oscillator. Output (which is essentially undelayed) leaves this blocking oscillator on pin f for delivery to Datrac as the clear pulse. This output pulse, which is approximately 2 microseconds wide, also passes into the delay and blocking oscillator. The negative-going portions of these pulses are extracted by capacitor C6, resistor R10, and diode CR3 and fire the blocking oscillator composed of transistors Q4 and Q5, transformer T2, and associated components. Output from this oscillator is then delivered to pin Z as data sync for delivery to the Demultiplexer. Output from this blocking oscillator is also fed into a second delay and blocking oscillator circuit. Again, the negative-going portions of the 2-microsecond pulses are extracted by capacitor C9, resistor R18, and diode CR5 and fire the blocking oscillator composed of transistors Q7 and Q8, transformer T3, and associated components. Output is delivered to pin T as a command pulse to the storage cards.

Monitor points for the no. 1 and no. 3 outputs are at pins f and T, respectively.

7.3.9 Digital-to-Analog Converter

The Digital-to-Analog Converter is the same converter (Datrac) that is used for analog-to-digital conversion, but operated in the digital-to-analog mode.

The Digital-to-Analog Converter accepts the nine-bit digital words from the Digital Reproduce Electronics and reconstructs the analog PAM composite pulse train. This composite pulse train is then delivered to the Gate Driver Amplifier of the Base Band Unit, which in turn delivers it to the Demultiplexer.

7.3.10 Base Band Unit, Reproduce Mode

In the Reproduce Mode of operation, only the Gate Driver Amplifier and the Reference Amplifier portions of the Base Band Unit (Fig. 7-18) are used.

Input to the Reference Amplifier is from the DC Reference Fliter in the Demultiplexer. The Reference Amplifier output in the form of a d-c reference correction voltage is delivered by way of jack J16 to grid 7 of vacuum tube V1 in the Gate Driver Amplifier. The Reference Amplifier functions in the same manner in the reproduce mode as it does in the record mode.

The output of the Digital-to-Analog Converter in the form of an analog PAM composite pulse train provides the second input (at jack J14) to the Gate Driver Amplifier. The output of the Gate Driver Amplifier is delivered to jack J17 as d-c video to the Demultiplexer. Except for the changes in input, the Gate Driver Amplifier functions in the same fashion in the reproduce mode as it does in the record mode.

7.3.11 Demultiplexer, Reproduce Mode

Although the Demultiplexer in the reproduce mode (Fig. 7-19) functions in much the same way as it does in the record mode, inputs are from different sources and a

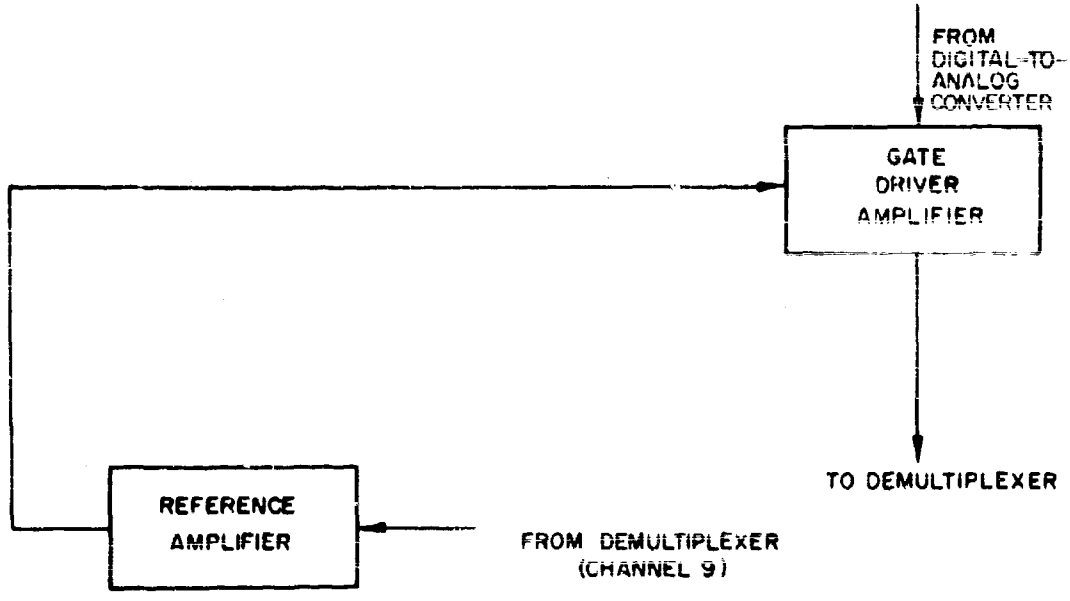


Fig. 7-18 G-A Base Band Unit, Reproduce Mode

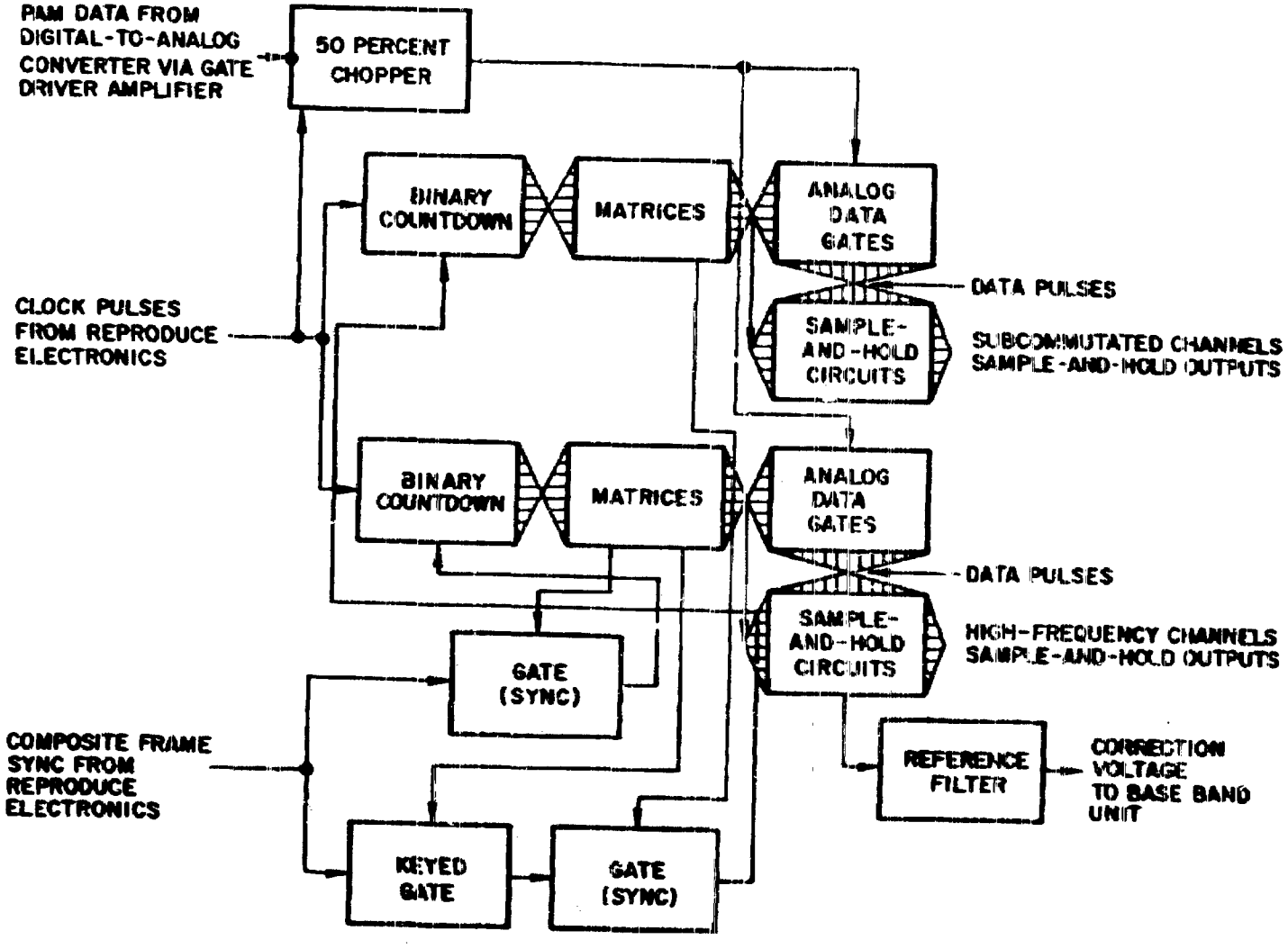


Fig. 7-19 Functional Diagram of G-A Demultiplexer, Reproduce Mode

part of the synchronization logic is not used. Since clock pulses and composite frame sync pulses have been recorded, there is no need for a data sync generator, frame sync generator, or a shift register.

7.3.11.1 Frame Sync Delay Reproduce

One additional circuit is used in the reproduce mode of operation. Frame Sync Delay Reproduce is a delay network to delay the composite frame sync from the data sync pulses by approximately 5 to 10 microseconds. The composite frame sync pulse is also transformed to the correct impedance and amplitude for driving the Demultiplexer. A schematic diagram of the Frame Sync Delay Reproduce is shown in Fig. A-54. Since this circuit was developed from the sync gate, the flip-flop and one-shot no. 2 as shown in the schematic are not used.

Composite frame sync pulses from the Digital Reproduce Electronics appear on pin Z. This positive pulse is differentiated by capacitor C1, diode CR1, and resistor R1 so that the positive-going portion of the pulses triggers the one-shot composed of transistors Q2 and Q4 and associated components. This one-shot fires blocking oscillator no. 1 composed of transistors Q6 and Q7, transformer T1, and associated components at a time several microseconds after the initial arrival of the composite frame sync pulse. This delay can be varied between 4 and 20 microseconds by adjusting resistor R3, but the delay is usually from 5 to 10 microseconds.

The positive-going output pulses of blocking oscillator no. 1 are delivered to dual emitter follower composed of transistors Q9 and Q11 and associated components. The output level of the dual emitter follower is seen at test point TP1 and is adjusted by variable resistor R28 to 10 ($\pm$ 2.5) volts peak-to-peak.

The gate composed of transistor Q12 and resistors R36 and R37, which is normally open, passes a positive pulse that fires blocking oscillator no. 2 composed of transistors Q13 and Q14, transformer T2, and associated components. The output of blocking oscillator no. 2 is delivered to pin f as the delayed composite frame sync to be delivered to pin z of the Sync Gate and to pin P of the Sync Selector.

7.3.12 Power Supply Interlock

The basic purpose of the Power Supply Interlock is to prohibit the application of power to any of the components of the PAM-FM Ground Station unless power from all four of the power supplies is present simultaneously. Other functions of this unit are: (1) to provide a time delay between the application of heater power and plate voltage to the Base Band Unit; (2) to provide a means of distributing power to units; and (3) to route various record/reproduce, Magnetic Tape Recorder interlock, and G-A/ Vibration relay signals between major components in the Ground Station.

The Power Supply Interlock is composed of 15 relays (two of which are one-minute, thermal-delay relays), a 115-volt-ac isolation transformer which provides power for the 115-volt relays, and various connectors.

Special attention should be given the schematic diagram shown in Fig. A-34 as all controlling signals, their origins and destinations, and the routes of incoming and outgoing power cables are clearly labeled.

7.3.13 Test Signal Generator

The purpose of the Test Signal Generator is to furnish a test signal for the VHF telemetry receiver when the Ground Station is being readied for use. A schematic diagram is shown in Fig. A-55. It is composed of two 28-volt power supplies, a multiplexer, a VHF/FM transmitter, a transmitter termination and receiver coupling device, and a calibrator.

The two 28-volt power supplies (Hewlett Packard 721A) are connected to the calibrator as shown in Fig. A-34. The multiplexer and transmitter, similar to the vehicle equipment, are sealed units and are connected as shown in the schematic diagram. Power for the transmitter is obtained from the +300-volt Lambda power supply by way of the Power Supply Interlock.

The transmitter termination and receiver coupling device, when used with an external attenuator, provides approximately 1000 microvolts of signal across the antenna terminals of the Nems-Clarke 1412 Receiver. This device properly terminates the r-f output of the transmitter.

The calibrator provides test voltages to modulate various inputs of the multiplexer. Ground level, +5 volts, +2.5 volts, or externally applied modulation may be selected as calibrator output. Two preset reference voltages are produced by a network composed of diode CR1, and resistors, R1, R2, and R3. These two voltages are coupled through the emitter follower composed of transistor Q1 and resistor R6 for delivery to the selector switch S1. Selector switch S1 selects either of these two voltages, as well as ground potential and external modulation, as output to the multiplexer patch panel.

Any type of external modulation may be applied to the test signal generator provided it does not exceed the limits of +5 volts and 0 volts with respect to ground. Filaments of the transmitter must be on for at least one minute before plate voltage is applied by the transmitter plate voltage switch located on the Test Signal Generator panel.

7.3.14 Relay Board

The purpose of the Relay Board is to make it possible to shift quickly between record and reproduce modes of Ground Station operation. Several circuit rearrangements among the component boards in the Demultiplexer and other units are required when station modes are switched. In the Demultiplexer, several cards with three DPDT relays each provide the necessary switching. For example, switching between the Sync Separators and the Sync Reproduce Electronics, or between the Duty Cycle and the Base Band Unit, are all accomplished with Relay Boards, which are in turn driven by the Record/Reproduce controls of the Monitor Panel. A schematic diagram of the Relay Board is shown in Fig. A-35.

7.3.15 Main Monitor Panel

The functioning of main and sub monitor panels as a means of applying "scope probes" rapidly to critical points in the Ground Station is documented in Volume I and in Section 11 of this volume. It should be pointed out that the main monitor panel also performs, by means of nine DPDT relays, most of the switching necessary to change a Ground Station between G-A and Vibration operation. Also, control signals for POWER ON-OFF, RECORD-REPRODUCE, and G-A-VIBRATION are initiated by a series of push buttons on the Monitor Panel. A schematic diagram of the Monitor Panel is shown in Fig. A-36.

7.3.16 Signal Strength and Voice Record and Reproduce Filters

The purpose of the Signal Strength and Voice Record and Reproduce Filters is to combine the receiver signal strength output and the voice signal for recording with FM record electronics and to separate the two signals on reproduce. This is done with simple passive filters and a resistive adder which limits the frequency response of the recorded signal strength from dc to approximately 100-cps and the voice signal from approximately 300-cps to 10 kc. A schematic diagram is shown in Fig. A-37.

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Section 8
MAINTENANCE

WARNING: The high voltages in this equipment are dangerous. To prevent serious injury or death, use caution while performing maintenance procedures.

8.1 INTRODUCTION

8.1.1 Scope

This section is intended as a guide to the location and correction of a faulty circuit or circuit board. Its usefulness depends upon the ability of the operator to isolate a trouble to a particular circuit by use of the theory discussion in Section 7. If the operator understands the function of the station as a whole, he can, by use of the monitor switches and the rack-mounted oscilloscope, isolate most troubles to a major section and, with the aid of these procedures, to the specific circuitry or printed circuit board that is at fault.

Because the Ground Station is highly complex and field experience is limited, it is difficult to anticipate troubles and give specific, detailed procedures for isolating and repairing them. However, this section does contain a recommended procedure for checking through each circuit for required inputs and outputs at the critical points. The checkpoints are chosen so that the trouble is isolated to a single component or to a small group of components. It is assumed that the operator will then replace the suspected components with others that meet the specifications called out on the drawings and parts lists in the Appendix.

The instructions are supported by a schematic diagram, a component assembly drawing of each printed circuit board, a parts list, and a block diagram that shows the signal flow and the critical waveforms and voltages of the more important portions of the circuit. Before the detailed trouble isolation procedures are performed, it is recommended that certain general procedures be done. These are given in Section 8.2.

The troubleshooting procedures in this section do not contain the details of trouble isolation in blocking oscillators, one-shots, and flip-flops. Each time trouble is isolated to one of these circuits, the procedures in Section 8.4.1, 8.4.2, or 8.4.3 should be followed.

8.1.2 General Information

The following general information is applicable any time maintenance is being performed.

1. Some of the values listed in this section are qualified with the word "approximately." Values that are not so qualified or for which tolerances are given are critical values and must be treated as such.

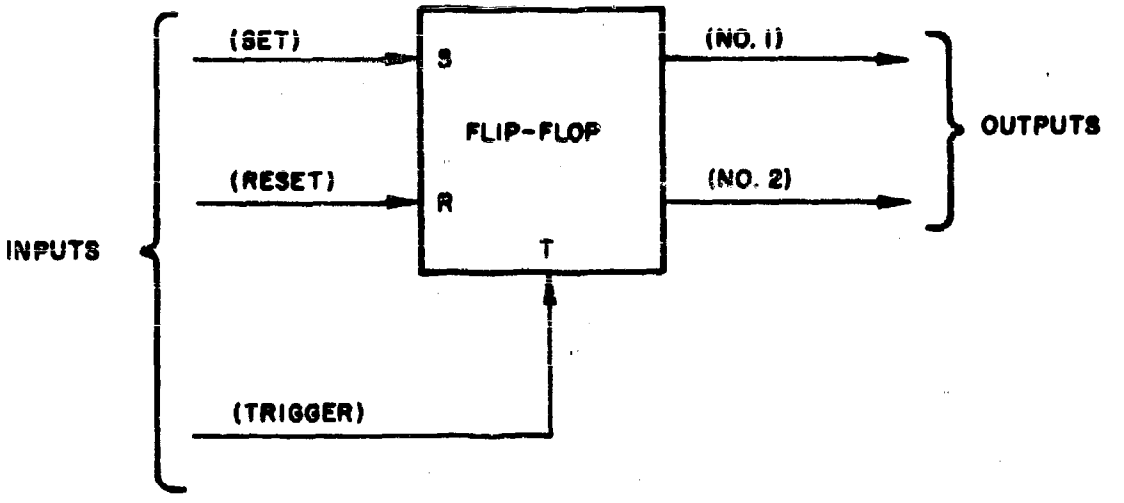
2. Cables that interconnect units are identified by plastic or metal strips that are attached to the individual cables. Wiring information and wiring block diagrams are in Section 10.

3. All variable resistors on the printed circuit boards are at the front, opposite the connector side.

4. The test equipment described in Volume I, Section 2 should be available for maintenance.

5. The following flip-flop convention (Fig. 8-1) is included as an aid to understanding the block diagrams.

6. Maintenance instructions for the Lambda and Harrison power supplies, the Nems-Clarke receiver, the Tektronix oscilloscope and pre-amplifier, the Ampex tape recorder, the E.I. amplifiers, the Datrac, and the Visicorder are contained in manuals published by the manufacturers and supplied with the Ground Station.



NOTES:

1 — ONES ON TRIGGER INPUT MAKE ALTERNATE ONES ON NO. 1 AND NO. 2 OUTPUTS.

2 — ONE ON RESET INPUT MAKES (NO. 1) OUTPUT A ZERO AND (NO. 2) OUTPUT A ONE.

3 — ONE ON SET INPUT MAKES (NO. 1) OUTPUT A ONE AND (NO. 2) OUTPUT A ZERO.

Fig. 8-1 Flip-Flop Convention

7. When removing printed circuit cards from the card racks, use the special card-removing tool and have the power to the rack turned off. When a card is removed during a recording period, the power may be left on if care is taken to prevent shorting components on printed circuit boards. Remove cards carefully and handle them with care so that components, plugs, and printed wiring are not damaged.

8.2 GENERAL INSTRUCTIONS

Before attempting to isolate and repair trouble, the following general procedures should be done.

1. Check that all cables are connected securely.

2. Check that all power supplies are delivering required voltages within ±1 percent, unless otherwise specified.

3. Check that all switches are in the proper positions as given in the Operating Instructions, Volume I.

4. Check that all printed circuit boards required are present and are inserted firmly in their correct slots with correct orientation.

5. In faulty vacuum tube circuits, first check to determine whether the trouble is caused by vacuum tube failure. If a faulty tube is replaced, check other components to determine whether there is a specific cause for the tube failure. All vacuum tube voltages are given with respect to ground.

6. Check wiring continuity, capacitors for shorts, and solder points.

8.3 TROUBLESHOOTING FOR ABSENT OR INCORRECT INPUTS

If one or more of the inputs to a card is absent or incorrect, proceed as follows:

1. Remove card being maintained from its slot.

2. Insert card that precedes (in the circuitry) the one being maintained into a card extension.

NOTE: The cards that precede a card in the circuitry are identified in the schematic and block diagrams.

3. Check outputs of this card that are inputs to the card being maintained. If these outputs are correct, the trouble is in the input circuitry of the card being maintained or in the wiring between. If these outputs are incorrect, the trouble is in this preceding card.

4. If the trouble is in the preceding card, repair it in accordance with the applicable instructions in this section; if the trouble is in the input circuitry of the card being maintained, continue with the maintenance procedures for that card.

5. If the trouble is in the inter-card wiring, check for continuity and connection of wires to proper pins.

8.4 TROUBLESHOOTING BLOCKING OSCILLATORS, ONE-SHOTS, AND FLIP-FLOPS

The troubleshooting procedures in the sections that follow do not contain the details of trouble isolation in blocking oscillators, one-shots, or flip-flops. The following paragraphs, 8.4.1, 8.4.2, and 8.4.3, contain some recommended procedures for isolating trouble in these types of circuits.

8.4.1 Blocking Oscillator

If trouble is isolated to a blocking oscillator, proceed as follows:

1. Visually inspect for component continuity with eyelets and printed circuit traces, and check that components are of the correct type and value. Make any necessary repairs.

2. Check wiring continuity and make necessary repairs.

3. Check that blocking oscillator is getting power.

4. Make sure that circuit is not overloaded.

5. Make sure that there is a proper input to the blocking oscillator.

6. Check transformer continuity by checking appropriate windings of the transformer with an ohmmeter.

7. Replace both transistors.

8. If a Zener diode is used, check it for reference voltage and replace it if necessary.

9. Check diodes and replace any that are faulty.

10. Check bypass capacitor for shorts and replace it if it is faulty.

8.4.2 One-Shot

If trouble is isolated to a one-shot, proceed as follows:

1. Visually inspect for component continuity with eyelets and printed circuit traces, and check that components are of the correct type and value. Make any necessary repairs.

2. Check wiring continuity and make necessary repairs.

3. Check that one-shot is getting power.

4. Make sure that circuit is not overloaded.

5. Make sure that there is a proper input to the one-shot.

6. Check that potentiometer adjustment is making contact.

7. Replace transitors.

8. Replace input diode.

8.4.3 Flip-Flop

If trouble is isolated to a flip-flop, proceed as follows:

1. Visually inspect for component continuity with eyelets and printed circuit traces, and check that components are of the correct type and value. Make any necessary repairs.

2. Check wiring continuity and repair if necessary.

3. Check that flip-flop is getting power.

4. Make sure that circuit is not overloaded.

5. Make sure that there is a proper input to the flip-flop.

6. Replace transistors.

7. Check diodes and replace any that are faulty.

8.5 RECEIVER

For instructions on isolating and repairing trouble in the receiver, refer to the manual of instructions for the Nems-Clarke Model 1412 Telemetry Receiver.

8.6 DC AMPLIFIER

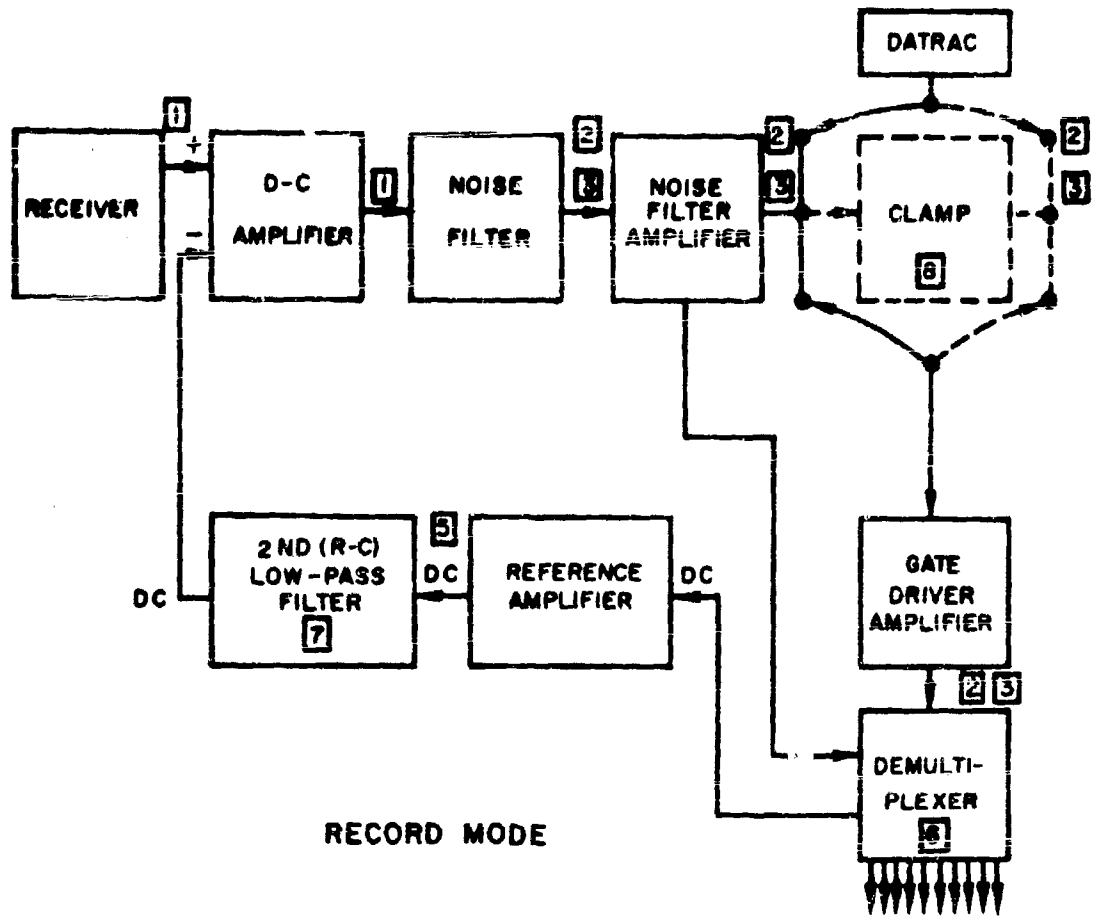
The DC Amplifier has a gain of approximately ten for the PAM signal from the receiver without inversion and a gain of approximately one for the feedback voltage with inversion. A schematic diagram of the DC Amplifier is in Fig. A-2; a block diagram of the Base Band Unit with appropriate waveforms is in Fig. 8-2. If there is trouble in the DC Amplifier, do the procedures in Paragraph 8.2 and proceed as follows:

1. Make sure that variable components are adjusted in accordance with Volume I, Section 4.

2. Check that PAM signal, Fig. 8-2, Note 1 appears at grid 2 of vacuum tube V1A (TP1). It should be approximately 1.5 volts peak-to-peak with negative peaks falling at 0 (±1) volt dc. If it is not, check diode CR7 for a 6 (±1) volt drop.

3. Check for presence of PAM signal at plate of tube V1B. Its negative peaks should be at +180 (±20) volts dc. If they are not, V1 or its associated components are faulty.

4. Check for presence of PAM signal at grid of tube V2A. Its negative peaks should be at +5 (±5) volts dc. If they are not, check diodes CR1, CR2, and CR3 to see that each has a 60 (±10) volt drop.



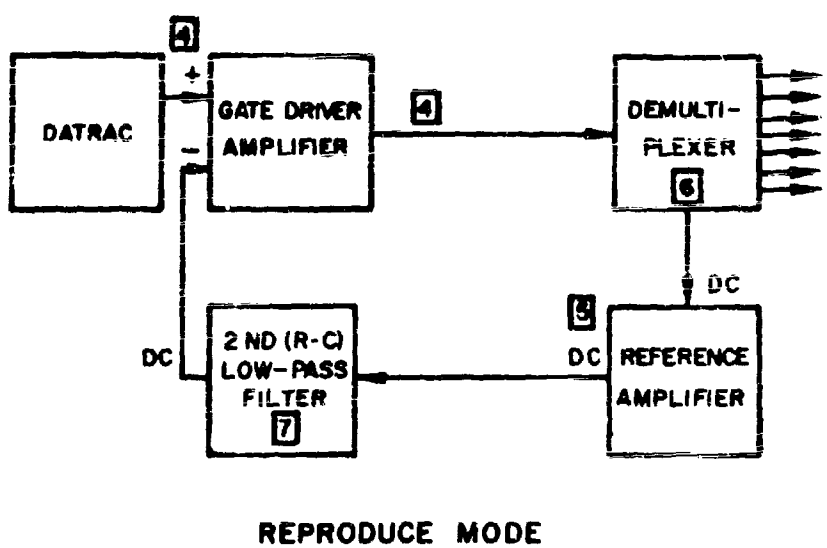


Fig. 8-2 Base Band Unit Block Diagram (Sheet 1 of 2)



[1] PORTION OF VIBRATION AND G-A COMPOSITE PULSE TRAINS



[2] OUTPUT OF G-A NOISE FILTER



[3] OUTPUT OF VIBRATION NOISE FILTER



[4] DATRAC REPRODUCE OUTPUT FOR VIBRATION AND G-A

[5] CAN CONTAIN SEVERAL VOLTS OF LOW FREQUENCY WHICH IS FILTERED OUT BY THE 2nd (R-C) LOW-PASS FILTER

[6] CONTAINS REFERENCE PULSE SELECTION CIRCUIT AND 1st LOW-PASS FILTER

[7] CONTAINED WITHIN GATE DRIVER AMPLIFIER CHASSIS

[8] DOTTED LINES SHOW OPTIONAL USE OF CLAMP DURING RECORD

Fig. 8-2 Base Band Unit Block Diagram (Sheet 2 of 2)

5. Check for presence of PAM signal at plate of tube V2B. Its negative peaks should be at +180 (±20) volts dc. If they are not, V2 or its associated components are faulty.

6. Check for presence of PAM signal at grid of tube V3A. Its negative peaks should be at +5 (±5) volts dc. If they are not, check diodes CR4, CR5, and CR6 to see that each has a 60 (±10) volt drop.

7. Check both plates of tube V3. The voltage of each should be +300 (±10) volts dc. If it is not, resistor R19 or R20 is faulty.

8. Check both cathodes of tube V3 (TP3). The PAM signal (Fig. 8-2, Note 1) should be 10 (±2) volts peak-to-peak with negative peaks at -2 (±3) volts. If it is not, V3 or its associated components are faulty.

9. Check grids of tubes V1B and V2B for presence of PAM signal that is no greater than 5 volts peak-to-peak. If signal is not correct, resistor R9, R10, R11, R15, or R16 is faulty.

8.7 NOISE FILTER, VIBRATION

The Vibration Noise Filter improves the signal-to-noise ratio of the PAM signal without introducing excessive crosstalk. It also provides a means of inserting a d-c offset. A schematic diagram of the Noise Filter is in Fig. A-3; a block diagram of the Base Band Unit with appropriate waveforms is in Fig. 8-2. If there is trouble in the Vibration Noise Filter, do the procedures in Paragraph 8.2 and proceed as follows:

1. Make sure that all variable components are adjusted in accordance with Volume I, Section 4.

2. Check that G-A/VIB switch is at VIB and that the proper plug-in unit is securely in place.

3. Check that PAM signal (fig. 8-2, Note 1) appears at input (TP4). It should be 10 (±2) volts peak-to-peak with negative peaks at -2 (±3) volts. If it is not, the trouble is in the DC Amplifier or the connecting cable.

4. Check that PAM signal appears at both grids of tube V1. It should be 3.5 (±2) volts peak-to-peak with negative peaks at -1 (±2) volts. If it is not, resistor R2, R3, R4, R5, or R6 or transformer L1 is faulty.

NOTE: The PAM signal waveform will be somewhat distorted on the grid of V1B; however, this is normal.

5. Check that PAM signal appears at both cathodes of tube V1. It should be 3.5 (±2) volts peak-to-peak with negative peaks at +6 (±3) volts. If it is not, V1 resistor R9 or R10, or associated components are faulty.

6. Check that PAM signal appears at both plates of tube V2. It should be 3.5 (±2) volts peak-to-peak with negative peaks at -4 (±3) volts. If it is not, resistor R7 or R8, tube V2, or associated components are faulty.

7. Check that output (Fig. 8-2, Note 3) of Noise Filter (TP5) is 3.5 (±2) volts peak-to-peak with negative peaks at -4 (±3) volts. If it is not, the output circuitry is faulty.

3.8 NOISE FILTER, G-A

The G-A Noise Filter improves the signal-to-noise ratio of the PAM signal without introducing excessive crosstalk. It also provides a means of inserting a d-c offset. A schematic diagram of the Noise Filter is in Fig. A-3; a block diagram of the Base Band Unit with appropriate waveforms is in Fig. 8-2. If there is trouble in the G-A Noise Filter, do the procedures in Paragraph 8.2 and proceed as follows:

1. Make sure that variable components are adjusted in accordance with Volume I, Section 4.

2. Check that G-A/VIB switch is at G-A and that G-A plug-in is securely in place.

3. Check that PAM signal (Fig. 8-2, Note 1) appears at input (TP4). It should be 10 (±2) volts peak-to-peak with negative peaks at -2 (±3) volts. If it is not, the trouble is in the DC Amplifier or the connecting cable.

4. Check that PAM signal appears at both grids of tube V1. It should be 3.5 (±2) volts peak-to-peak with negative peaks at -1 (±2) volts. If it is not, resistor R2 R3, R4, R5, or R6 or transformer L1 is faulty.

5. Check that PAM signal appears at both cathodes of tube V1. It should be 3.5 (±2) volts peak-to-peak with negative peaks at +6 (±3) volts. If it is not, tube V1, resistor R9 or R10, or associated components are faulty.

6. Check that PAM signal appears at both plates of tube V2. It should be 3.5 (±2) volts peak-to-peak with negative peaks at -4 (±3) volts. If it is not, resistor R7 R8, tube V2, or associated components are faulty.

7. Check that output of Noise Filter at TP5 (Fig. 8-2, Note 2) is 3.5 (±2) volts peak-to-peak with negative peaks at -4 (±3) volts. If it is not, the output circuit is faulty.

8.9 NOISE FILTER AMPLIFIER

The Noise Filter Amplifier amplifies the output of the Noise Filter so that (1) the dc-coupled output is 19 (±1) volts peak-to-peak, and (2) the ac-coupled output is between 0 and 15 volts peak-to-peak. A schematic diagram of the Noise Filter Amplifier is in Fig. A-4; a block diagram of the Base Band Unit with appropriate waveforms is in Fig. 8-2. If there is trouble in the Noise Filter Amplifier, do the procedures in Paragraph 8.2 and proceed as follows:

1. Make sure that variable components are adjusted in accordance with instructions in Volume I, Section 4.

2. Check that PAM signal (Fig. 8-2, Note 2 or 3) is at input (TP6) and is 3.5 (±2) volts peak-to-peak with negative peaks at -4 (±3) volts. If it is not, the trouble is in the Noise Filter or the connecting cable.

3. Check plate of tube V1A. The negative peaks of the PAM signal should be at +180 (±20) volts dc. If they are not, V1 or its associated components are faulty.

4. Check plate of tube V1B. The negative peaks of the PAM signal should be at 180 (±20) volts dc. If they are not, V1 or its associated components are faulty.

5. Check grid of tube V2A. The negative peaks of the PAM signal should be at 0 (±5) volts. If they are not, check that diodes CR1, CR2, and CR3 each has a 60 (±10) volt drop.

6. Check plate of tube V2B. The negative peaks of the PAM signal should be at +180 (±20) volts dc. If they are not, V2 or its associated components are faulty.

7. Check grid of tube V3A. The negative peaks of the PAM signal should be at 0 (±5) volts. If they are not, check that diodes CR4, CR5, and CR6 each has a 60 (±10) volt drop.

8. Check cathode of tube V3A (TP8). The PAM signal (Fig. 8-2, Note 2 or 3) should be 19 (±1) volts peak-to-peak with negative peaks at -9 (±1) volts dc. If it is not, V3 or its associated components are faulty.

9. Check grids of tubes V1B and V2B for presence of PAM signal that is no greater than 10 volts peak-to-peak. If the signal is not correct, resistor R7, R8, R9, or R13 is faulty.

10. Check that PAM signal appears at grid of tube V3B. Its amplitude should be between 0 and 15 volts peak-to-peak. If it is not, resistor R17 or R18 is faulty.

11. Check cathode of tube V3B. The PAM signal (Fig. 8-2, Note 2 or 3) should be between 0 and 15 volts peak-to-peak. If it is not, V3 or its associated components are faulty.

12. Check for ac video output at TP7. The PAM signal should be between 0 and 15 volts peak-to-peak. If it is not, capacitor C4 or resistor R16 or R23 is faulty.

8.10 REFERENCE VOLTAGE OPTIONAL CLAMP

The Reference Voltage Optional Clamp restores the d-c level to the PAM signal from the Noise Filter Amplifier if the DC Reference Feedback Loop should fail to operate properly.

A schematic diagram of the Clamp is in Fig. A-5. If there is trouble in the Clamp, do the procedures in Paragraph 8.2 and proceed as follows:

1. Check that PAM signal is at jack J28. It should be 19 (±1) volts peak-to-peak. (The d-c level is not important when the Clamp is being used.) If it is not, the Noise Filter Amplifier or the connecting cable is faulty.

2. Check output PAM signal at either jack J29 or J31. When the SERVO-CLAMP switch is at CLAMP, the negative peaks should fall at -9 (±0.5) volts. If it does not, check voltage drop across diode CR2. It should be 9 (±0.5) volts. If it is not, replace diode CR2.

3. Check capacitor C1 and replace if necessary.

4. Check diode CR1 for forward conduction and high inverse impedance. Replace diode if necessary.

8.11 GATE DRIVER AMPLIFIER

The Gate Driver Amplifier inserts a gain factor of approximately 0.33 and a d-c offset voltage into the PAM signal. It also contains the second low-pass filter of the d-c reference feedback loop. A schematic diagram of the Gate Driver Amplifier is in Fig. A-11; a block diagram of the Base Band Unit with appropriate waveforms is in Fig. 8-2. If there is trouble in the Gate Driver Amplifier, do the procedures in Paragraph 8.2 and proceed as follows:

1. Adjust variable components as follows: With the input at jack J13 disconnected, and resistor R18 set at mid-scale, resistor R8 should be adjusted for zero output at test point TP11. With the input connected, resistor R3 (attenuator) should be adjusted so that the peak-to-peak voltage with full modulation is 6.5 (± 0.5) volts. Resistor R18 (DC Offset No. 2) should be adjusted so that the sync level is -1.5 (± 0.25) volts at test point TP11. Resistor R18 (limiter bias) should be adjusted so that the positive peaks of the pulse train will be clipped at +8 (±0.5) volts.

2. Check for input signal at TP9. It should be as shown in Fig. 8-2, Note 2 or 3, as applicable. The signal should be 19 (±1) volts with negative peaks at -9 (±1) volts. If it is not, check functioning of relay K1. If the relay is functioning properly, the trouble is in the Noise Filter Amplifier or the connecting cable.

3. Check for presence of PAM signal on grid of tube V1A. It should be between 4 and 8 volts peak-to-peak and symmetrical about the zero axis. If it is not, resistor R1, R2, R3, or R5 is faulty.

4. Check plate of tube V1A. The negative peaks of the PAM signal should be +180 (±20) volts. If they are not, V1 or resistor R6 or R7 is faulty.

5. Check plate of tube V1B. The negative peaks of the PAM signal should be at +180 (±20) volts. If they are not, V1 or its associated components are faulty.

6. Check both grids of tube V2. The PAM signal should be 7 (±1) volts peak-to-peak. The negative peaks should be -2 (±5) volts. If they are not, check diode CR1 for a 175 (±20) volt drop. Also, check diode CR2 for inverse breakdown.

7. Check plates of tube V2 for +300 (±10) volts dc. If the signal is not correct, V2 or its associated components are faulty.

8. Check cathodes of tube V2. The PAM signal should be 7 (±1) volts peak-to-peak. The negative peaks should be at +5 (±5) volts. If the signal is incorrect V2, or its associated components are faulty.

9. Check grid of tube V1B. The PAM signal should be less than 6 volts peak-to-peak. If it is not, resistor R11 or R14 or relay K2 is faulty.

10. Check output at TP11. It should be as shown in Fig. 8-2, Note 4. The signal should be 7 (±1) volts peak-to-peak. The negative peaks should be at +5 (±5) volts. If the signal is not correct, V2 or its associated components are faulty.

11. Check relay K2 to make sure that resistor R11 is grounded while on record mode and receives signal from low-pass filter on reproduce mode. If not, check relay wiring and power to relay.

8.12 REFERENCE AMPLIFIER

For instructions on isolating and repairing trouble in the Reference Amplifier, refer to the Electro Instruments, Inc., Handbook of Operating and Maintenance Instructions, A-12 DC Amplifier. A schematic diagram of the Reference Amplifier is in Fig. A-7.

8.13 DATA SYNC SEPARATOR

The Data Sync Separator, by means of a 40-kc (Vibration) or 16-kc (G-A) band-pass filter, regenerates clock and data sync information from the PAM pulse train. A schematic diagram of the Vibration Data Sync Separator is in Fig. A-8; a block diagram is in Fig. 8-3. A schematic diagram of the G-A Data Sync Separator is in Fig. A-39; a block diagram is in Fig. 8-4. If there is trouble in either the Vibration or G-A Data Sync Separator, do the procedures in Paragraph 8.2 and proceed as follows:

1. Make sure that clamp and clipper is adjusted properly by checking that signal at TP1 is as shown in Fig. 8-3 or 8-4, as applicable. If not, adjust as follows: The output level control of the clamp-and-clipper circuit, resistor R19, is adjusted so that the peak-to-peak amplitude of the output sine wave at the junction of capacitor C14 and diode CR7 is 15 (±1) volts. Fine tuning of the tank circuit is made by adjusting capacitor C13A.

   To make this adjustment, a dual-trace oscilloscope should be used to observe the a-c video at the junction of capacitor C1 and diode CR3 while the band-pass filter output is observed at pin d. Any probes connected to the outputs of the tank circuit should be removed when making this adjustment. The phase difference between the a-c video and the band-pass filter output sine wave at pin d should be reduced to ±10 degrees by adjusting capacitor C13A. The zero crossing points of these two waveforms should be used when making this phase comparison. Zero crossing points are half-way between peak-to-peak.

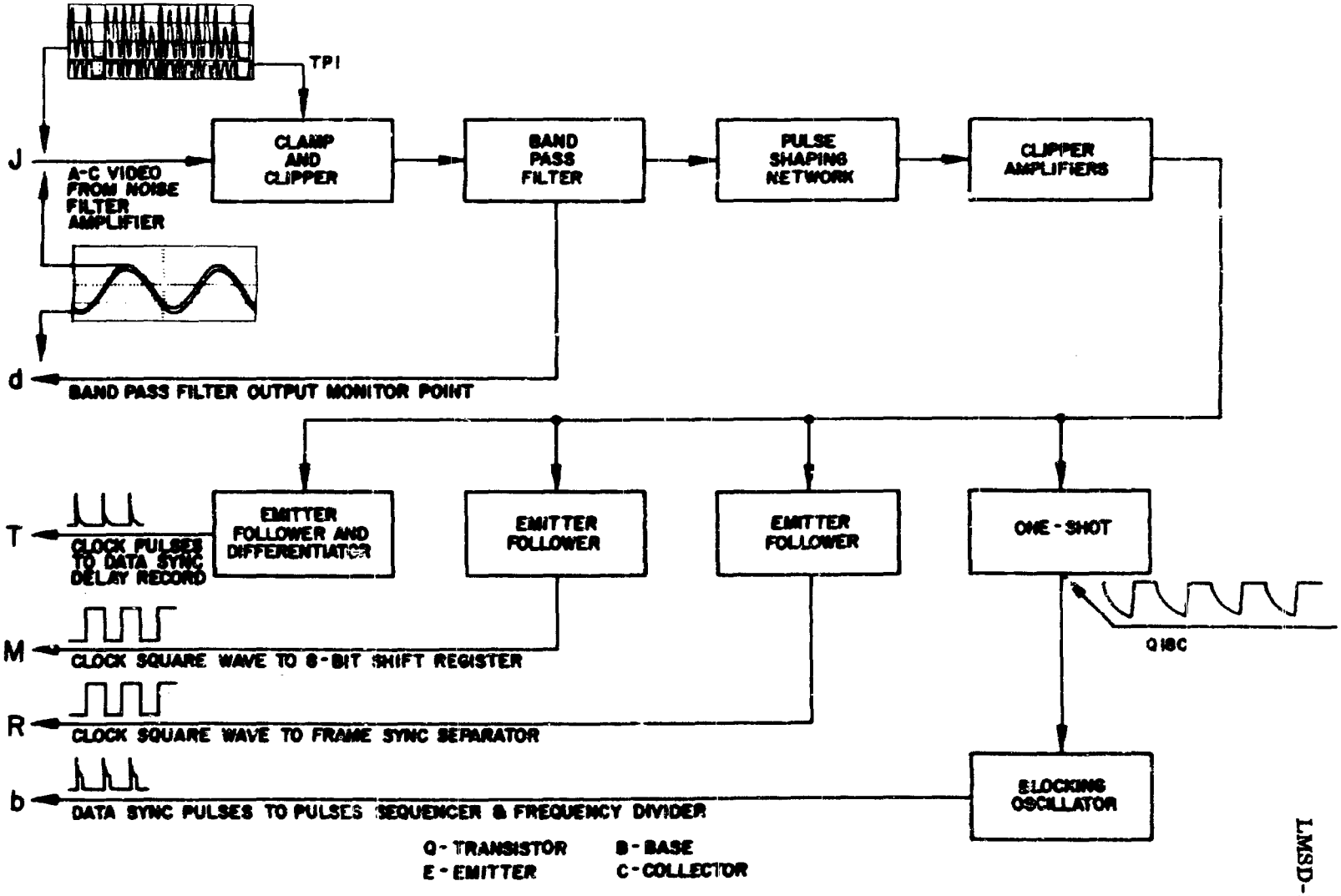


Fig. 8-3 Data Sync Separator Block Diagram, Vibration

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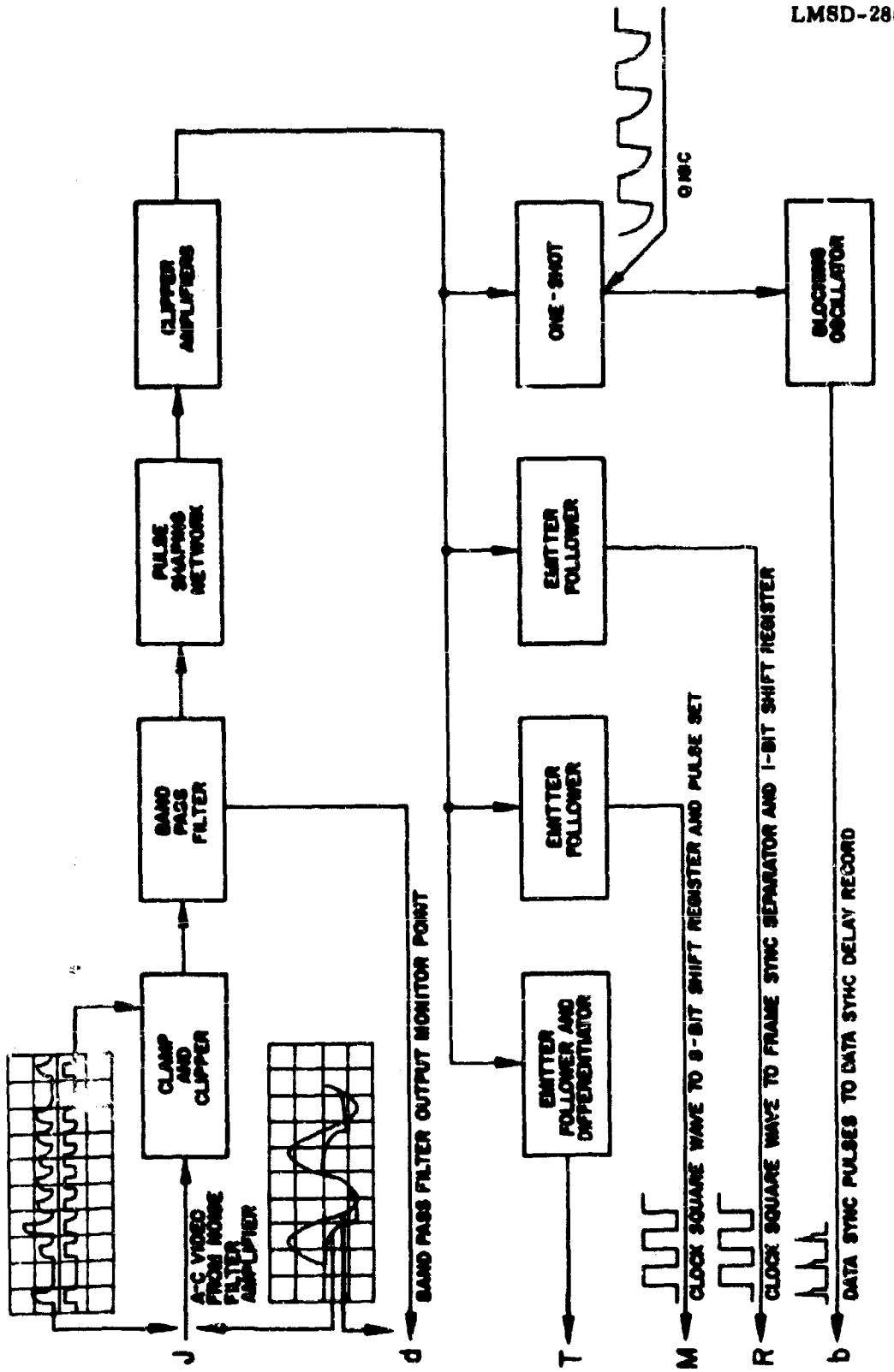


Fig. 8-4 Data Sync Separator Block Diagram, G-A

2. Check supply voltage across decoupling capacitors. It should be +20 (±1) volts across C3 and -10 (±1) volts across C24. If it is not, check diode CR1 for 10 (±1) volts drop, and check both decoupling networks.

3. Check for presence of clipped and clamped PAM signal at TP1 (Fig. 8-3 or 8-4, as applicable). If it is absent or not correct, make the following checks in the order given.

a. Check diodes CR3 and CR13 by checking that PAM signal appears in clamped form at base of transistor Q3.

b. Check that clamped PAM signal appears at emitter of transistor Q3. If it does not, transistor Q3 or resistor R9 is faulty.

4. Check for presence of input at pin d, as shown in Fig. 8-3 or 8-4, as applicable. It should be 1.6 (±0.2) volts peak-to-peak. If it is not, make the following checks in the order given.

a. Check that clipped and clamped PAM signal appears at emitter of transistor Q6. If it does not, transistor Q6, diode CR3, or resistor R13, R14, R15, R18, or R19 is faulty.

b. Check that sine wave of 15 (±2) volts appears at collector of transistor Q11. If it does not, transistor Q11 or its associated components are faulty.

c. Check diode CR7 by checking that clamped sine wave appears at base of transistor Q14.

d. Check that clamped sine wave appears at emitter of transistor Q14. If it does not, transistor Q14 is faulty.

e. Check that clamped sine wave appears at emitter of transistor Q17. If it does not, transistor Q17 or resistor R44 or R45 is faulty.

5. Check emitter of transistor Q9. Its output should be a square wave. If it is not, make the following checks in the order given.

a. Check diodes CR9 and CR10 for an approximately square wave of 0.5 volt peak-to-peak. If the signals are incorrect, diode CR9 or CR10, capacitor C18, or resistor R48 is faulty.

b. Check collector of transistor Q19. Its output should be an approximately square wave. If it is not, transistor Q19, capacitor C22, or resistor R53 or R54 is faulty.

c. Check collector of transistor Q2. Its output should be an approximately square wave. If it is not, transistor Q2, diode CR12, capacitor C2, or resistor R2, R6, or R7 is faulty.

d. Check intersection of resistors R11 and R12 for an approximately square wave. If it is not present, transistor Q5 or resistor R11 or R12 is faulty.

e. Check collector of transistor Q7. Its output should be an approximately square wave. If it is not, transistor Q7, diode CR5, capacitor C7, or resistor R16 or R20 is faulty. If these components are found to be operating properly, the trouble is in transistor Q9 or resistor R23.

6. Check for positive pulse at pin T. If it is not present, check emitter of transistor Q1 for an approximate square wave. If it is not present, transistor Q1 or resistor R3 is faulty. If these components are found to be operating properly, the trouble is transistor Q4, capacitor C4, diode CR2, or resistor R8 or R10.

7. Check pin M for a clock square wave. If it is not present, transistor Q8 or resistor R17 or R21 is faulty.

8. Check pin R for a clock square wave. If it is not present, transistor Q10 or resistor R24 or R28 is faulty.

9. Check pin b for blocking oscillator pulses. If they are not present, make the following checks.

a. Check emitter of transistor Q12 for a square wave. If it is not present, transistor Q12 or resistor R17 or R30 is faulty.

b. Check collector of transistor Q18. The output of the one-shot should be as shown in Fig. 8-3 or 8-4, as applicable. If it is not, the one-shot is faulty. In this case, refer to Paragraph 8.4.2 for corrective action. If the one-shot is found to be operating properly, the blocking oscillator is faulty. In this case refer to Paragraph 8.4.1 for corrective action.

8.14 FRAME SYNC SEPARATOR

The Frame Sync Separator generates a sync pulse for each sync interval in the composite PAM pulse train. A schematic diagram of the Vibration Frame Sync Separator is in Fig. A-9; a block diagram is in Fig. 8-5. A schematic diagram of the G-A Frame Sync Separator is in Fig. A-40; a block diagram is in Fig. 8-6. If there is trouble in either the Vibration of the G-A Frame Sync Separator, do the procedures in Paragraph 8.2 and proceed as follows:

1. Make sure that variable components are adjusted properly in accordance with Volume I, Section 4.

2. Check supply voltages across decoupling capacitors. It should be +20 (±1) volts across capacitor C1 and -10 (±1) volts across capacitor C3. If it is not, check diode CR1 for 10 (±1) volts drop, and check both decoupling networks.

3. Check pin R for a clock square wave. If it is not present, refer to Paragraph 8.3 for corrective action.

4. Check for clock pulses at pin S. If it is not present, the clock blocking oscillator is faulty. Refer to Paragraph 8.4.1 for corrective action.

5. Check collector of transistor Q9. The output of the one-shot should be as shown in Fig. 8-5 or 8-6, as applicable. If it is not, the one-shot is faulty. Refer to Paragraph 8.4.2 for corrective action.

6. Check collectors of transistors Q10 and Q11 for negative blocking oscillator pulses. If they are not present, the blocking oscillator is faulty. Refer to Paragraph 8.4.1 for corrective action.

7. Check for presence of clipped and clamped PAM signal at TP1. It should be as shown in Fig. 8-5 or 8-6, as applicable. If it is not, make the following checks in the order given.

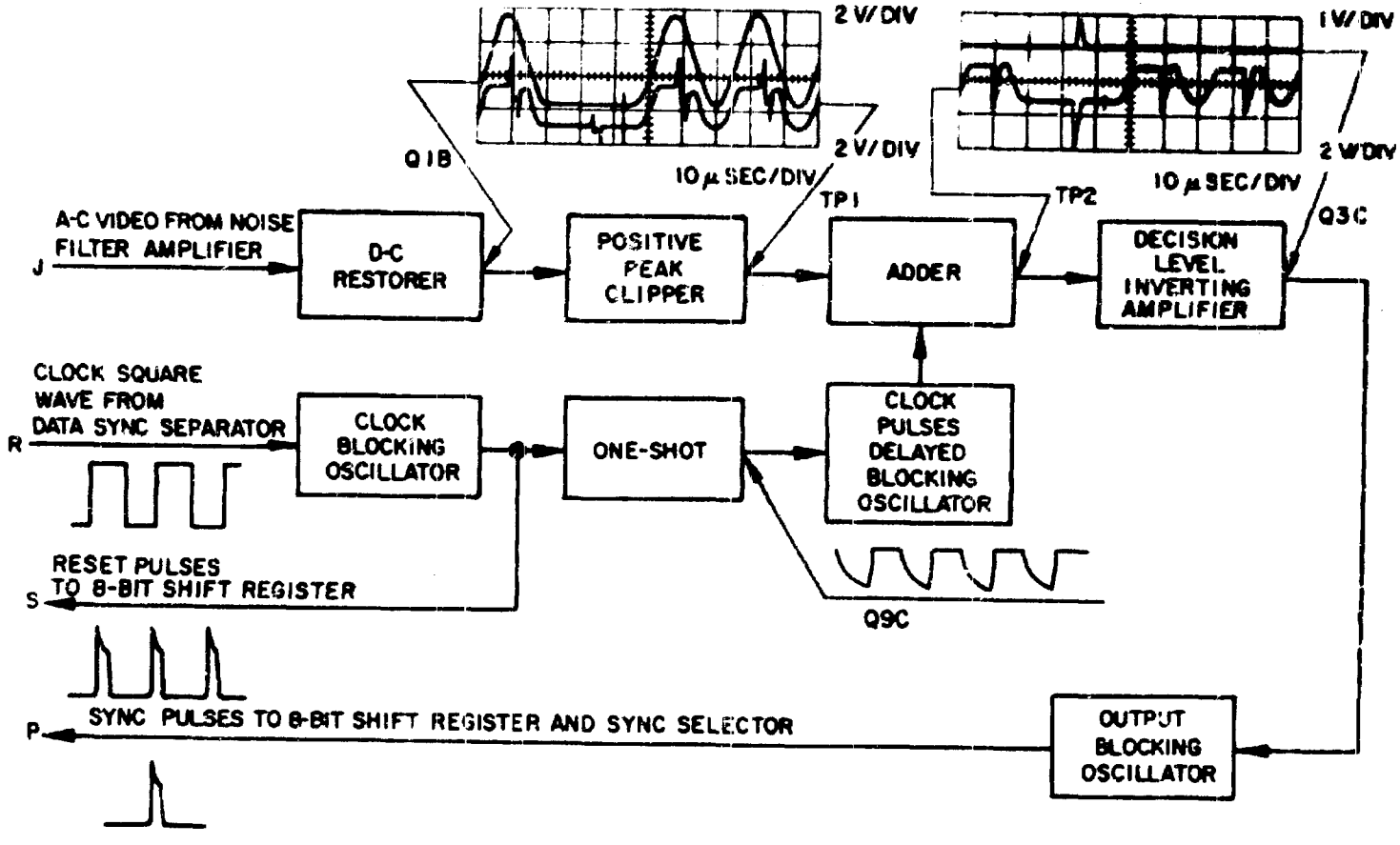


Fig. 8-5 Frame Sync Separator Block Diagram, Vibration

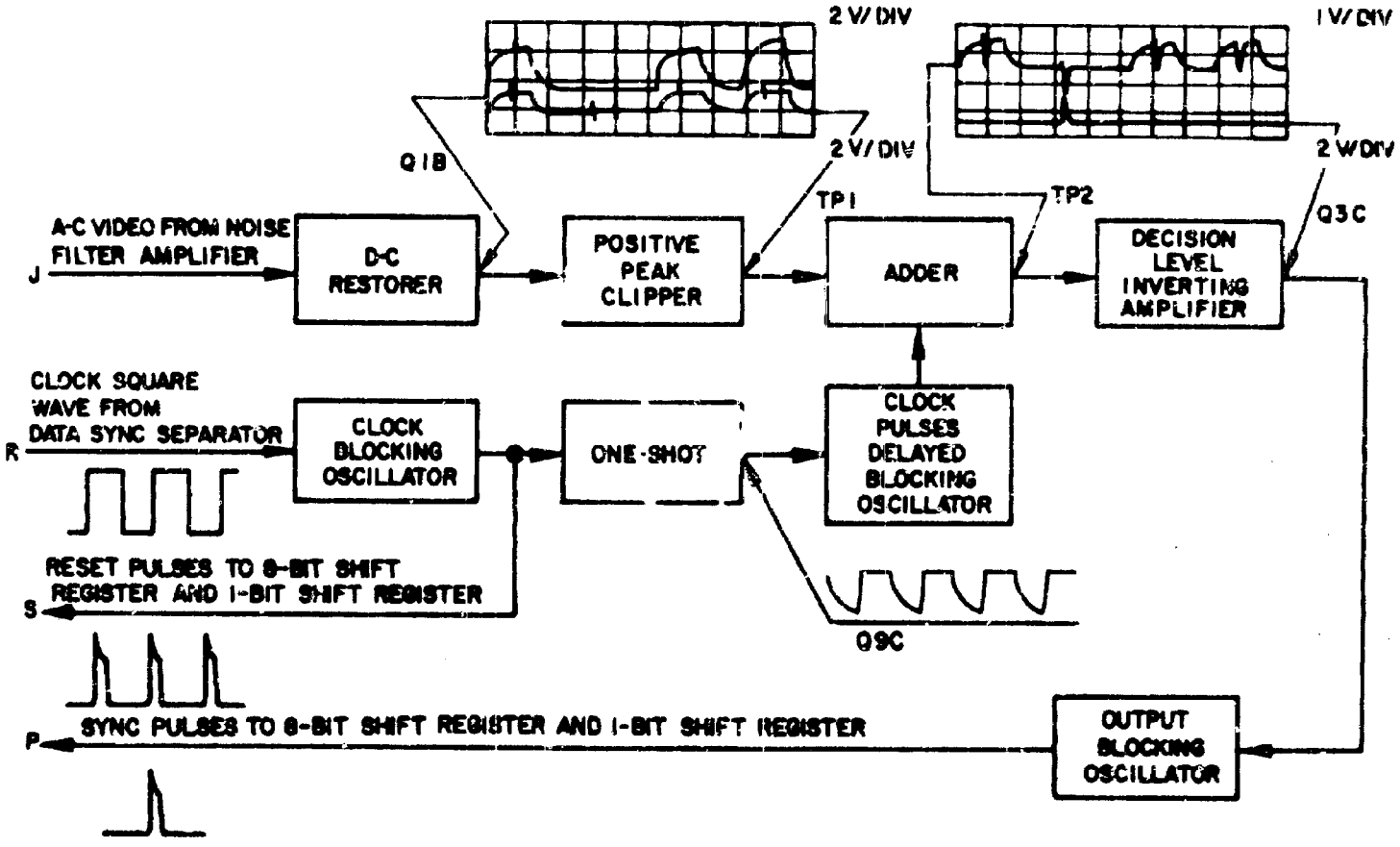


Fig. 8-3 Frame Sync Separator Block Diagram, G-A

a. Check diodes CR2 and CR11 by checking that clamped and clipped PAM signal appears at base of transistor Q1

b. Check that clamped PAM signal appears at emitter of transistor Q1. If it does not, transistor Q1 or resistor R6 is faulty.

8. Check output at TP2. It should be as shown in Fig. 8-5 or 8-6, as applicable. If it is not, diode CR3 or its associated components are faulty.

9. Check emitter of transistor Q2. Its output should be a negative spike of approximately 1 volt. If it is not, transistor Q2 or its associated components are faulty.

10. Check collector of transistor Q3. Its output should be as shown in Fig. 8-5 or 8-6, as applicable. If it is not, transistor Q3 or its associated components are faulty.

11. Check for blocking oscillator pulses at pin P. If they are not present, the blocking oscillator is faulty. Refer to Paragraph 8.4.1 for corrective action.

8.15 EIGHT-BIT SHIFT REGISTER

The Eight-Bit Shift Register delays sync information eight data channels in time so that the signal can be logically compared. A schematic diagram of the Vibration Eight-Bit Shift Register is in Fig. A-10; a block diagram is in Fig. 8-7. A schematic diagram of the G-A Eight-Bit Shift Register is in Fig. A-41; a block diagram is in Fig. 8-8. If there is trouble in either the Vibration of the G-A Eight-Bit Shift Register, do the procedures in Paragraph 8.2 and proceed as follows:

1. Check supply voltage across decoupling capacitor C20. It should be 20 (±1) volts. If it is not, check decoupling network.

2. Check pin M for clock square wave. If it is not present, refer to Paragraph 8.3 for corrective action.

3. Check collector of transistor Q2 for a square wave of 18 (±2) volts. If it is not present, transistor Q2, capacitor C2, diode CR3, or resistor R4 or R5 is faulty.

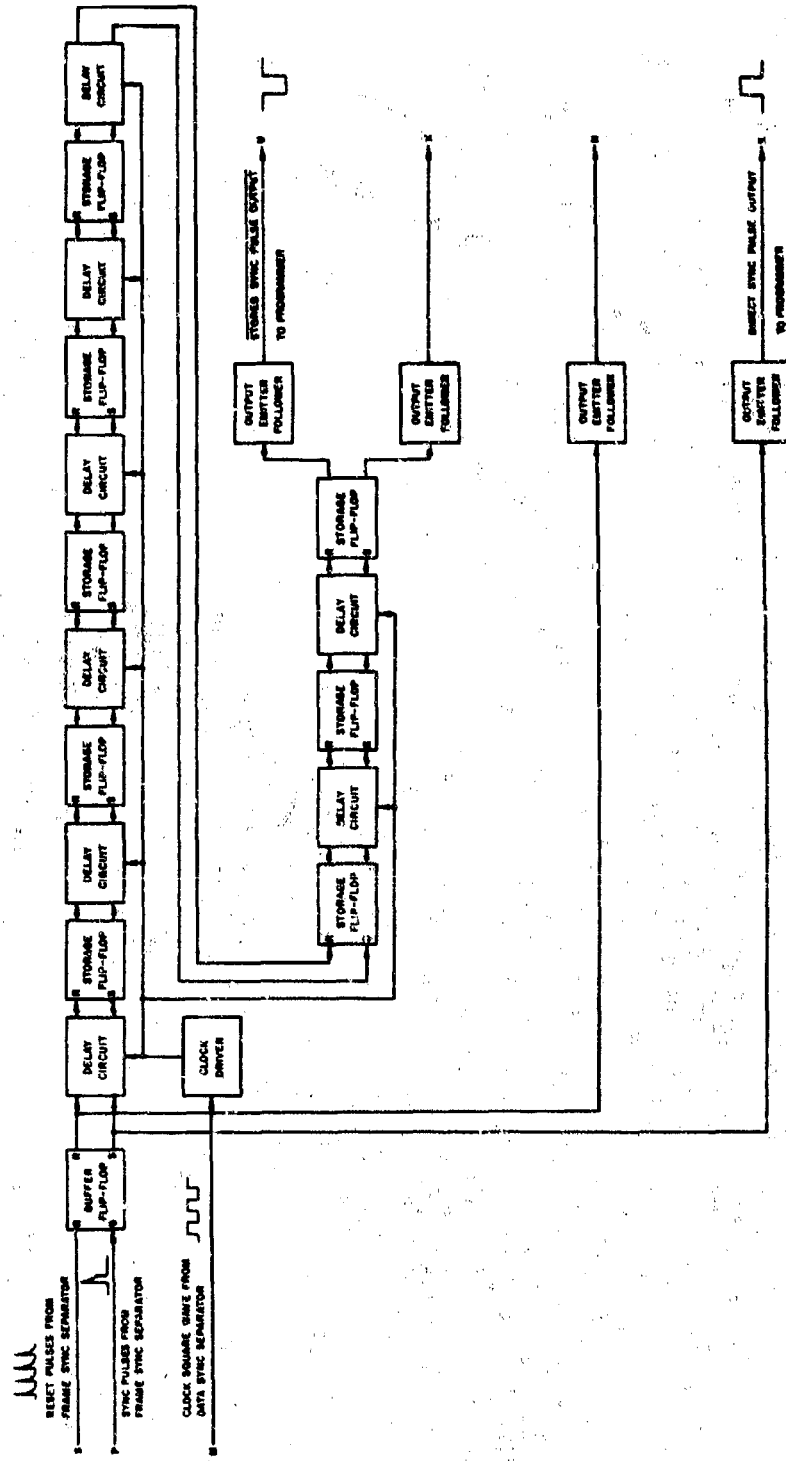


Fig. 8-7 Eight-Bit Shift Register Block Diagram, Vibration

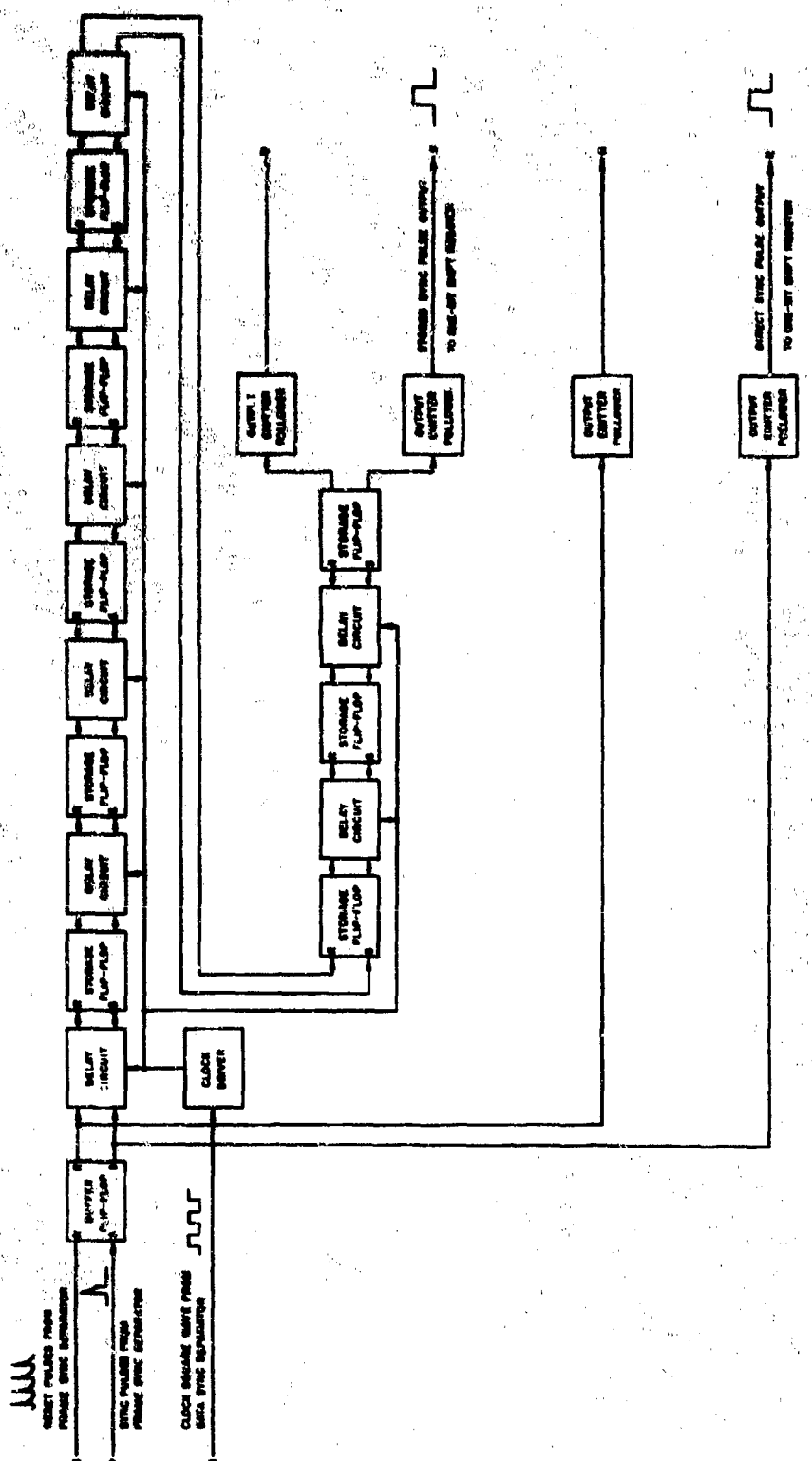


Fig. 8-8 Eight-Bit Shift Register Block Diagram, G-A

4. Check pin S for reset pulses, as shown in Fig. 8-7 or 8-8 as applicable. If they are not present or correct, refer to Paragraph 8.3 for corrective action.

5. Check pin P for sync pulses. If they are not present or correct, refer to Paragraph 8.3 for corrective action.

6. Check collector of transistor Q1. Its output should be positive rectangular pulses of 18 (±2) volts that are in time phase with sync pulses on pin P. If not, the flip-flop is faulty. Refer to Paragraph 8.4.3 for corrective action.

7. Check collector of transistor Q3. Its output should be a negative (from +20 volts) rectangular pulse of 18 (±2) volts that is in time phase with the sync pulse on pin P. If it is not, the flip-flop is faulty. Refer to Paragraph 8.4.3 for corrective action.

8. Check emitter of transistor Q23. There should be a positive rectangular pulse of 18 (±2) volts that is in time phase with the sync pulse on pin P. If not, transistor Q23 or resistor R60 is faulty.

9. Check intersection of diodes CR6 and CR7, capacitor C5, and resistor R10. The signal should charge exponentially to 18 (±2) volts and discharge to 0 during the positive portion of the clock square wave on pin M. This should be in time phase with the sync pulses at pin P. If the signal or time phasing is incorrect, diode CR6 or CR7, capacitor C5, or resistor R10 is faulty.

10. Check intersection of diodes CR4 and CR5, capacitor C4, and resistor R9. The signal should charge exponentially to 18 (±2) volts and discharge to 0 during the positive portion of the square wave on pin M. It should be present every time that there is a clock square wave and not a signal on pin P. If the signal or time phasing is incorrect, diode CR4 or CR5, capacitor C5, or resistor R9 is faulty.

11. Check intersection of diodes CR8 and CR9 and capacitor C5. There should be a negative spike for every pulse on pin P. If there is not, diode CR8 or CR9 or capacitor C5 is faulty.

12. Check intersection of diodes CR10 and CR11 and capacitor C4. There should be a negative spike every time that there is a clock square wave and not a signal at

pin P. If the signal or time phasing is not correct, diode CR10 or CR11 or capacitor C4 is faulty.

13. Check collector of transistor Q4. There should be a positive rectangular pulse of 18 (*2) volts and it should be delayed one clock period with respect to the pulse on pin P. If the signal is incorrect, the flip-flop is faulty. Refer to Paragraph 8.4.3 for corrective action.

14. Check collector of transistor Q5. Its output should be a negative rectangular pulse of 18 (±2) volts that is delayed one clock period with respect to the sync pulse on pin P. If the signal is incorrect, the flip-flop is faulty. Refer to Paragraph 8.4.3 for corrective action.

15. Check each remaining stage by doing steps 9 through 12 for each stage.

NOTE: Time phasing of signals in the first-stage flip-flop will be delayed one clock period from those in the buffer flip-flop. Time phasing of the signal in the second stage flip-flop will be delayed two clock periods from those in the buffer flip-flop, etc. Also, the signals will be measured on corresponding components with different reference designation numbers.

16. Check emitter of transistor Q20. Its output should be as shown for pin U in Fig. 8-7. If it is not, transistor Q20 or resistor R57 is faulty. For G-A, check emitter of transistor Q21. Its output should be the same as that shown for pin X in Fig. 8-8. If it is not, transistor Q21 or resistor R58 is faulty.

8.16 ONE-BIT SHIFT REGISTER

The One-Bit Shift Register produces an output pulse whenever (1) sync pulses from the Frame Sync Separator arrive one clock period apart and (2) whenever two pulses from the Eight-Bit Shift Register coincide. A schematic diagram of the One-Bit Shift Register is in Fig. A-41; a block diagram is in Fig. 8-9. If there is trouble in the One-Bit Shift Register, do the procedures in Paragraph 8.2 and proceed as follows:

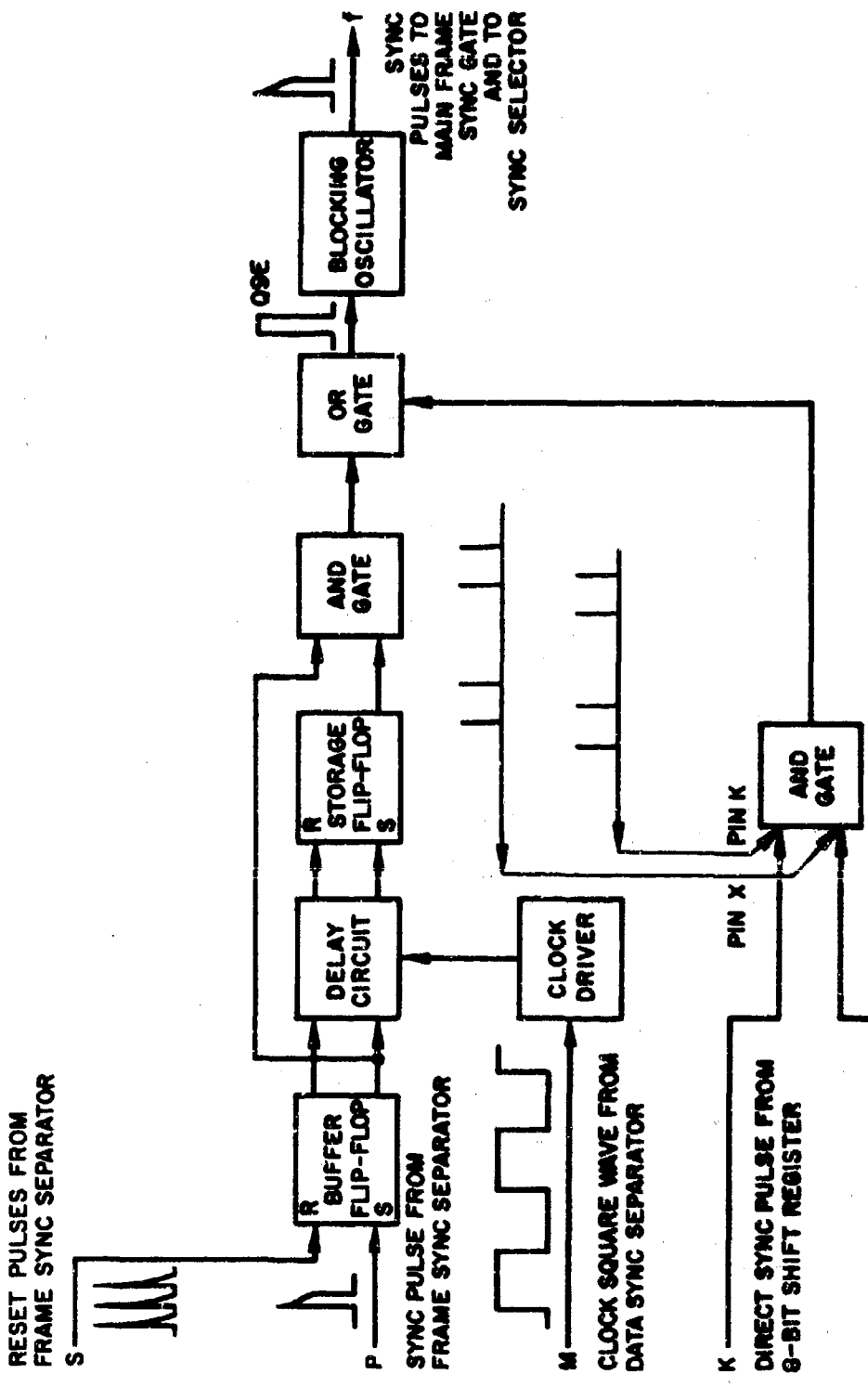


Fig. 8-9 One-Bit Shift Register Block Diagram

1. Check supply voltage across decoupling capacitor C10. It should be +20 (±1) volts. If it is not, check decoupling network. Also, check voltage at cathode of diode CR6. It should be 10 (±1) volts. If not, diode CR6 or resistor R21 is faulty.

2. Check input at pin S. It should be as shown in Fig. 8-9. If it is not, refer to Paragraph 8.3 for corrective action.

3. Check input at pin P. It should be as shown in Fig. 8-9. If it is not, refer to Paragraph 8.3 for corrective action.

4. Check input at pin M. It should be as shown in Fig. 8-9. If it is not, refer to Paragraph 8.3 for corrective action.

5. Check input at pin K. It should be as shown in Fig. 8-9. If it is not, refer to Paragraph 8.3 for corrective action.

6. Check input at pin X. It should be as shown in Fig. 8-9. If it is not, refer to Paragraph 8.3 for corrective action.

7. Check collector of transistor Q2. Its output should be positive rectangular pulses of 18 (±2) volts that are in time phase with the sync pulses at pin P. If not, the flip-flop is faulty. Refer to Paragraph 8.4.3 for corrective action.

8. Check collector of resistor Q3. Its output should be a negative (from +20 volts) rectangular pulse of 18 (±2) volts in time phase with the sync pulse at pin P. If it is not, the flip-flop is faulty. Refer to Paragraph 8.4.3 for corrective action.

9. Check intersection of diode CR6, diode CR7, capacitor C5, and resistor R11. The signal should charge exponentially to 18 (±2) volts and discharge to 0 during the positive portion of the clock square wave at pin M. This should occur in time phase with the sync pulses at pin P. If the signal or time phasing is incorrect, diode CR6 or CR7, capacitor C5, or resistor R11 is faulty.

10. Check intersection of diode CR4, diode CR5, capacitor C4, and resistor R10. The signal should charge exponentially to 18 (±2) volts and discharge to 0 during the positive portion of the square wave on pin M. It should be present every time that there is a square wave and not a signal on pin M. If the signal or time phasing is incorrect, diode CR4 or CR5, capacitor C4, or resistor R10 is faulty.

11. Check intersection of diode CR8, diode CR9, and capacitor C5. There should be a negative spike for every pulse on pin P. If not, diode CR8 or CR9 or resistor R10 is faulty.

12. Check intersection of diodes CR10 and CR11 and capacitor C4. There should be a negative spike every time that there is a clock square wave and not a signal at pin P. If the signal or time phasing is not correct, diode CR10, CR11, or capacitor C4 is faulty.

13. Check collector of transistor Q4. There should be a positive rectangular pulse of 18 (±2) volts and it should be delayed one clock period with respect to the pulse on pin P. If the signal is not correct, the flip-flop is faulty. Refer to Paragraph 8.4.3 for corrective action.

14. Check collector of transistor Q5. Its output should be a negative rectangular pulse of 18 (±2) volts that is delayed one clock period with respect to the sync pulse on pin P. If the signal is incorrect, the flip-flop is faulty. Refer to Paragraph 8.4.3 for corrective action.

15. Check emitters of transistors Q6 and Q7. The signal at each point should be as described previously for the collectors of transistors Q4 and Q2, respectively. If not, transistor Q6 or Q7, or resistor R16 or R17 is faulty.

16. Check intersection of diode CR12, diode CR13, and resistor R8. The signal should be a rectangular pulse of 18 (±2) volts amplitude that is in time phase with Channel 1 sync pulse on pin P. If it is not, diode CR12, diode CR13, or resistor R8 is faulty.

17. Check intersection of diode CR14, diode CR15, and resistor R9. The signal should be a rectangular positive pulse of 18 (±2) volts that is in time phase with Channel 9 sync pulse at pin P. If it is not, diode CR14, diode CR15, or resistor R9 is faulty.

18. Check intersection of emitters of transistors Q8 and Q9, resistor R20, and capacitor C6. The signal should be positive rectangular pulses of 18 (±2) volts in time phase with Channel 1 and Channel 9 sync pulses at pin P. If it is not, transistor Q8 or Q9, resistor R20, or capacitor C6 is faulty.

19. Check output at pin f. It should be as shown in Fig. 8-9 with an amplitude of 8 (±2) volts, and it should be in time phase with the pulses measured in Step 18.

8.17 PROGRAMMER

The Programmer performs the ANDing logic associated with the Eight-Bit Shift Register and provides the binary countdown for the Sync Gate. A schematic diagram of the Programmer is in Fig. A-11; a block diagram is in Fig. 8-10. If there is trouble in the Programmer, do the procedures in Paragraph 8.2 and proceed as follows:

1. Check supply voltage across decoupling capacitor C6. It should be +20 ±1) volts. If it is not, check decoupling network.

2. Check pin K for input as shown in Fig. 8-10. If the input is incorrect, refer to Paragraph 8.3 for corrective action.

3. Check pin U for input as shown in Fig. 8-10. If the input is incorrect, refer to Paragraph 8.3 for corrective action.

4. Check base of transistor Q1. Its output should be as shown in Fig. 8-10. If it is not, check diodes CR1 and CR2, transistor Q1, and resistor R1.

5. Check pin Z for waveform as shown in Fig. 8-10. If it is not correct, transistor Q1 or resistor R2 is faulty.

6. Check pin d for keying pulse input as shown in Fig. 8-10. If it is not correct, refer to Paragraph 8.3 for corrective action.

7. Check pin f for main frame sync input as shown in Fig. 8-10. If it is not correct, refer to Paragraph 8.3 for corrective action.

8. Check pin a for keying pulse output as shown in Fig. 8-10. If it is not correct, the flip-flop is faulty. Refer to Paragraph 8.4.3 for corrective action.

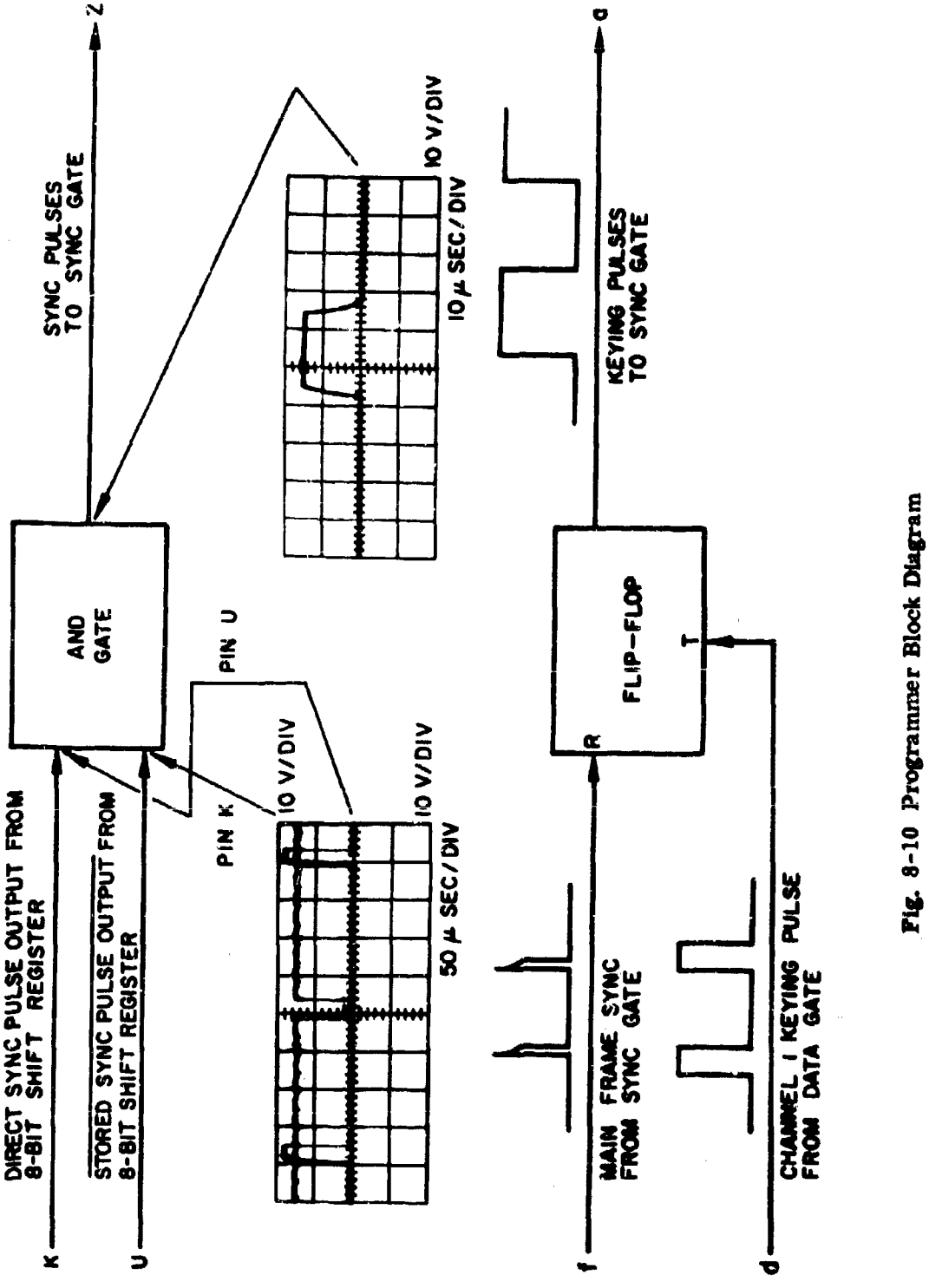


Fig. 8-10 Programmer Block Diagram

8.18 SYNC SELECTOR

The Sync Selector gates subcom sync pulses to the subcom sync gate and combines these pulses with main frame sync pulses. This combination, called composite frame sync, is delivered to the Record Electronics for recording. A schematic diagram of the Vibration Sync Selector is in Fig. A-12; a block diagram is in Fig. 8-11. A schematic diagram of the G-A Sync Selector is in Fig. A-42; a block diagram is in Fig. 8-12. If there is trouble in either the G-A Sync Selector or the Vibration Sync Selector, do the procedures in Paragraph 8.2 and proceed as follows:

1. Check supply voltage across decoupling capacitor C1. It should be +20 (±1) volts. If it is not, check decoupling network. Check voltage across decoupling capacitor C2. It should be -10 (±1) volts. If it is not, check resistor R5, diode CR1, and capacitor C2.

2. Check input at pin Z. It should be as shown in Fig. 8-11 or 8-12, as applicable. If it is not, refer to Paragraph 8.3 for corrective action.

3. Check emitter of transistor Q2. It should be the same as the input as pin Z, as shown in Fig. 8-11 or 8-12, as applicable. If it is not, transistor Q2 or resistor R6 is faulty.

4. Check input at pin K. It should be as shown in Fig. 8-11 or 8-12, as applicable. If it is not, refer to Paragraph 8.3 for corrective action.

5. Check collector of transistor Q3. Its output should be -10 (±1) volts with baseline at +14 (±3) volts. If it is not, resistor R3, R7, or R9 or transistor Q3 or Q5 is faulty.

6. Check input at pin P. It should be as shown in Fig. 8-11 or 8-12, as applicable. If it is not, refer to Paragraph 8.3 for corrective action.

7. Check emitter of transistor Q1. Its output should be the same as the input at pin P, as shown in Fig. 8-11 or 8-12, as applicable. If it is not, transistor Q1 or resistor R4 is faulty.

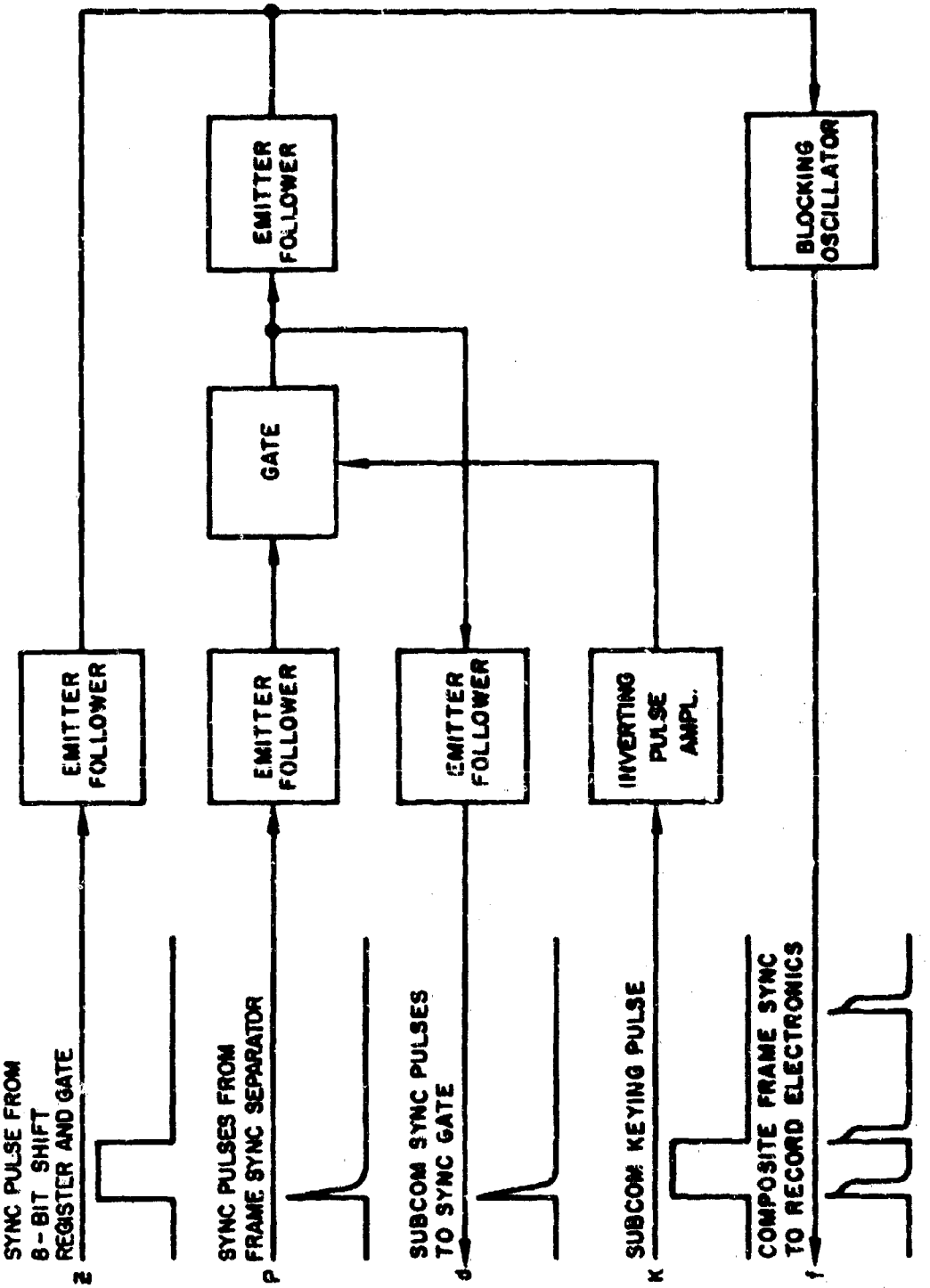


Fig. 8-11 Sync Selector Block Diagram, Vibration

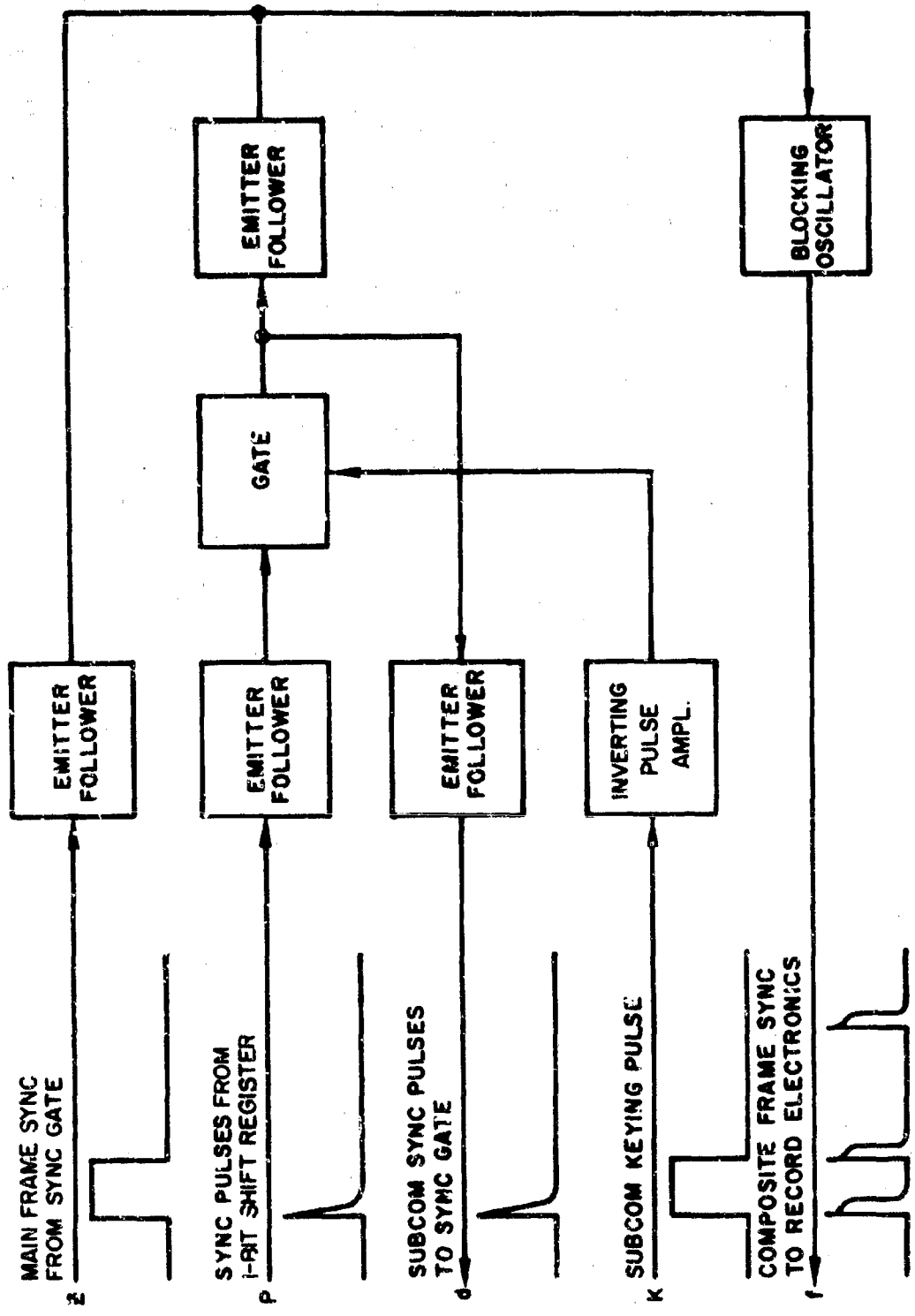


Fig. 8-12 Sync Selector Block Diagram, G-A

8. Check collector of transistor Q4. Its output should be the same as the input at pin P, as shown in Fig. 8-11 or 8-12, as applicable. If it is not, transistor Q4, resistors R8 or R10, or capacitor C7 is faulty.

9. Check output at pin d. It should be as shown in Fig. 8-11 or 8-12, as applicable. If it is not, transistor Q7 or resistor R12 is faulty.

10. Check emitter of transistor Q6. Its output should be the same as the output at pin d, as shown in Fig. 8-11 or 8-12, as applicable. If it is not, transistor Q5 or Q6 or resistor R11 is faulty.

11. Check output at pin f. It should be as shown in Fig. 8-11 or 8-12, as applicable. If it is not, the blocking oscillator, capacitors C3 or C4, resistor R13, or diode CR2 is faulty. Refer to Paragraph 8.4.1 for procedures on troubleshooting the blocking oscillator.

8.19 SYNC GATE

The Sync Gate allows sync pulses to pass only when a true sync pulse is expected. All other potential sync pulses are blocked from the Demultiplexer. A schematic diagram of the Sync Gate is in Fig. A-13; a block diagram is in Fig. 8-13. If there is trouble in the Sync Gate, proceed as follows:

1. Make sure that variable components are adjusted properly in accordance with Volume I, Section 4.

2. Check supply voltage across decoupling capacitor C2. It should be 20 (±1) volts. If it is not, check decoupling network.

3. Check pin a for keying pulse input as shown in Fig. 8-13. If it is not present, refer to Paragraph 8.3 for corrective action.

4. Check pin Z for sync pulse input as shown in Fig. 8-13. If it is not present, refer to Paragraph 8.3 for corrective action.

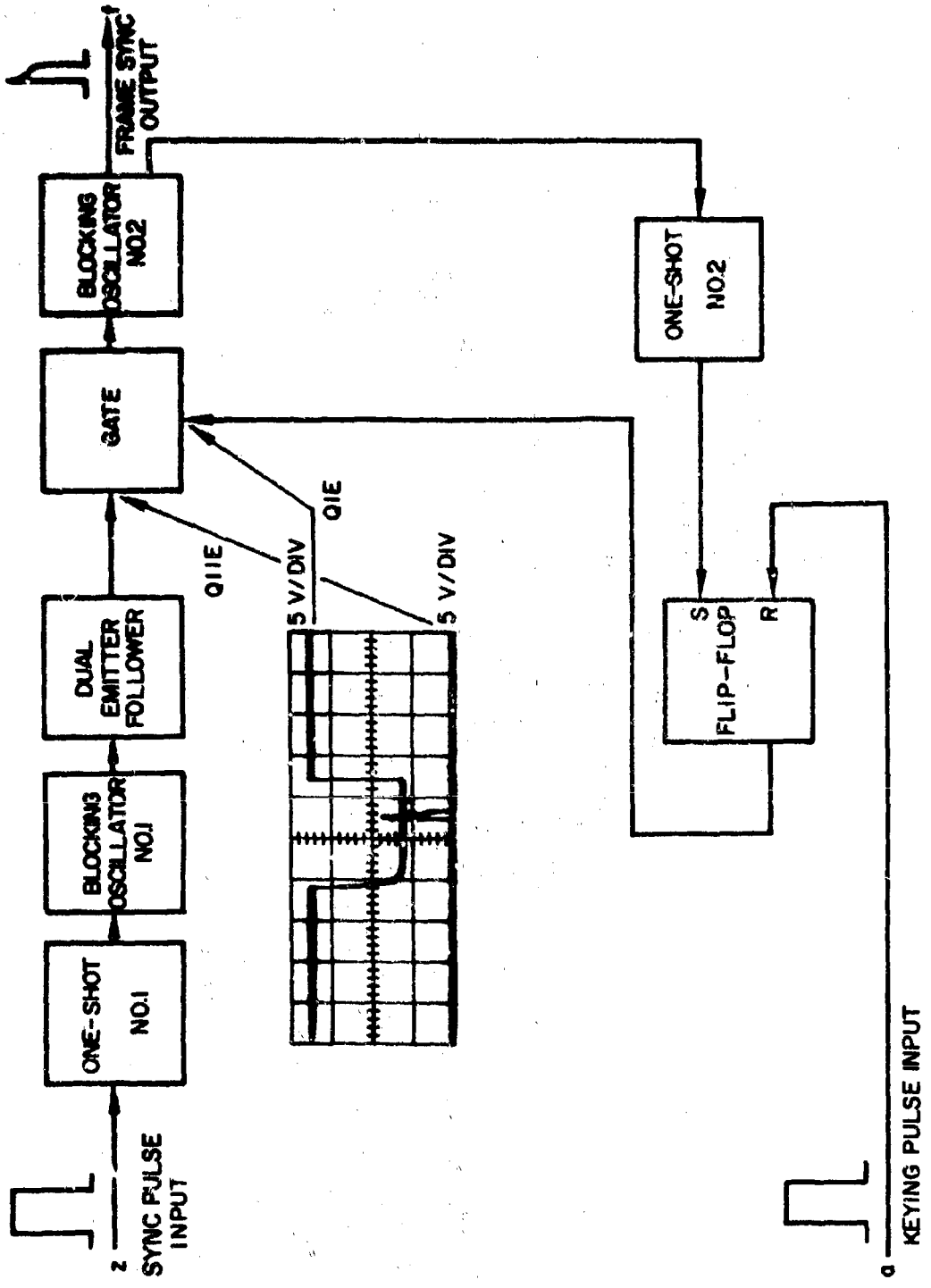


Fig. 8-13 Sync Gate Block Diagram

5. Check cathode of diode CR1. Its output should be a positive spike that is in time phase with the input at pin Z. If it is not, capacitor C1 or C3, diode CR1, or resistor R1 is faulty.

6. Check collector of transistor Q4. Its output should be a waveform that starts at +18 (±2) volts and falls off exponentially to +4 (±2) volts; it should then return to +18 (±2) volts with a rise time of less than 2 microseconds. There should be a nominal delay of from 5 to 10 microseconds between the positive-going portions of the waveforms on pin z and the collector of transistor Q4. If not, one-shot no. 1 is faulty. Refer to Paragraph 8.4.2 for corrective action.

7. Check voltage of terminal 2 of transformer T1. It should be a positive blocking oscillator pulse of 7 (±2) volts. If it is not, blocking oscillator no. 1 is faulty. Refer to Paragraph 8.4.1 for corrective action.

8. Check emitter of transistor Q9. Its output should be a positive blocking oscillator pulse of 8 (±2) volts. If it is not, transistor Q9 or resistor R27 or R28 is faulty.

9. Check emitter of transistor Q11. Its output should be as shown in Fig. 8-13. If it is not, transistor Q11 or resistor R32 or R33 is faulty.

10. Check the following points in the circuitry.

NOTE: The waveforms at the following points are interrelated. If one is incorrect, all will probably be incorrect. For normal operation, the waveforms should be as given in steps 10a through 10e.

a. Collector of transistor Q8: Waveform should start at +18 (±2) volts and fall off exponentially to +4 (±2) volts; it should then return to +18 (±2) volts with a rise time of less than 2 microseconds.

b. Collector of transistor Q3: Waveform should be as shown in Fig. 8-13 (Q1E). If it is not, one-shot no. 2 or the flip-flop is faulty. Refer to Paragraph 8.4.2 and 8.4.3, respectively, for corrective action.

c. Collector of transistor Q5: Waveform should be the complement of the waveform of Q1 as shown in Fig. 8-13 (Q1E). If it is not, the flip-flop is faulty. Refer to Paragraph 8.4.3 for corrective action.

d. Collector of transistor Q12: There should be a blocking oscillator pulse that is 2 (±2) volts high. If not, transistor Q12 or its associated components are faulty.

e. Pin f: Waveform should be as shown in Fig. 8-13. If it is not, blocking oscillator no. 2 is faulty. Refer to Paragraph 8.4.1 for corrective action.

8.26 ZERO DATA SELECTOR

The Zero Data Selector separates alternating zero data on Channel 1 from alternating sync information on Channel 1. A schematic diagram of the Zero Data Selector is in Fig. A-14; a block diagram is in Fig. 8-14. If there is trouble in the Zero Data Selector, do the procedures in Paragraph 8.2 and proceed as follows:

1. Check supply voltage across decoupling capacitors. It should be +20 (±1) volts across capacitor C2 and -20 (±1) volts across capacitor C1. If it is not, check decoupling networks.

2. Check cathode of diode CR5 for -10 (±1) volts. If it is not correct, check diode CR5 and/or resistor R3.

3. Check pin f for main frame sync pulses as shown in Fig. 8-14. If they are not present, refer to Paragraph 8.3 for corrective action.

4. Check pin d. Its output should be as shown for Q1E in Fig. 8-14. If it is not, refer to Paragraph 8.3 for corrective action.

5. Check emitter of transistor Q1. Its output should be as shown in Fig. 8-14. If it is not, transistor Q1 or resistor R4 is faulty.

6. Check collector of transistor Q2. Its output should be the same as that shown for Q4E on Fig. 8-14. If it is not, the flip-flop is faulty. Refer to Paragraph 8.4.3 for corrective action.

7. Check collector of transistor Q3. Its output should be the complement of the waveform shown for Q4E in Fig. 8-14. If it is not, the flip-flop is faulty. Refer to Paragraph 8.4.3 for corrective action.

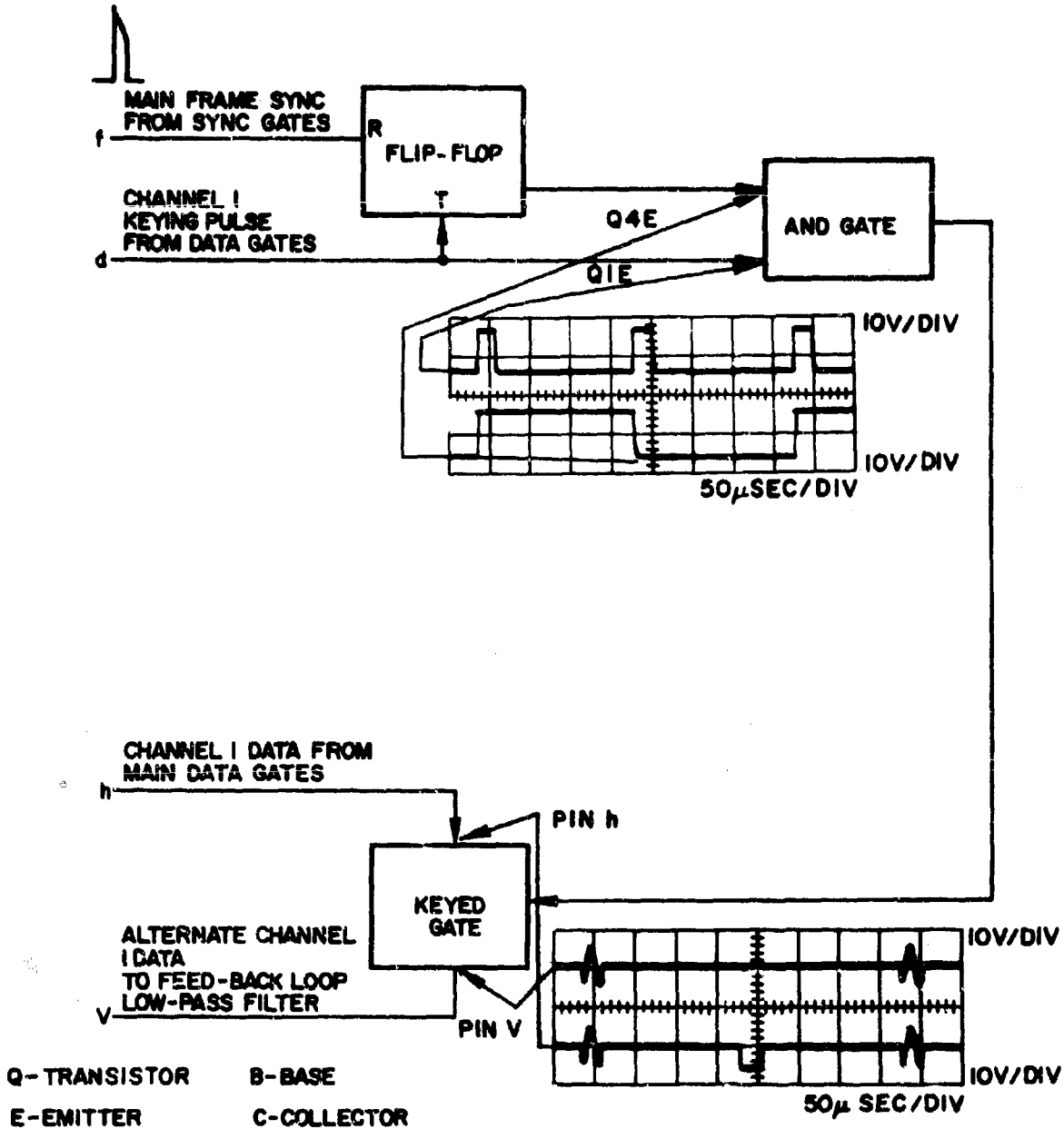


Fig. 8-14 Zero Data Selector Block Diagram

8. Check emitter of transistor Q4. Its output should be as shown in Fig. 8-14. If it is not, transistor Q4, resistor R21, or diode CR4 is faulty.

9. Check intersection of diode CR4, resistor R17, and resistor R16. Its output should be a rectangular pulse from -15 (±2) to -5 (±1) volts. These rectangular pulses should occur one-half as often as the pulses at the emitter of transistor Q1. If it is not, diode CR4, resistor R17, or resistor R16 is faulty.

10. Check collector of transistor Q7. Its output should be rectangular pulses that are going negative from +19 (±1) volts to -10 (±1) volts in phase with the signal at the intersection of CR4, R17, and R16. If it is not, transistor Q7 or resistor R13 or R16 is faulty.

11. Check pin h for the waveform shown in Fig. 8-14. If it is not correct, refer to Paragraph 8.3 for corrective action.

12. Check pin V for the waveform shown in Fig. 8-14. If it is not correct, transistor Q5 or Q6 or their associated components are faulty.

8.21 FREQUENCY DIVIDER

The Frequency Divider divides the Data Sync frequency by a factor of eight for Vibration and four for G-A. Schematic diagrams of the Frequency Divider are in Figs. A-15 and A-44; a block diagram is in Fig. 8-15. If there is trouble in either the Vibration or the G-A Frequency Divider, do the procedures in Paragraph 8.2 and proceed as follows:

1. Check supply voltage across decoupling capacitor C1. It should be -20 (±1) volts. If it is not, check decoupling network.

2. Check input at pin b. It should be as shown in Fig. 8-15. If it is not, refer to Paragraph 8.3 for corrective action.

3. Check collector of transistor Q1. Its output should be the same as that for pin j, as shown in Fig. 8-15. If it is not, flip-flop no. 1 is faulty. Refer to Paragraph 8.4.3 for corrective action.

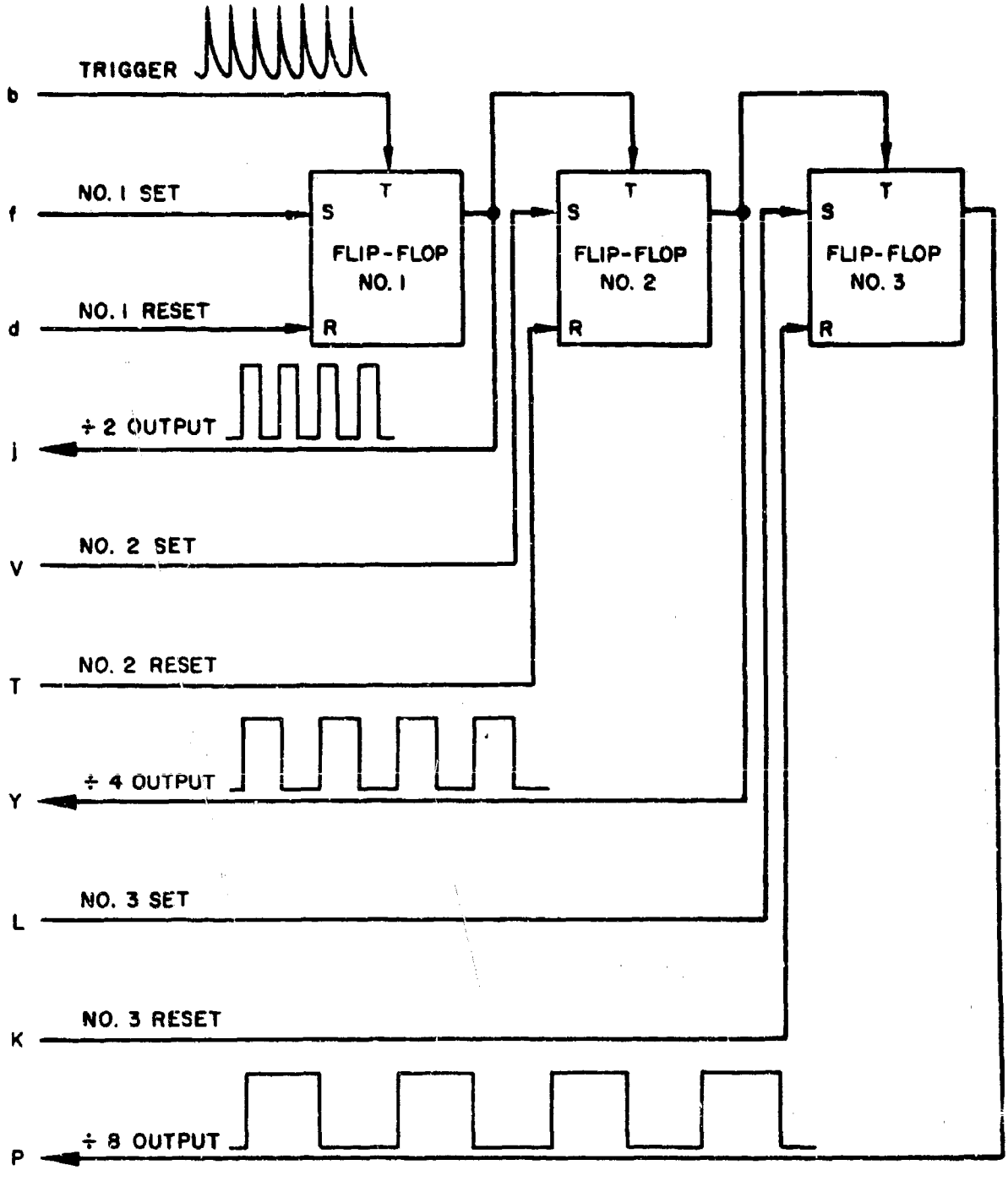


Fig. 8-15 Frequency Divider Block Diagram

4. Check collector of transistor Q4. Its output should be the same as that of pin Y, as shown in Fig. 8-15. If it is not, flip-flop no. 2 is faulty. Refer to Paragraph 8.4.3 for corrective action.

5. Check collector of transistor Q7. Its output should be the same as that of pin P, as shown in Fig. 8-15. If it is not, flip-flop no. 3 is faulty. Refer to Paragraph 8.4.3 for corrective action.

6. Check output at pin P. It should be as shown in Fig. 8-15. If it is not, transistor Q9 or resistor R34 is faulty.

8.22 EIGHT-CHANNEL PULSE SEQUENCER

The Eight-Channel Pulse Sequencer generates eight pulses on eight separate output lines in sequence from the clock pulse input. Schematic diagrams of the Eight-Channel Pulse Sequencer are in Figs. A-16 and A-45; a block diagram is in Fig. 8-16. If there is trouble in either the Vibration or G-A Eight-Channel Pulse Sequencer, do the procedures in Paragraph 8.2 and proceed as follows:

1. Check input voltage across decoupling capacitor C136. It should be -20 (±1) volts. If it is not, check decoupling network.

2. Check input at pin b. It should be as shown in Fig. 8-16. If it is not, refer to Paragraph 8.3 for corrective action.

3. Check collector of transistor Q102. Its output should be a square wave at one-half the trigger frequency. If it is not, the flip-flop is faulty. Refer to Paragraph 8.4.3 for corrective action.

4. Check collector of transistor Q101. Its output should be a square wave at one-half the trigger frequency and opposite in phase to the signal in Step 3. If it is not, flip-flop no. 1 is faulty. Refer to Paragraph 8.4.3 for corrective action.

5. Check collector of transistor Q104. Its output should be a square wave at one-fourth the trigger frequency.

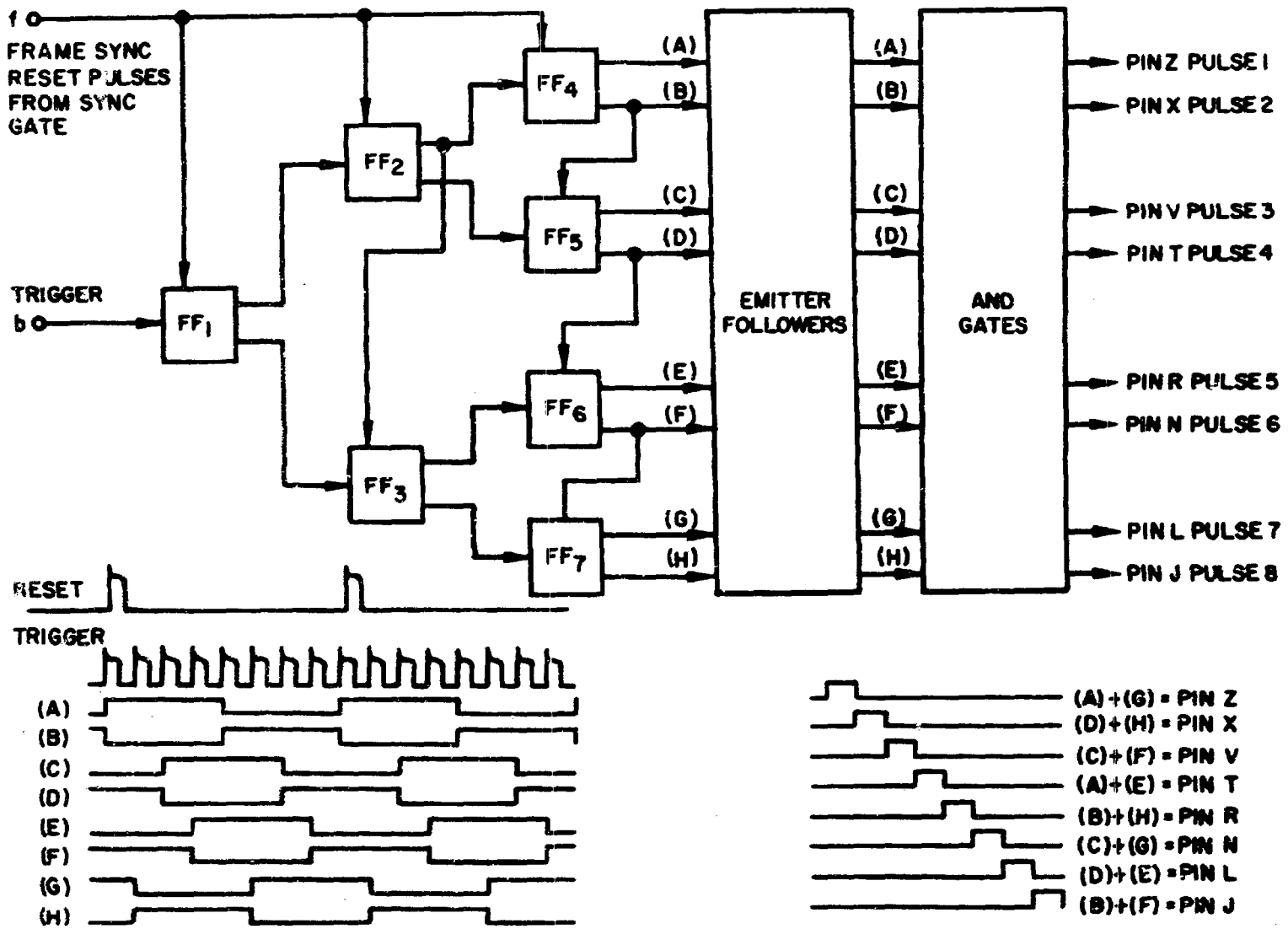


Fig. 8-16 Eight-Channel Pulse Sequencer Block Diagram

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6. Check collector of transistor Q103. Its output should be a square wave at one-fourth the trigger frequency and opposite in phase to the signal in Step 5. If it is not, flip-flop no. 2 is faulty. Refer to Paragraph 8.4.3 for corrective action.

7. Check collector of transistor Q110. Its output should be a square wave at one-fourth the trigger frequency.

8. Check collector of transistor Q109. Its output should be a square wave at one-fourth the trigger frequency and opposite in phase to the signal in Step 7. If it is not, flip-flop no. 3 is faulty. Refer to Paragraph 8.4.3 for corrective action.

9. Check collector of transistor Q108. Its output should be as shown in Fig. 8-16, Note (A).

10. Check collector of transistor Q107. Its output should be as shown in Fig. 8-16, Note (B). If it is not, flip-flop no. 4 is faulty. Refer to Paragraph 8.4.3 for corrective action.

11. Check collector of transistor Q106. Its output should be as shown in Fig. 8-16, Note (C).

12. Check collector of transistor Q105. Its output should be as shown in Fig. 8-16, Note (D). If it is not, flip-flop no. 5 is faulty. Refer to Paragraph 8.4.3 for corrective action.

13. Check collector of transistor Q112. Its output should be as shown in Fig. 8-16, Note (E).

14. Check collector of transistor Q111. Its output should be as shown in Fig. 8-16, Note (F). If it is not, flip-flop no. 6 is faulty. Refer to Paragraph 8.4.3 for corrective action.

15. Check collector of transistor Q114. Its output should be as shown in Fig. 8-16, Note (G).

16. Check collector of transistor Q113. Its output should be as shown in Fig. 8-16, Note (H). If it is not, flip flop no. 7 is faulty. Refer to Paragraph 8.4.3 for corrective action.

17. Check emitter of transistor Q115. Its output should be as shown in Fig. 8-16, Note (A). If it is not, transistor Q115 or resistor R165 is faulty.

18. Check emitter of transistor Q116. Its output should be as shown in Fig. 8-16, Note (B). If it is not, transistor Q116 or resistor R166 is faulty.

19. Check emitter of transistor Q117. Its output should be as shown in Fig. 8-16, Note (C). If it is not, transistor Q117 or resistor R167 is faulty.

20. Check emitter of transistor Q118. Its output should be as shown in Fig. 8-16, Note (D). If it is not, transistor Q118 or resistor R168 is faulty.

21. Check emitter of transistor Q119. Its output should be as shown in Fig. 8-16, Note (E). If it is not, transistor Q119 or resistor R169 is faulty.

22. Check emitter of transistor Q120. Its output should be as shown in Fig. 8-16, Note (F). If it is not, transistor Q120 or resistor R170 is faulty.

23. Check emitter of transistor Q121. Its output should be as shown in Fig. 8-16, Note (G). If it is not, transistor Q121 or resistor R171 is faulty.

24. Check emitter of transistor Q122. Its output should be as shown in Fig. 8-16, Note (H). If it is not, transistor Q122 or resistor R172 is faulty.

25. Check output at pin Z. It should be as shown in Fig. 8-13. If it is not, diode CR130 or CR122 or resistor R182 is faulty.

26. Check output at pin X. It should be as shown in Fig. 8-16. If it is not, diode CR131 or CR123 or resistor R183 is faulty.

27. Check output at pin V. It should be as shown in Fig. 8-16. If it is not, diode CR132 or CR124 or resistor R184 is faulty.

28. Check output at pin T. It should be as shown in Fig. 8-16. If it is not, diode CR133 or CR125 or resistor R185 is faulty.

29. Check output at pin R. It should be as shown in Fig. 8-16. If it is not, diode CR134 or CR126 or resistor R186 is faulty.

30. Check output at pin N. It should be as shown in Fig. 8-16. If it is not, diode CR135 or CR127 or resistor R187 is faulty.

31. Check output at pin L. It should be as shown in Fig. 8-16. If it is not, diode CR140 or CR128 or resistor R188 is faulty.

32. Check output at pin J. It should be as shown in Fig. 8-16. If it is not, diode CR150 or CR129 or resistor R189 is faulty.

8.23 MATRIX

The Matrix contains eight AND gates for ANDing keying signals. A schematic diagram of the Matrix is in Fig. A-46; a block diagram is in Fig. 8-17. If there is trouble in the Matrix, do the procedures in Paragraph 8.2 and proceed as follows:

1. Check input voltage across decoupling capacitor C1. It should be -20 (±1) volts. If it is not, check decoupling network.

2. Check output at pin k. It should be as shown in Fig. 8-17. If it is not, check inputs at pins j and z, as shown in Fig. 8-17.

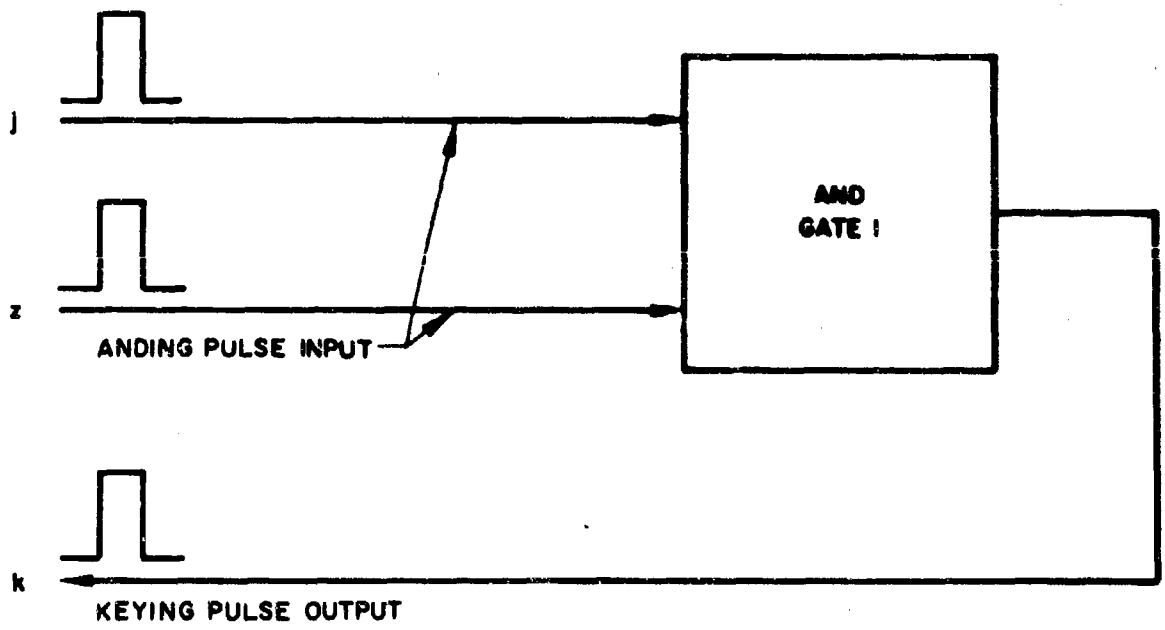


Fig. 8-17 Matrix Block Diagram (Typical Element)

3. Check emitter of transistor Q1. Its output should be the same as that at pin j, as shown in Fig. 8-17. If it is not, transistor Q1 or resistor R3 is faulty.

4. Check emitter of transistor Q2. Its output should be the same as that at pin z, as shown in Fig. 8-17. If it is not, transistor Q2 or resistor R5 is probably faulty. If they are found to be operating properly, diode CR1 or CR2 or resistor R6 is faulty.

5. Repeat Steps 2 through 4 for each gate, keeping in mind that the component numbers and pin letters are different for each gate.

6. If the preceding steps do not isolate the trouble, checking wiring continuity, capacitors for shorts, solder points, and resistances.

8.24 DATA GATES

The Data Gates sample the PAM composite pulse train and divide it into eight different outputs for delivery to the display electronics. Schematic diagrams of the Data Gates are in Figs. A-17 and A-47. A block diagram is in Fig. 8-18. If there is trouble in the Data Gates, do the procedures in Paragraph 8.2 and proceed as follows:

1. Check input voltage across decoupling capacitors. It should be +20 (±1) volts across capacitor C1 and -20 (±1) volts across capacitor C2. Check intersection of diode CR1 and resistor R17. It should be -10 (±1) volts. If it is not, check decoupling networks.

2. Check input at pin H. It should be the composite PAM pulse train from the Gate Driver Amplifier.

3. Check input at pin Z. It should be as shown in Fig. 8-18. If it is not, refer to Paragraph 8.3 for corrective action.

4. Check emitter of transistor Q3. It should be the same as pin Z, as shown in Fig. 8-18. If it is not, transistor Q3 or resistor R18 is faulty.

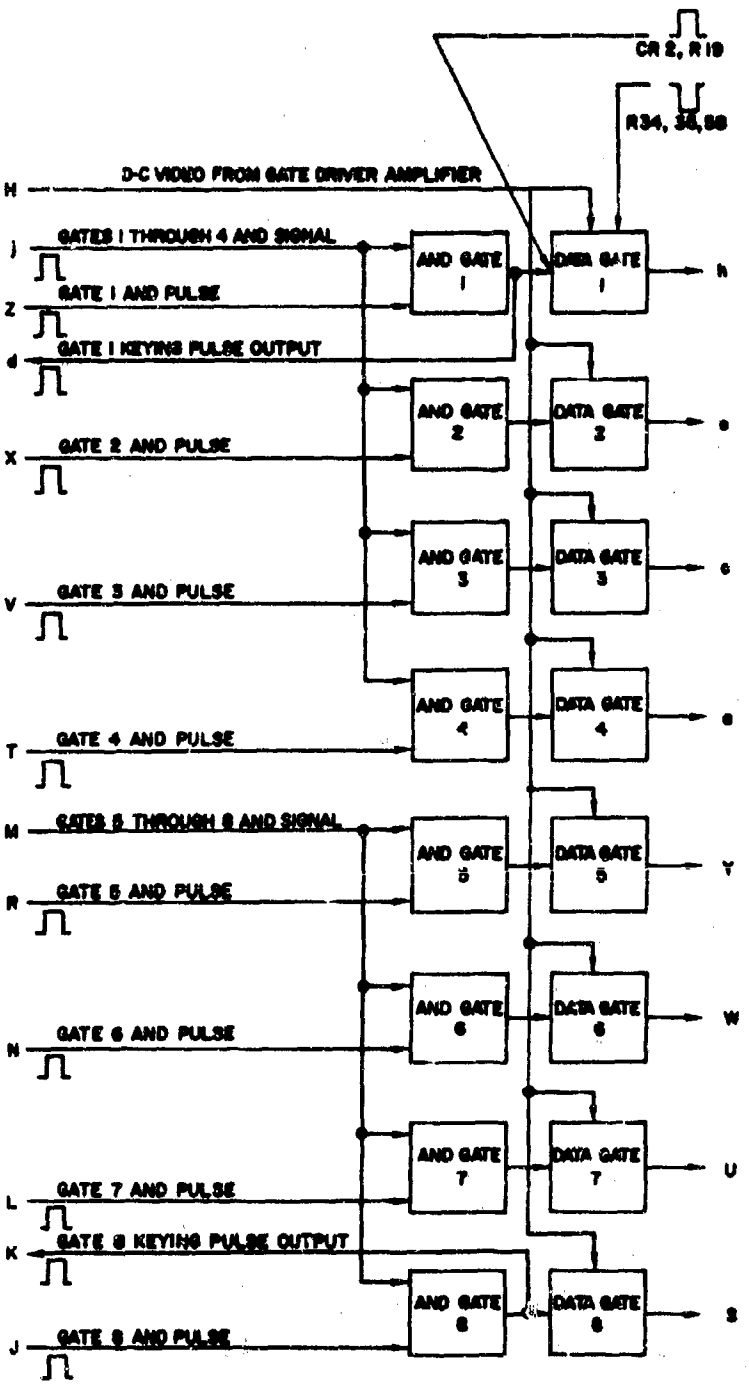


Fig. 8-18 Data Gates Block Diagram

5. Check input at pin X. It should be as shown in Fig. 8-18. If it is not, refer to Paragraph 8.3 for corrective action.

6. Check emitter of transistor Q4. It should be the same as pin X, as shown in Fig. 8-18. If it is not, transistor Q4 or resistor R20 is faulty.

7. Check input at pin V. It should be as shown in Fig. 8-18. If it is not, refer to Paragraph 8.3 for corrective action.

8. Check emitter of transistor Q5. It should be the same as pin V, as shown in Fig. 8-18. If it is not, transistor Q5 or resistor R22 is faulty.

9. Check input at pin T. It should be as shown in Fig. 8-18. If it is not, refer to Paragraph 8.3 for corrective action.

10. Check emitter of transistor Q6. It should be the same as pin T, as shown in Fig. 8-18. If it is not, transistor Q6 or resistor R24 is faulty.

11. Check input at pin R. It should be as shown in Fig. 8-18. If it is not, refer to Paragraph 8.3 for corrective action.

12. Check emitter of transistor Q8. It should be the same as pin R, as shown in Fig. 8-18. If it is not, transistor Q8 or resistor R27 is faulty.

13. Check input at pin N. It should be as shown in Fig. 8-18. If it is not, refer to Paragraph 8.3 for corrective action.

14. Check emitter of transistor Q9. It should be the same as pin N, as shown in Fig. 8-18. If it is not, transistor Q9 or resistor R29 is faulty.

15. Check input at pin L. It should be as shown in Fig. 8-18. If it is not, refer to Paragraph 8.3 for corrective action.

16. Check emitter of transistor Q10. It should be the same as pin L. If it is not, transistor Q10 or resistor R31 is faulty.

17. Check input at pin J. It should be as shown in Fig. 8-18. If it is not, refer to Paragraph 8.3 for corrective action.

18. Check emitter of transistor Q11. It should be the same as pin J. If it is not, transistor Q11 or resistor R33 is faulty.

19. Check emitter of transistor Q2. Its output should be the same as the input on pin J, which is either a 0 dc level or a positive pulse from -15 (±3) volts to -7 (±2) volts. If it is not, transistor Q2 or resistor R3 is faulty.

20. Check intersection of diode CR2 and resistor R19. Its output should be a positive pulse from -15 (±3) volts to -7 (±2) volts. If it is not, diode CR2 or resistor R19 is faulty.

21. Check intersection of diode CR3 and resistor R21. Its output should be a positive pulse from -15 (±3) volts to -7 (±2) volts. If it is not, diode CR3 or resistor R21 is faulty.

22. Check intersection of diode CR4 and resistor R23. Its output should be a positive pulse from -15 (±2) volts to -7 (±2) volts. If it is not, diode CR4 or resistor R23 is faulty.

23. Check intersection of diode CR5 and resistor R25. Its output should be a positive pulse from -15 (±2) volts to -7 (±2) volts. If it is not, diode CR5 or resistor R25 is faulty.

24. Check intersection of diode CR6 and resistor R26. Its output should be a positive pulse from -15 (±2) volts to -7 (±2) volts. If it is not, diode CR6 or resistor R26 is faulty.

25. Check intersection of diode CR7 and resistor R28. Its output should be a positive pulse from -15 (±2) volts to -7 (±2) volts. If it is not, diode CR7 or resistor R28 is faulty.

26. Check intersection of diode CR8 and resistor R30. Its output should be a positive pulse of from -15 (±2) volts to -7 (±2) volts. If it is not, diode CR8 or resistor R30 is faulty.

27. Check intersection of diode CR9 and resistor R32. Its output should be a positive pulse of from -15 (±2) volts to -7 (±2) volts. If it is not, diode CR9 or resistor R32 is faulty.

28. Check output at pin d. It should be as shown in Fig. 8-18. If it is not, transistor Q1 or resistor R16 is faulty.

29. Check output at pin K. It should be as shown in Fig. 8-18. If it is not, transistor Q12 or resistor R15 is faulty

30. Check output at pin h. It should be the composite PAM pulse train from the Gate Driver Amplifier whenever keying signals on pins Z and j coincide; otherwise, it should be 0. If it is not, check collector of transistor Q21. Its output should be a negative-going signal between +10 (±1) volts and -10 (±1) volts. If it is, transistor Q13 or Q29 is faulty. If it is not, transistor Q21 is faulty.

31. Check output at pin e. It should be the composite PAM pulse train whenever keying signals on pins X and j coincide; otherwise, it should be 0. If it is not, check collector of transistor Q22. Its output should be a negative-going signal between +10 (±1) volts and -10 (+1) volts. If it is, transistor Q14 or Q30 is faulty. If it is not, transistor Q22 is faulty.

32. Check output at pin c. It should be the composite PAM pulse train whenever keying signals on pins V and j coincide; otherwise, it should be 0. If it is not, check collector of transistor Q23. Its output should be a negative-going signal between +10 (±1) volts and -10 (±1) volts. If it is, transistor Q15 or Q31 is faulty. If it is not, transistor Q23 is faulty.

33. Check output at pin a. It should be the composite PAM pulse train whenever keying signals on pins T and j coincide; otherwise, it should be 0. If it is not, check collector of transistor Q24. Its output should be a negative-going signal between +10 (±1) volts and -10 (±1) volts. If it is, transistor Q16 or Q32 is faulty. If it is not, transistor Q24 is faulty.

34. Check output at pin Y. It should be the composite PAM pulse train whenever keying signals on pins R and M coincide; other wise it should be 0. If it is not, check collector of transistor Q25. Its output should be a negative-going signal between +10 (±1) volts and -10 (±1) volts. If it is, transistor Q17 or Q33 is faulty. If it is not, transistor Q25 is faulty.

35. Check output at pin W. It should be the composite PAM pulse train whenever keying signals on pins N and M coincide; otherwise, it should be 0. If it is not, check collector of transistor Q26. Its output should be a negative-going signal between +10 (±1) volts and -10 (±1) volts. If it is, transistor Q18 or Q34 is faulty. If it is not, transistor Q26 is faulty.

36. Check output at pin U. It should be the composite PAM pulse train whenever keying signals on pins L and M coincide; otherwise, it should be 0. If it is not, check collector of transistor Q27. Its output should be a negative-going signal between +10 (±1) volts and -10 (±1) volts. If it is, transistor Q19 or Q35 is faulty. If it is not, transistor Q27 is faulty.

37. Check output at pin S. It should be the composite PAM pulse train whenever keying signals on pins J and M coincide; otherwise, it should be 0. If it is not, check collector of transistor Q28. Its output should be a negative-going signal between +10 (±1) volts and -10 (±1) volts. If it is, transistor Q20 or Q36 is faulty. If it is not, transistor Q28 is faulty.

8.25 PULSE SET

The Pulse Set board generates trigger pulses for the different pulse sequencers. A schematic diagram of the Pulse Set board is in Fig. A-48; a block diagram is in Fig. 8-19. If there is trouble in the Pulse Set board, do the procedures in Paragraph 8.2 and proceed as follows:

1. Make sure that variable components are adjusted in accordance with procedures in Volume I, Section 4.

2. Check input voltage across decoupling capacitors. It should be -20 (±1) volts across capacitor C12 and +20 (±1) volts across capacitor C13. If it is not, check decoupling networks. Check for presence of -10 (±1) volts at the cathode of diode CR7. If it is not, diode CR7 or resistor R25 is faulty. Check for presence of -10 (±1) volts at cathode of diode CR14. If it is not, diode CR7 or resistor R33 is faulty.

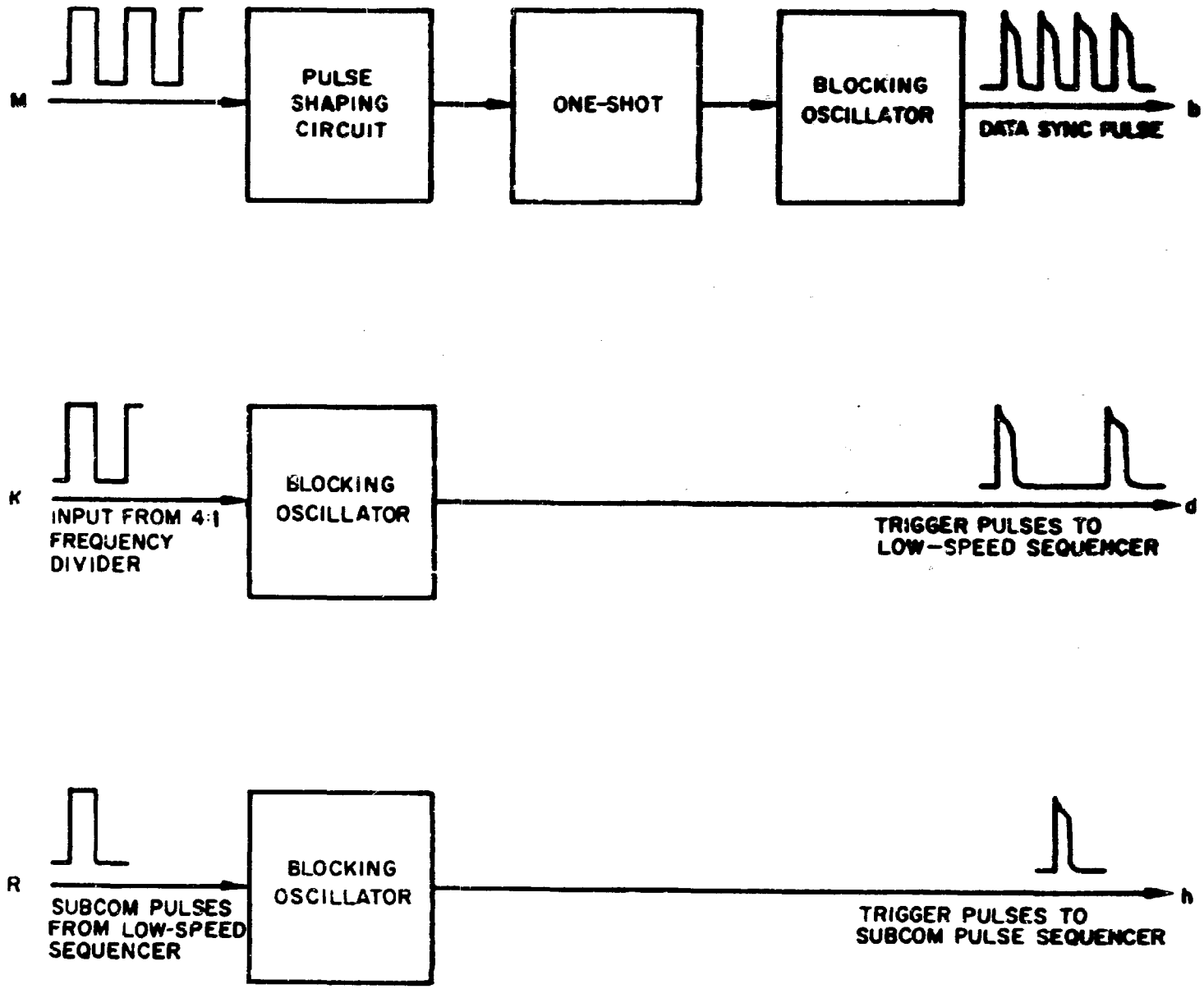


Fig. 8-19 Pulse Set Block Diagram

3. Check input at pin M. It should be as shown in Fig. 8-19. If it is not, refer to Paragraph 8.2 for corrective action.

4. Check emitter of transistor Q1. Its output should be the same as that of pin M, as shown in Fig. 8-19. If it is not, transistor Q1 or resistor R5 is faulty.

5. Check collector of transistor Q2. It should be a square wave of +19 (±1) volts amplitude. If it is not, transistor Q2, resistors R1 or R2, diode CR1, or capacitor C1 is faulty.

6. Check emitter of transistor Q3. Its output should be a square wave of 19 (±1) volts amplitude. If it is not, transistor Q3 or resistor R6 is faulty.

7. Check cathode of diode CR2. Its output should be positive spikes of approximately 10 volts amplitude. If it is not, diode CR2, capacitor C2 or C3, or resistor R7 is faulty.

8. Check collector of transistor Q5. Its output should be a negative pulse from +17 (±3) volts falling off exponentially to +3 (±2) volts and rising to +17 (±3) volts in less than 2 microseconds. If it is not, the one-shot is faulty. Refer to Paragraph 8.4.2 for corrective action.

9. Check emitter of transistor Q6. Its output should be a positive spike of approximately 10 volts amplitude. If it is not, transistor Q6, resistor R13 or R14, or capacitor C6 is faulty.

10. Check output at pin b. It should be as shown in Fig. 8-19. If it is not, the blocking oscillator is faulty. Refer to Paragraph 8.4.1 for corrective action.

11. Check input at pin K. It should be as shown in Fig. 8-19. If it is not, refer to Paragraph 8.3 for corrective action.

12. Check emitter of transistor Q9. Its output should be the same as that for pin K, as shown in Fig. 8-19. If it is not, transistor Q9 or resistor R23 is faulty.

13. Check output at pin d. It should be as shown in Fig. 8-19. If it is not, the blocking oscillator is faulty. Refer to Paragraph 8.4.1 for corrective action.

14. Check input at pin R. It should be as shown in Fig. 8-19. If it is not, refer to Paragraph 8.3 for corrective action.

15. Check emitter of transistor Q12. Its output should be the same as that for pin R. If it is not, transistor Q12 or resistor R32 is faulty.

16. Check output at pin h. It should be as shown in Fig. 8-19. If it is not, refer to Paragraph 8.3 for corrective action.

8.26 DUTY CYCLE II

The Duty Cycle II board shapes the keying pulses that are delivered to the Sample and Hold board. A schematic diagram of the Duty Cycle II board is in Fig. A-49; a block diagram is in Fig. 8-20. If there is trouble in the Duty Cycle II board, do the procedures in Paragraph 8.2 and proceed as follows:

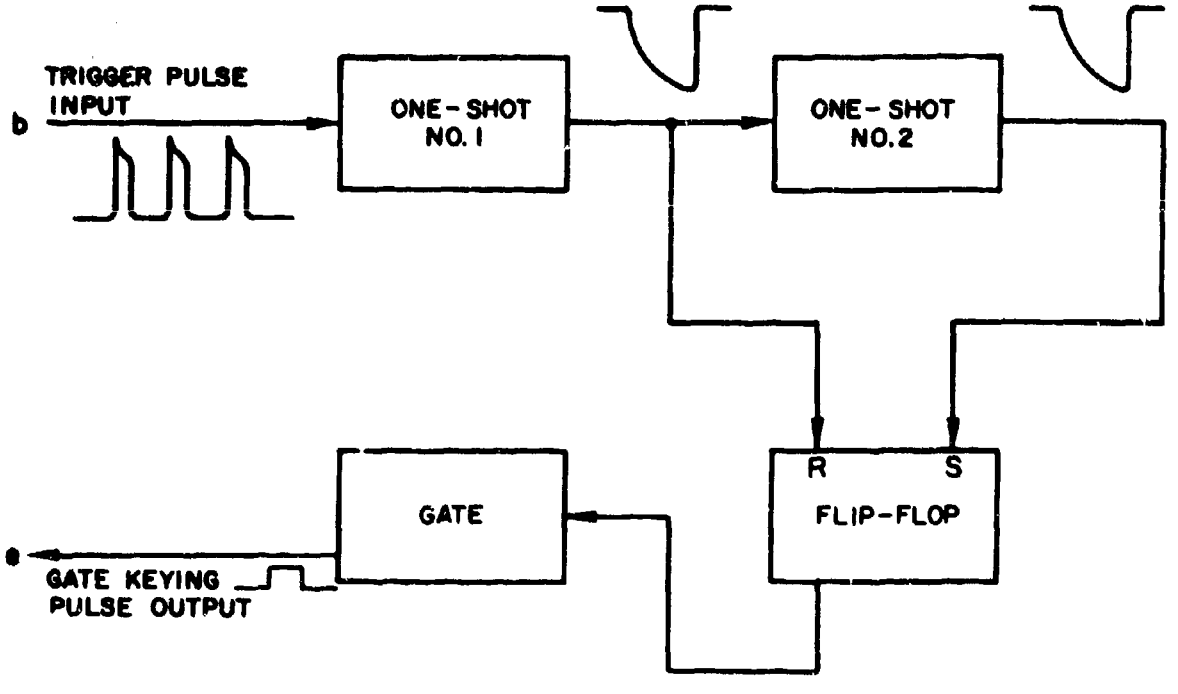


Fig. 8-20 Duty Cycle II Block Diagram

1. Make sure that variable components are adjusted in accordance with Volume I, Section 4.

2. Check the following dc voltages where indicated: -20 (±1) volts across capacitor C2, +20 (±1) volts across C16, -10 (±1) volts at cathode of CR5. If they are incorrect, check associated decoupling networks and components.

3. Check input at pin b. It should be as shown in Fig. 8-20. If it is not, refer to Paragraph 8.3 for corrective action.

4. Check collector of transistor Q2. Its output should be the one-shot output, as shown in Fig. 8-20. If it is not, one-shot no. 1 is faulty. Refer to Paragraph 8.4.2 for corrective action.

5. Check emitter of transistor Q3. Its output should be a positive pulse rising from approximately 10 volts to -19 (±1) volts with a sharp rise time and decaying exponentially to -19 (±1) volts. If it is not, transistor Q3, resistor R11 or R12, or capacitor C6 is faulty.

6. Check emitter of transistor Q4. Its output should be the same as that of transistor Q3 given in Step 5. If it is not, transistor Q4 or resistor R13 is faulty.

7. Check collector of transistor Q6. Its output should be the output shown for one-shot no. 2 in Fig. 8-20. If it is not, the one-shot is faulty. Refer to Paragraph 8.4.2 for corrective action.

8. Check emitter of transistor Q7. Its output should be the same as that of transistor Q3 given in Step 5. If it is not, transistor Q7, resistor R22 or R23, or capacitor C10 is faulty.

9. Check collector of transistor Q8. Its output should be the same as the output at pin e, as shown in Fig. 8-20. Check collector of transistor Q9. Its output should be the complement of the output at pin e. If the correct outputs at these two points are not present, the flip-flop is faulty. Refer to Paragraph 8.4.3 for corrective action.

10. Check output at pin e. It should be as shown in Fig. 8-20. If it is not, transistor Q10 or resistor R33 is faulty.

8.27 DATA SYNC DELAY RECORD

Data Sync Delay Record generates, from clock pulses received from the Data Sync Separator, the Datrac command pulse that is in phase with the composite PAM pulse train. Schematic diagrams of the Data Sync Delay Record board are in Figs. A-18 and A-51. A block diagram is in Fig. 8-21. If there is trouble in the Data Sync Delay Record board, do the procedures in Paragraph 8.2 and proceed as follows:

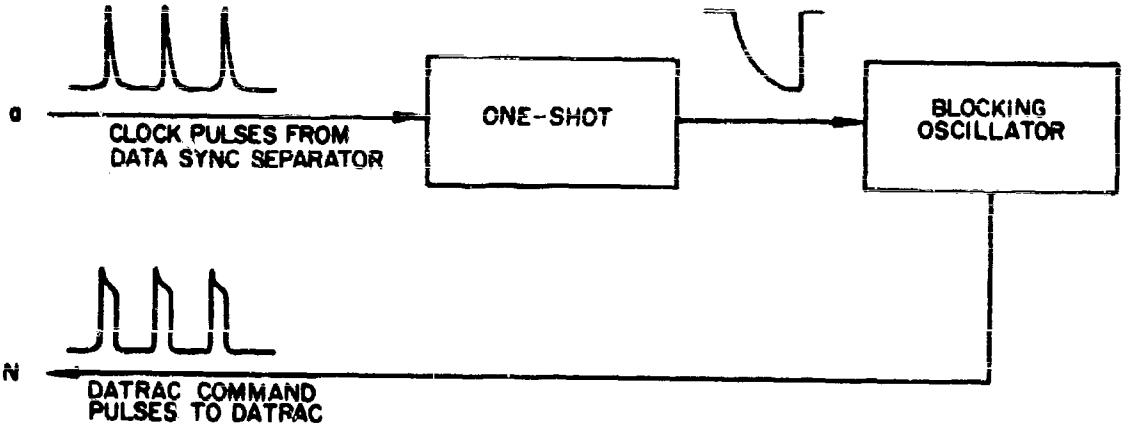


Fig. 8-21 Data Sync Delay Record Block Diagram

1. Make sure that variable components are adjusted in accordance with procedures in Volume I, Section 4.

2. Check input voltage across decoupling capacitors. It should be +20 (±1) volts across capacitor C1 and -20 (±1) volts across capacitor C3. If it is not, check decoupling networks.

3. Check input at pin a. It should be as shown in Fig. 8-21. If it is not, refer to Paragraph 8.3 for corrective action.

4. Check emitter of transistor Q1. Its output should be the same as the input at pin a. If it is not, transistor Q1 or resistor R2 or R3 is faulty.

5. Check collector of transistor Q3. It should be the one-shot output shown on Fig. 8-21. If it is not, refer to Paragraph 8.4.2 for corrective action.

6. Check output at pin N. It should be as shown in Fig. 8-21. If it is not, the blocking oscillator is faulty. Refer to Paragraph 8.4.1 for corrective action.

8.28 FILTER BOARD

The Filter Board (interpolation filter) separates modulation frequencies and blocks keying components from the PAM pulses from the Data Gates. The resulting output is smoothed data that corresponds to pulse modulation. A schematic diagram of the Filter Board is in Fig. A-19. If trouble is suspected, i.e., if there is a modulated pulse train on the Filter Board input and no smoothed data output, make continuity checks on the filter with the board removed from the station.

1. With an ohmmeter, check the continuity between pins N and H. It should be 10 K ($\pm$10%). If it is not, check continuity from "OUT" to "IN" on filter. It should be less than 200 ohms. If it is not, replace filter. If it is, resistor R21 or the wiring is faulty.

2. With an ohmmeter, check the continuity between pin N and "GRD." It should be greater than 9 K. If it is not, the filter is shorted and must be replaced.

3. Check the second filter by repeating Steps 1 and 2.

8.29 SAMPLE AND HOLD

The Sample and Hold circuit samples the value of the demultiplexed signal (upon the arrival of a keying pulse from the Matrix) and holds this value until the next

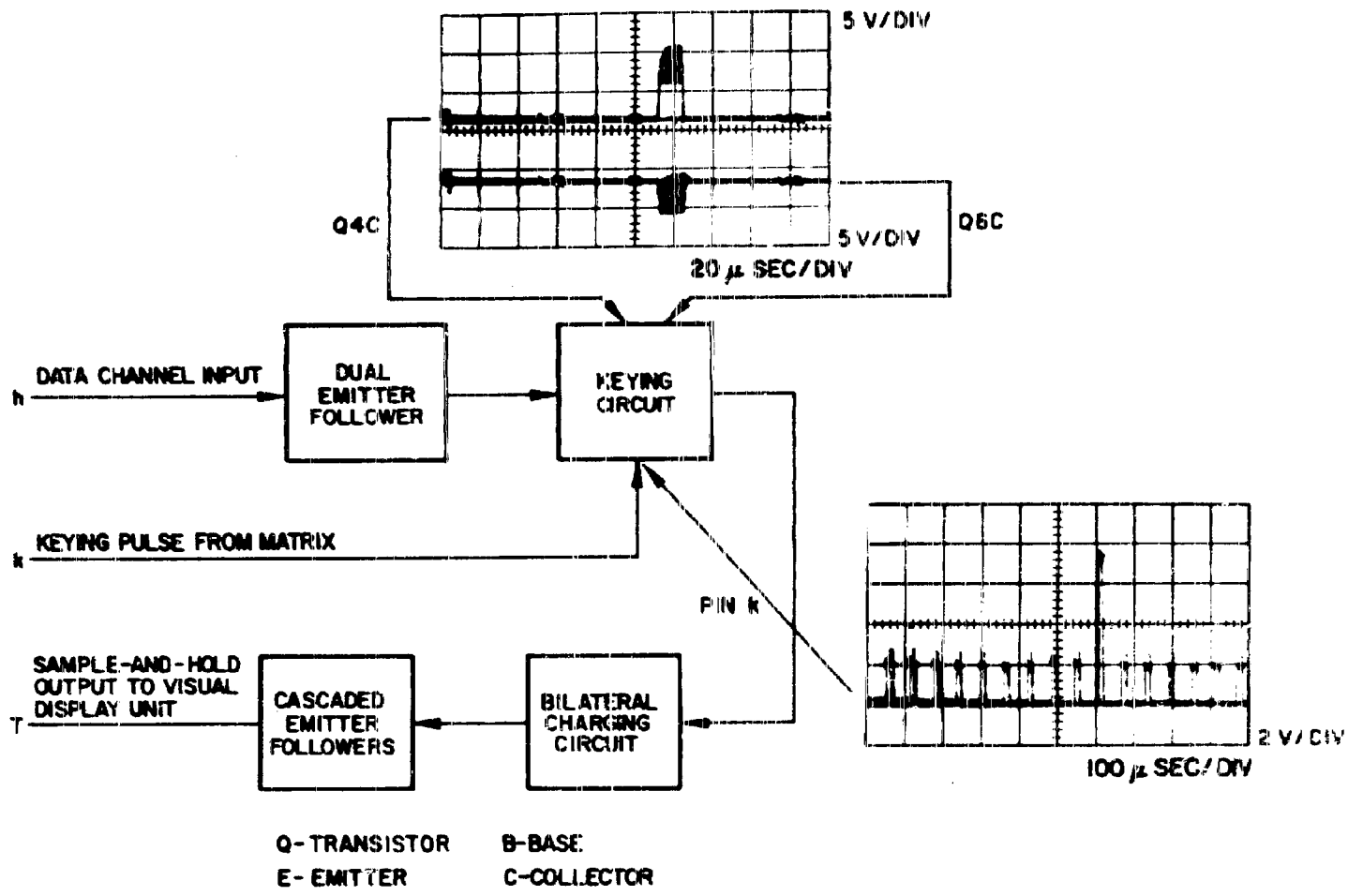


Fig. 8-22 Sample and Hold Block Diagram

demultiplexed pulse is sampled, at which time this next value is held. A schematic diagram of the Sample and Hold board is in Fig. A-63; a block diagram is in Fig. 8-22. If there is trouble in the Sample and Hold board, do the procedures in Paragraph 8.2 and proceed as follows:

1. Check supply voltages. They should be +20 (±1) volts at pin B, +10 (±1) volts at pin C, and -10 (±1) volts at pin E.

2. Check input at pin k. It should be as shown in Fig. 8-22. If it is not, refer to Paragraph 8.3 for corrective action.

3. Check collector of transistor Q3. Its output should be -10 (±2) volts with the baseline at +3 (±2) volts. If it is not, transistor Q3, Q4, or Q5 or resistor R2, R4, R6, R7, or R9 is faulty.

4. Check collector of transistor Q4. Its output should be as shown in Fig. 8-22. If it is not, transistor Q4 or resistor R1, R5, R6, or R9 is faulty.

5. Check collector of transistor Q6. Its output should be as shown in Fig. 8-22. If it is not, transistor Q5 or Q6 or resistor R3, R7, R8, R10, or R11 is faulty.

6. Check base of transistor Q9. Its output should be the sampled and held signal applied to pin h. If it is not, transistor Q1, Q2, Q7, or Q8, or associated components are faulty.

7. Check output at pin T. It should be the same as the output at the base of transistor Q9, in Step 6. If it is not, transistor Q9, Q10, or Q11 or resistor R14 or R45 is faulty.

8. Repeat the same procedures for the remaining two similar circuits, keeping in mind that the component numbers and pin letters are the only differences.

8.30 DC REFERENCE FILTER

The DC Reference Filter inserts the correct DC reference level into the composite PAM pulse train for the display electronics. A schematic diagram of the DC

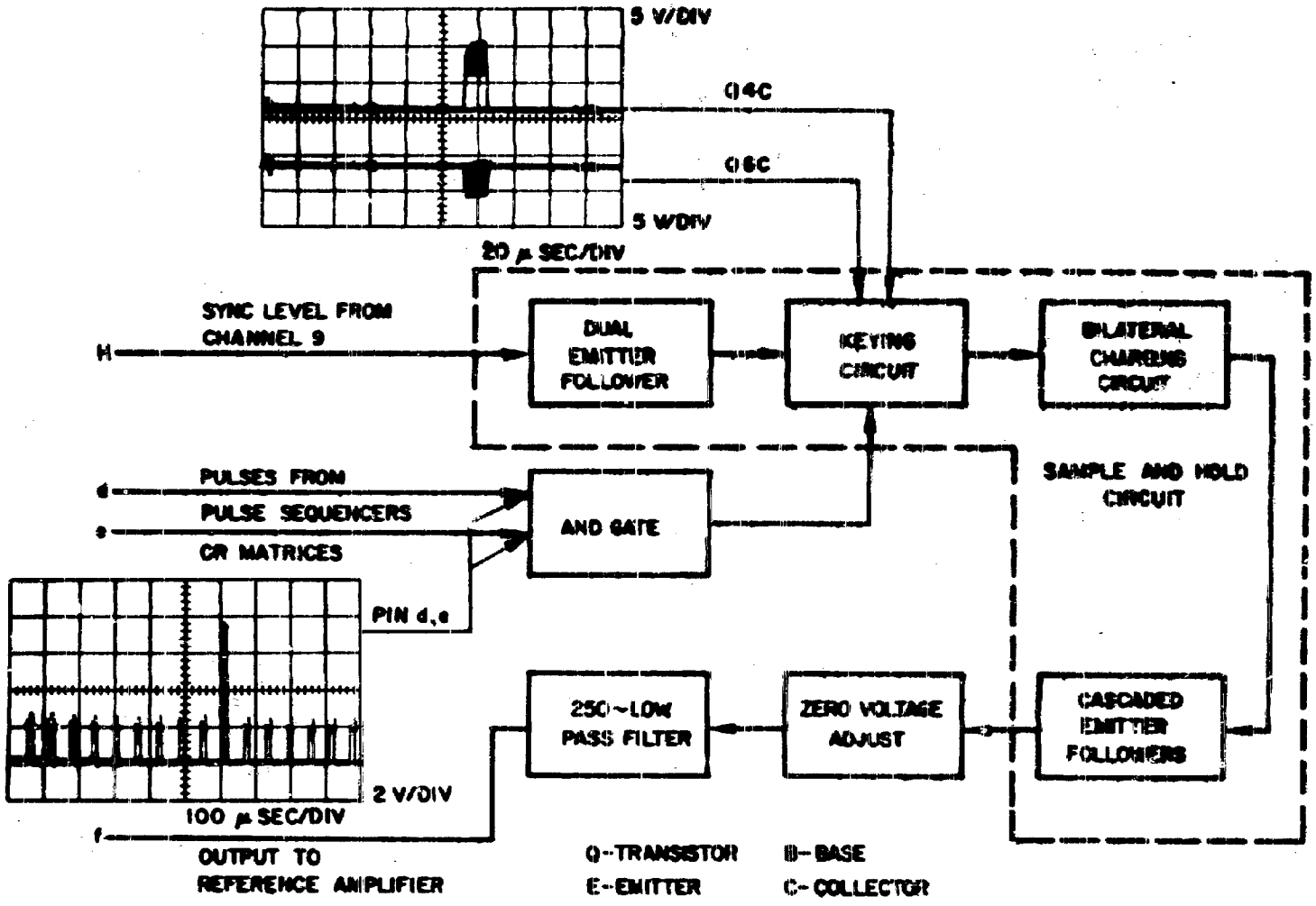


Fig. 8-23 DC Reference Filter Block Diagram

Reference Filter is in Fig. A-52; a block diagram is in Fig. 8-23. If there is trouble in the DC Reference Filter, do the procedures in Paragraph 8.2 and proceed as follows:

1. Make sure that variable components are adjusted properly in accordance with Volume I, Section 4.

2. Check supply voltages. There should be +10 (±2) volts at the anode of diode CR1. If there is not, diode CR1 or resistor R1 may be faulty. There should be -10 (±2) volts at the collector of diode CR2. If there is not, diode CR2 or resistor R2 may be faulty.

3. Check input at pin d. It should be as shown in Fig. 8-23. If it is not, refer to Paragraph 8.3 for corrective action.

4. Check intersection of diodes CR3 and CR4 and resistor R3. It should be the same as pin d, as shown in Fig. 8-24. If it is not, diode CR3 or CR4 or resistor R3 is faulty.

5. Check collector of transistor Q3. Its output should be a negative pulse of -10 (±2) volts with baseline at +3 (±2) volts. If it is not, transistor Q3, Q4, or Q5 or resistor R4, R7, R9, or R10 is faulty.

6. Check collector of transistor Q4. Its output should be as shown in Fig. 8-23. If it is not, transistor Q4 or resistor R5, R8, R9, or R12 is faulty.

7. Check collector of transistor Q6. Its output should be as shown in Fig. 8-23. If it is not, transistor Q5 or Q6 or resistor R6, R11, or R14 is faulty.

8. Check base of transistor Q9. Its output should be the sampled and held signal derived from the demultiplexed signal applied at pin H. If it is not, transistor Q1, Q2, Q7, or Q8 or their associated components are faulty.

9. Check emitter of transistor Q11. It should be the same as the output of the base of transistor Q9, as given in Step 8. If it is not, transistor Q9, Q10, or Q11 or resistor R17, R22, or R23 is faulty.

10. If the trouble has not been found, check filter as follows:

a. With board removed from station, check continuity from "IN" to "OUT." It should be less than 200 ohms. If it is not, replace filter.

b. Check continuity between "OUT" and "GND." It should be less than 10 K. If it is not, the filter is shorted and should be replaced.

8.31 FRAME SYNC STORAGE RECORD

The Frame Sync Storage Record board transforms the frame sync pulse train into the proper level for digital recording by the Digital Record Amplifier. A schematic diagram of the Frame Sync Storage Record board is in Fig. A-25; a block diagram is in Fig. 8-24. If there is trouble in the Frame Sync Storage Record Board, do the procedures in Paragraph 8.2 and proceed as follows:

1. Check supply voltage across decoupling capacitors. It should be 19 (±1) volts across capacitor C1 and -19 (±1) across C3. Check supply voltage across diode CR5. It should be 2 (±1) volts. If the voltages are not correct, check decoupling networks.

2. Check input at pin Z. It should be as shown in Fig. 8-24. The amplitude should be +15 (±1) volts with the base level at 0 (±1) volt. If it is not, refer to Paragraph 8.3 for corrective action.

3. Check collector of transistor Q1. Its output should be as shown in Fig. 8-24 If it is not, transistor Q1, resistor R3 or R2, or capacitor C2 is faulty.

4. Check input at pin T. It should be a positive-going pulse train, as shown in Fig. 8-24, at the clock frequency with an amplitude of +14 (±1) volts and the baseline at 0 (±1) volts.

5. Check intersection of capacitor C9 and resistor R17. The signal should be as shown in Fig. 8-24. If it is not correct, proceed as follows:

   a. Check emitter of transistor Q2. Its output should be as shown in Fig. 8-24 for pin T. If it is not, transistor Q2 is faulty.

6. Check output at pin K. It should be an asymetric square wave with levels of -5 (±1) and -15 (±3) volts. The negative swing should be in time phase with the leading edge of the pulses at the junction of capacitor C9 and resistor R17, as shown in Fig. 8-24. The positive swing should be in time with the leading edge of the pulses at the junction of capacitor C9 and resistor R17, as shown in Fig. 8-24. The positive swing should be in time with the leading edges of the pulses at pin Z.

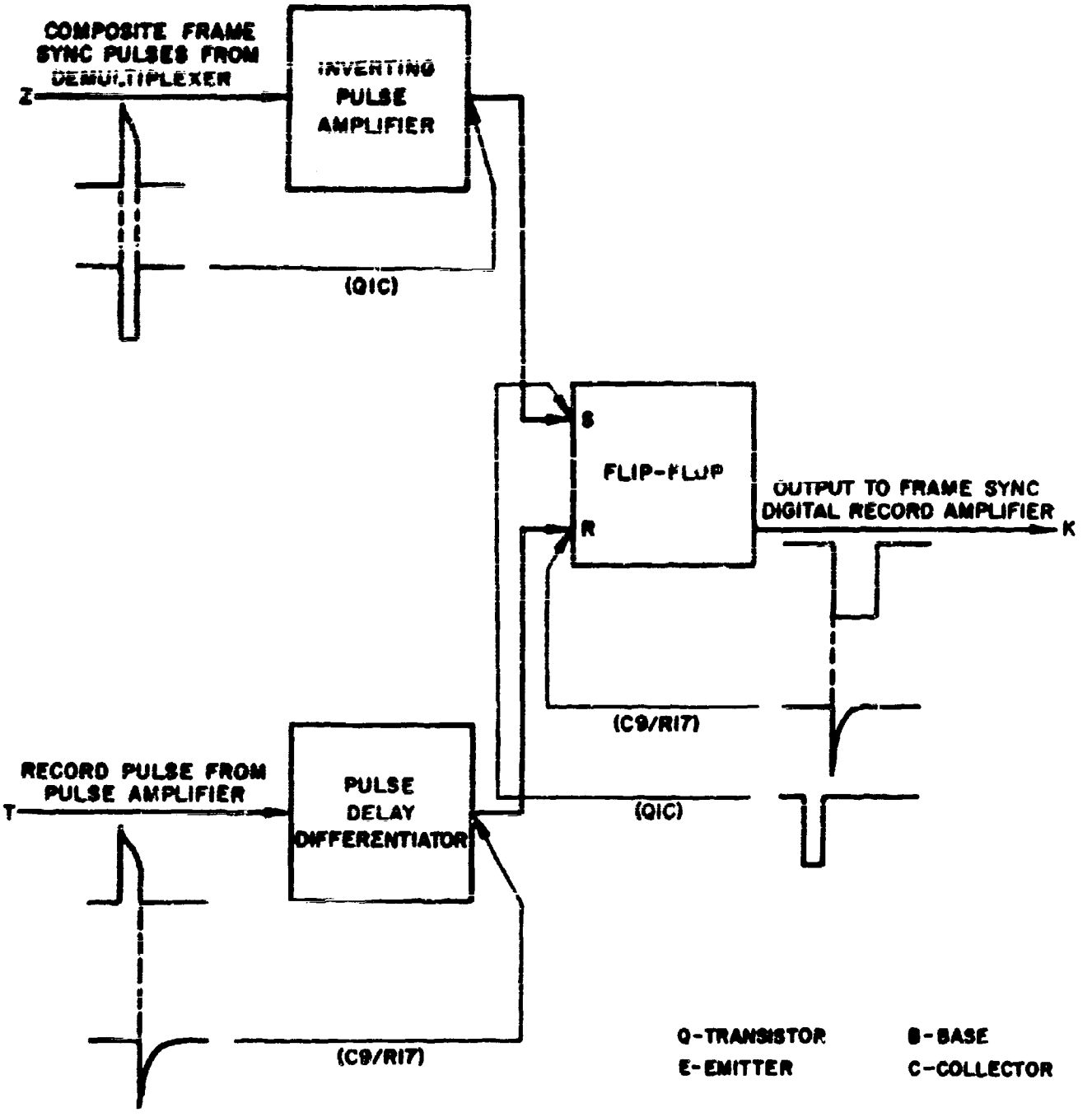


Fig. 8-24 Frame Sync Storage Record Block Diagram

If the signal is not correct, check collector of transistor Q4. Its output should be identical to the signal at pin K. If it is not, refer to Paragraph 8.4.3 for corrective action. If the signal is at the collector of transistor Q4, the trouble is in transistor Q5 or resistor R18.

8.32 PULSE AMPLIFIER

The Pulse Amplifier produces a 14-volt positive pulse starting at 0 volts dc for each positive pulse that enters it at greater than 9 volts. A schematic diagram of the Pulse Amplifier is in Fig. A-26; a block diagram is in Fig. 8-25. If there is trouble in the Pulse Amplifier, do the procedures in Paragraph 8.2 and proceed as follows:

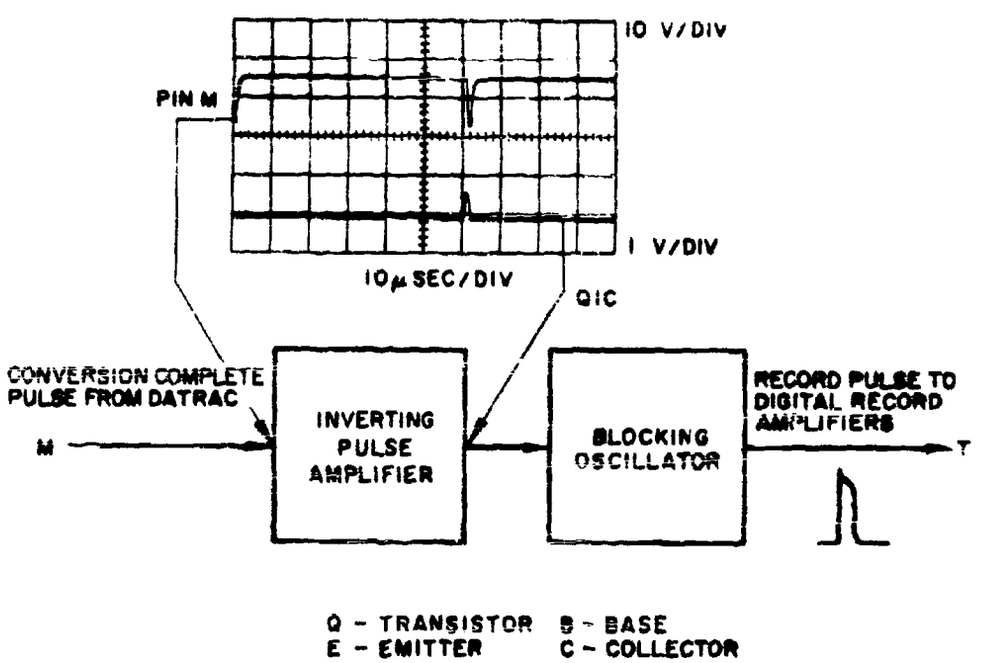


Fig. 8-25 Pulse Amplifier Block Diagram

1. Check supply voltage across decoupling capacitor C5. It should be -19 (±1) volts. Check voltage across diode CR3. It should be -13 (±2) volts. If the voltages are not correct, check decoupling network or associated Zener diodes.

2. Check input at pin M. It should be a positive-going pulse at greater than 30 volts amplitude with the baseline at 0 (±1) volt. If it is not, refer to Paragraph 8.3 for corrective action.

3. Check base of transistor Q1. Its signal should be a reproduction of the input at pin M with the baseline at -19 (±1) volts and the positive peaks clipped at -12 (±1) volts. If it is not, resistor R1, R2, R3, R12, R14, capacitor C1, diode CR5, or transistor Q1 is faulty.

4. Check collector of transistor Q1. Its output should be as shown in Fig. 8-25. If it is not, transistor Q1, capacitor C2, or resistor R4 is faulty.

5. Check output of blocking oscillator at pin T. It should be a positive pulse starting at ground and rising to 14 (±1) volts, as shown in Fig. 8-25. If it is not, the blocking oscillator is faulty. Refer to Paragraph 8.4.1 for corrective action.

8.33 DIGITAL RECORD AMPLIFIER

The Digital Record Amplifier receives the two-level digital output of the Datrac and transforms it into a suitable waveform for NRZ recording on the Magnetic Tape Recorder. A schematic diagram of the Digital Record Amplifier is in Fig. A-27; a block diagram is in Fig. 8-26. If there is trouble in the Digital Record Amplifier, do the procedures in Paragraph 8.2 and proceed as follows:

1. Check supply voltages across decoupling capacitors. It should be -19 (±1) volts across capacitor C4; +19 (±1) volts across capacitor C1 and capacitor C10; +7 (±2) volts across capacitor C5, and +10 (±4) volts across capacitor C9. Check supply voltage across diode CR1. It should be -11 (±2) volts. If the voltages are not correct, check decoupling networks and associated Zener diodes.

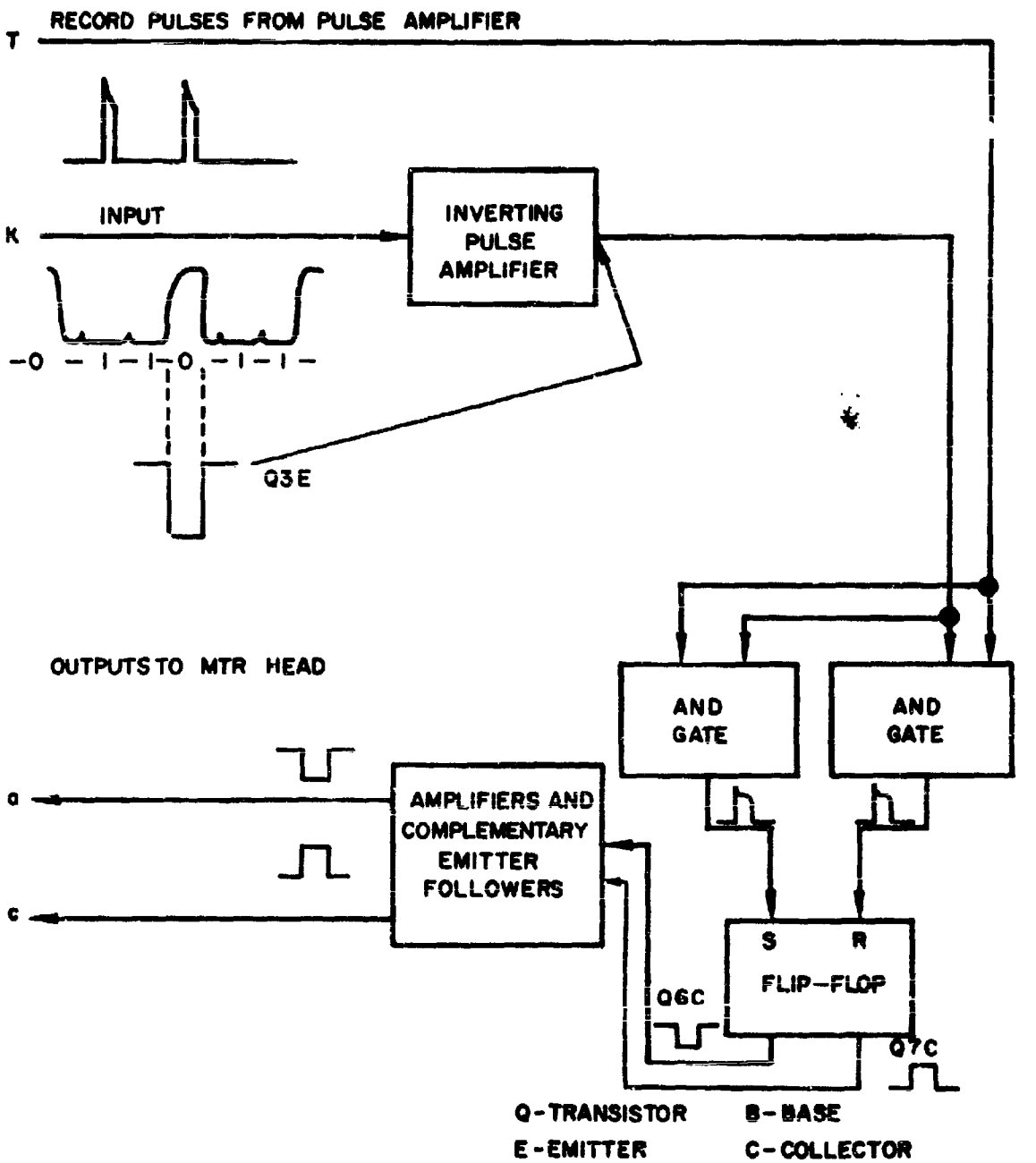


Fig. 8-26 Digital Record Amplifier Block Diagram

2. Check input at pin K. It should be the two-level digital output of the Datrac, as shown in Fig. 8-26, of either -19 (±1) volts or -4 (±1) volts. If it is not, refer to Paragraph 8.3 for corrective action.

3. Check emitter of transistor Q1. The signal should be identical to the input at pin K. If it is not, transistor Q1 or resistor R11 or R15 is faulty.

4. Check collector of transistor Q2. Its output should be an inverted version of the input signal with the levels at +19 (±1) and -11 (±2) volts. If it is not, transistor Q2, or resistor R7, R10, or R12 is faulty.

5. Check emitter of transistor Q3. Its output should be an inverted version of the input signal with levels at +19 (±1) and 0 (±1) volts. If it is not, transistor Q3 or Q4 or resistor R3 is faulty.

6. Check emitters of transistors Q4 and Q9. The signal at each point should be the same as that at the emitter of transistor Q3. If it is not, transistor Q4 or Q9, diode CR3, or resistor R13 or R24 is faulty.

7. Check input at pin T. It should be a positive blocking oscillator pulse of 14 volts amplitude with the baseline at ground. If it is not, refer to Paragraph 8.3 for corrective action.

8. Check collector of transistor Q7. The signal should be a two-level asymetric square wave which changes levels between +5 (±1) and +17 (±1) volts. The changes should occur in time phase with the leading edge of the pulses at pin T and should take place only when the input at pin K is at -19 (±10) volts. If this signal is not correct, the flip-flop is faulty. Refer to Paragraph 8.4.3 for corrective action.

9. Check emitters of transistors Q5 and Q8. The signal at each point should be the same as that at the collectors of transistors Q6 and Q7, as shown in Fig. 8-26. If it is not, transistor Q5 or Q6, capacitor C6 or C8, or resistor R21 or R22 is faulty.

NOTE: If the Digital Record Amplifier is being checked in the system and is driving the head of the Magnetic Tape Recorder, check output at pin c. The signal should be identical to that seen at the emitter of transistor Q11, except that the signal will rise and fall exponentially.

If the Digital Record Amplifier is not driving the recording head, then pins a and c should be shorted together and the signals at the emitters of transistors Q10 and Q11 rechecked. The signals at these two points should be as described in Step 11.

10. Check collectors of transistors Q14 and Q15. The signal at each point should be an asymetric square wave with levels of +10 (±1) and 0 (±1) volts. If it is not, transistor Q14 or Q15 or resistor R25, R26, R27, or R28 is faulty.

11. Check emitters of transistors Q10 and Q11. The signal at each point should be an asymetric square wave with rise and fall times of 5 (±2) microseconds with levels of 10 (±2) and 0 (±1) volts. If it is not, transistor Q10, Q11, Q12, or Q13 or resistor R31 is faulty.

8.34 DIGITAL REPRODUCE AMPLIFIER

The Digital Reproduce Amplifier accepts the digital signals from the reproduce heads of the Magnetic Tape Recorder and produces one negative pulse for each digital "one" recorded on the Magnetic Tape Recorder. A schematic diagram of the Digital Reproduce Amplifier is in Fig. A-28; a block diagram is in Fig. 8-27. If there is trouble in the Digital Reproduce Amplifier, do the procedures in Paragraph 8.2 and proceed as follows:

NOTE: In making these checks, the tape speed should be 100 ips.

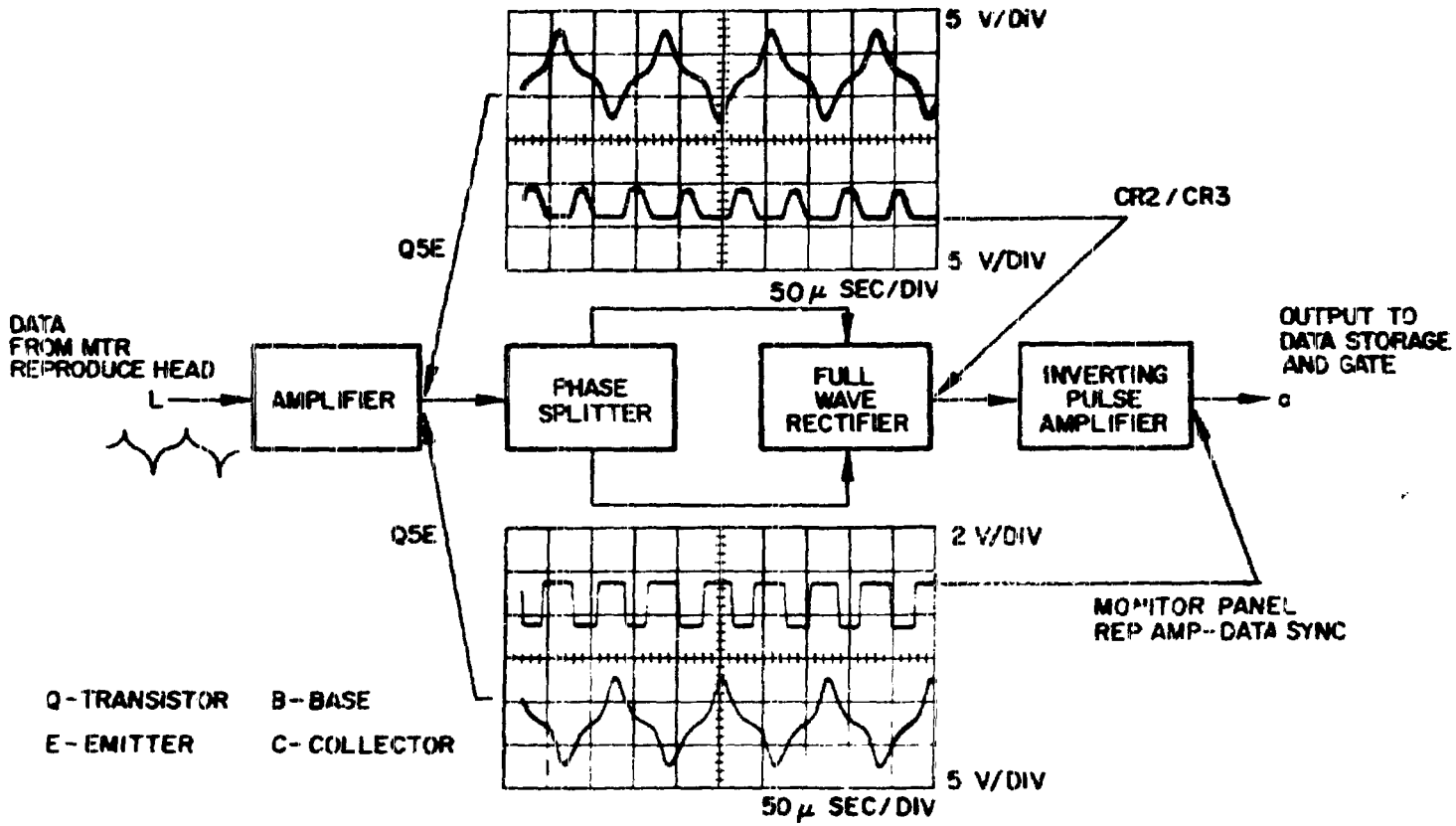


Fig. 8-27 Digital Reproduce Amplifier Block Diagram

1. Check supply voltages across decoupling capacitors. It should be -19 (±1) volts across capacitors C9, C10, and C18. It should be +19 (±1) volts across capacitor C16 and +13 (±2) volts across capacitor C17. If the voltages are not correct, check decoupling networks.

2. Disconnect input cable from Magnetic Tape Recorder. Check output of reproduce head by looking at signal across the two output pins of the head. This signal should be as shown for the data from the Magnetic Tape Recorder reproduce head in Fig. 8-27. It should be 13 (±5) millivolts peak-to-peak amplitude. When check is completed, reconnect input cable to Digital Reproduce Amplifier.

3. Check emitter of transistor Q5. Its output should be as shown in Fig. 8-27 with an amplitude of 10 (±3) volts peak-to-peak. If this signal is not correct, proceed as follows:

   a. Check collector of transistor Q1. Its output should be the same as that for the amplifier output except that the amplitude should be reduced. If not, transistor Q1 or its associated components are faulty.

   b. Check collector of transistor Q2. Its output should be the same as that described for the amplifier except that its amplitude will be greater than that at the collector of transistor Q1. If the signal is not correct, transistor Q2 or its associated components are faulty.

   c. Check collector of transistor Q3. Its output should be the same as that described for the amplifier output except that the amplitude should be 3 (±1) volts peak-to-peak. If it is not, transistor Q3 or its associated components are faulty.

   d. Check collector of transistor Q4. Its output should be the same as that described for the amplifier output. If it is not, transistor Q4 or its associated components are faulty.

4. Check output of full-wave rectifier at intersection of diodes CR2 and CR3. It should be as shown in Fig. 8-27. If the signal is not correct, proceed as follows:

   a. Check emitter of transistor Q10. Its output should be the same as that of the emitter of transistor Q5. If it is not, transistor Q10 or its associated components are faulty.

b. Check emitter of transistor Q9. Its output should be an inverted version of the signal at the emitter of transistor Q5. If it is not, transistor Q9 or its associated components are faulty.

c. Check base of transistor Q9. Its output should be the same as that described for the emitter of transistor Q5. If it is not, transistor Q10, capacitor C20, or resistor R36 or R43 is faulty.

d. If trouble is still present, diode CR2 or CR3 or their associated components are faulty.

5. Check output of inverting pulse amplifier at pin a. It should be as shown in Fig. 8-27, a negative pulse of 13 (±1) volts amplitude with baseline at +13 volts. There should be one pulse output for each pulse at the output of the full-wave rectifier. If the signal is not correct, proceed as follows:

a. Check emitter of transistor Q7. Its output should be the same as the output of the full-wave rectifier, except that the baseline should be at +0.5 volt. If it is not, transistor Q7 or resistor R32 or R34 is faulty.

b. Check collector of transistor Q8. Its output should be the same as that described for pin a. If it is not, transistor Q6 or Q8 or resistor R33 is faulty.

c. If the trouble still exists, transistor Q6 or resistor R28, R29, or R30 is faulty.

8.35 DATA STORAGE AND GATE

The Data Storage and Gate board is used as a buffer to store signals from the Digital Record Amplifiers. There are two identical circuits on each of the five boards in the Ground Station. Maintenance procedures for one circuit are given here. A schematic diagram of the Data Storage and Gate board is in Fig. A-29; a block diagram is in Fig. 8-28. If there is trouble in the Data Storage and Gate board, do the procedures in Paragraph 8.2 and proceed as follows:

1. Check supply voltages across decoupling capacitors. It should be +19 (±1) volts across capacitor C1; -19 (±1) volts across capacitor C2; +14 (±2) volts across

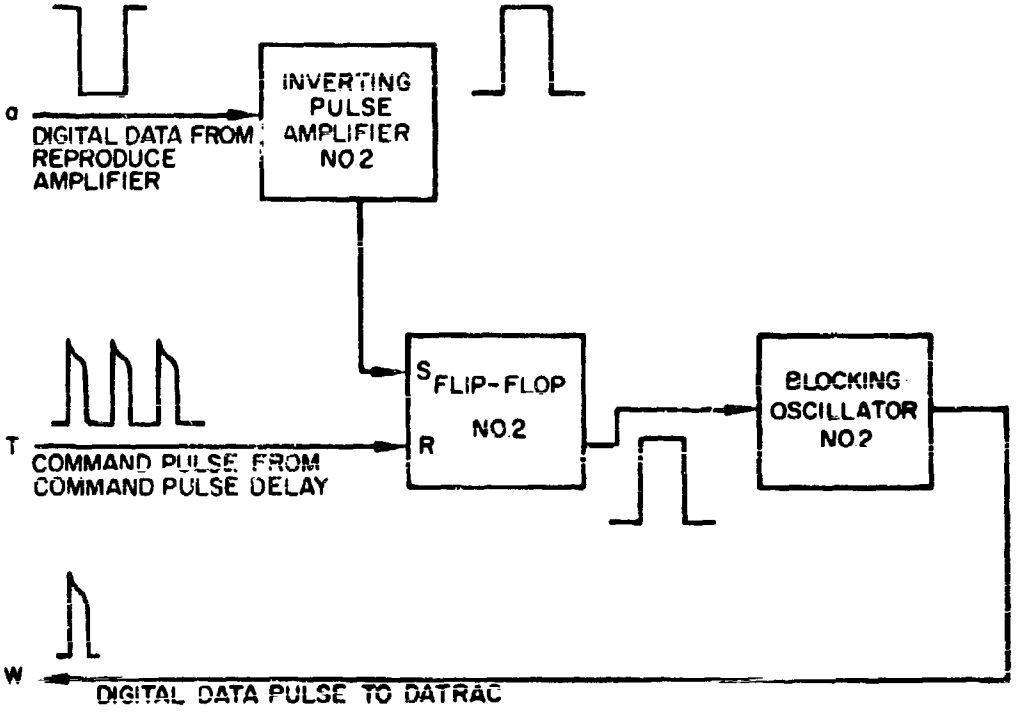


Fig. 8-28 Data Storage and Gate Block Diagram

capacitor C24; -9 (±2) volts across capacitor C25; and -15 (±2) volts across capacitor C26. Check voltage across diode CR13. It should be +9 (±2) volts. If the supply voltages are not correct, check decoupling networks and associated Zener diodes.

2. Check input at pin a. The negative-going pulse should be as shown in Fig. 8-28. If it is not, refer to Paragraph 8.3 for corrective action.

3. Check output of inverting pulse amplifier no. 2 at the collector of transistor Q7. It should be a positive-going pulse with an amplitude of 9 volts and a baseline at ground, as shown in Fig. 8-28.

4. Check output of flip-flop no. 2 at collector of transistor Q8. It should be an asymetric square wave with levels of -5 and -15 volts. The change from -15 to -5 volts should occur in time with the leading edge of the pulses at pin T. The change from -5 to -15 volts should occur in time with the leading edge of the pulses at pin a. If the signal is not correct, refer to Paragraph 8.4.3 for corrective action.

5. Check emitter of transistor Q10. The output should be identical to that described in Step 4. If it is not, transistor Q10, resistor R40, or capacitor C21 is faulty.

6. Check output of blocking oscillator no. 2 at pin W. It should be a positive pulse of 35 (±3) volts amplitude with the baseline at ground. If it is not, the blocking oscillator is faulty. Refer to Paragraph 8.4.1 for corrective action.

8.36 DATA SYNC DELAY REPRODUCE

The Data Sync Delay Reproduce receives pulses from the Data Sync Reproduce Amplifier and delays each until the corresponding nine-bit digital word is stored in the Data Storage and Gate board. A schematic diagram of the Data Sync Delay Reproduce board is in Fig. A-30; a block diagram is in Fig. 8-29. If there is trouble in the Data Sync Delay Reproduce board, do the procedures in Paragraph 8.2 and proceed as follows:

1. Check supply voltage across decoupling capacitors. It should be +19 (±1) volts across capacitor C2 and -19 (±1) volts across capacitor C7. Check voltage across

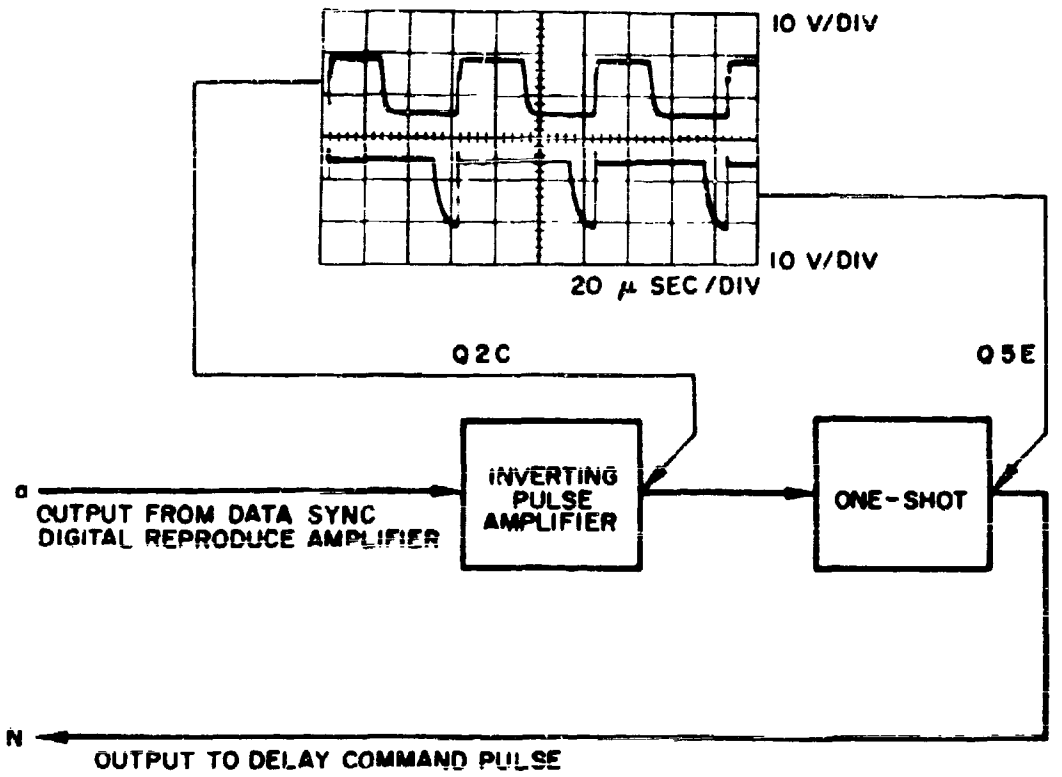


Fig. 8-29 Data Sync Delay Reproduce Block Diagram

diode CR1. It should be +15 (±2) volts. If the voltages are not correct, check decoupling networks and associated Zener diodes.

2. Check input at pin a. It should be a negative pulse from the Data Sync Reproduce Amplifier of 13 (±1) volts with the baseline at +13 volts, as shown in Fig. 8-29. If it is not, refer to Paragraph 8.3 for corrective action.

3. Check output of inverting pulse amplifier at collector of transistor Q2. The signal should be as shown in Fig. 8-29. The amplitude of this positive pulse should be 14 (±3) volts with the baseline at ground. If the signal is not correct, proceed as follows:

   a. Check emitter of transistor Q1. Its output should be the same as the signal described in Step 2. If it is not, transistor Q1 or resistor R3 or R2 is faulty. If these components are functioning properly, the trouble is in transistor Q2, resistor R4 or R5, or capacitor C1.

4. Check output signal of one-shot at collector of transistor Q4. It should be as shown in Fig. 8-29 for the emitter of transistor Q5. This signal should have one output pulse for each input pulse at pin a. The upper and lower limits should be -4 (±2) volts and -16 (±2) volts. If the signal is not correct, the one-shot is faulty. Refer to Paragraph 8.4.2 for corrective action.

5. Check emitter of transistor Q5. Its output should be the same as that described in Step 4 and Fig. 8-29. If the signal is not correct, transistor Q5 or resistor R15 is faulty.

8.37 DELAY COMMAND PULSE

The Delay Command Pulse board receives the signal from the Data Sync Delay Reproduce board. For each positive pulse input it generates three timing pulse outputs. A schematic diagram of the Delay Command Pulse board is in Fig. A-31; a block diagram is in Fig. 8-30. If there is trouble in the Delay Command Pulse board, do the procedures in Paragraph 8.2 and proceed as follows:

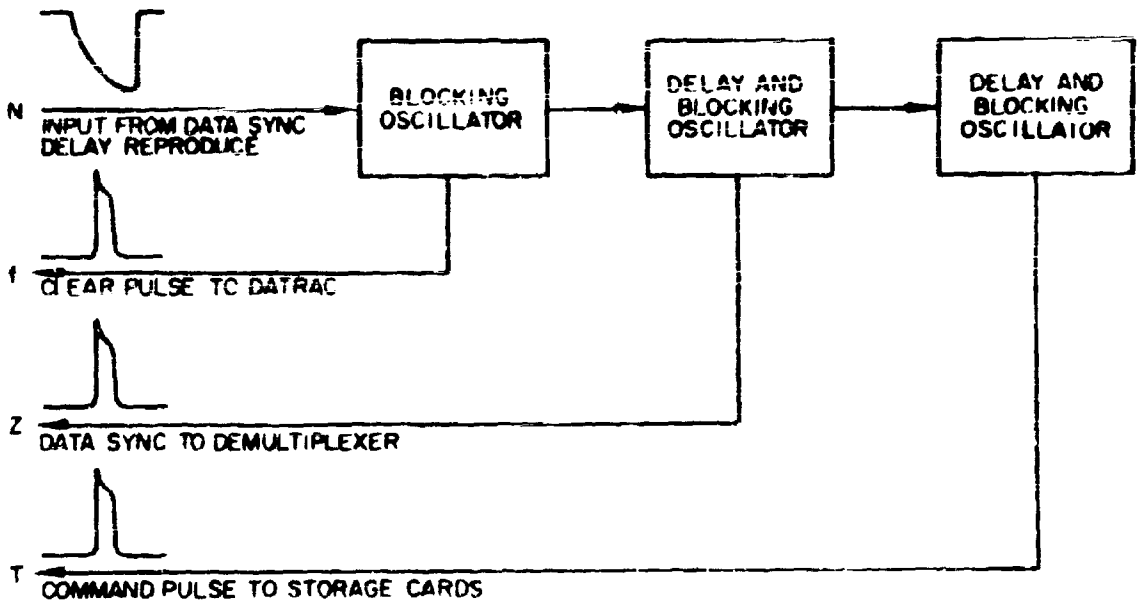


Fig. 8-30 Delay Command Pulse Block Diagram

1. Check supply voltage across decoupling capacitors. It should be -19 (±1) volts across capacitors C1 and C3. If it is not, check decoupling networks.

2. Check input at pin N. It should be the output signal from Data Sync Delay Reproduce, as shown in Fig. 8-30. If it is not, refer to Paragraph 8.3 for corrective action.

3. Check output at pin f. It should be a positive pulse of 28 (±4) volts amplitude with the baseline at ground. There should be one output pulse for each input pulse at pin N. If this signal is not correct, the first blocking oscillator is faulty. Refer to Paragraph 8.4.1 for corrective action.

4. Check emitter of transistor Q3. Its output should be a positive pulse with an amplitude of 9 (±1) volts and the baseline at -18 (±1) volts. If it is not, transistor Q3, capacitor C6, or resistor R7 or R11 is faulty.

5. Check output of delay and blocking oscillator at pin Z. It should be a positive pulse of 14 (±1) volts amplitude with the baseline at ground. There should be one pulse for each input at pin N. If this signal is not correct, the second blocking oscillator is faulty. Refer to Paragraph 8.4.1 for corrective action.

6. Check emitter of transistor Q6. Its output should be a positive pulse with an amplitude of 15 (±1) volts and the baseline at -18 (±1) volts. If it is not, transistor Q6, capacitor C9, or resistor R15 or R17 is faulty.

7. Check output of delay and blocking oscillator at pin T. It should be a positive pulse with an amplitude of 13 (±1) volts and the baseline at -19 (±1) volts. There should be one output pulse for each pulse appearing at pin N. If this signal is not correct, refer to Paragraph 8.4.1 for corrective action.

8.38 DUTY CYCLE I

The Duty Cycle I board serrates the composite PAM pulse train from the digital-to-analog converter to approximately a 50 percent duty cycle. A schematic diagram of the Duty Cycle I board is in Fig. A-32; a block diagram is in Fig. 8-31. If there is trouble in the Duty Cycle I board, do the procedures in Paragraph 8.2 and proceed as follows:

1. Make sure that variable components are adjusted according to the procedures in Volume I, Section 4.

2. Check input voltage across decoupling capacitors. It should be -20 (±1) volts across capacitor C1, +20 (±1) volts across capacitor C22, and -10 (±1) volts across capacitor C20. If it is not, check decoupling networks.

3. Check input at pin b. It should be as shown in Fig. 8-31. If it is not, refer to Paragraph 8.3 for corrective action.

4. Check collector of transistor Q2. Its output should be a typical one-shot waveform, i.e., negative from -3 (±2) volts, falling exponentially to -17 (±2) volts, and then rising to -3 (±2) volts with a rise time of less than 2 microseconds. If it is not, one-shot no. 1 is faulty. Refer to Paragraph 8.4.2 for corrective action.

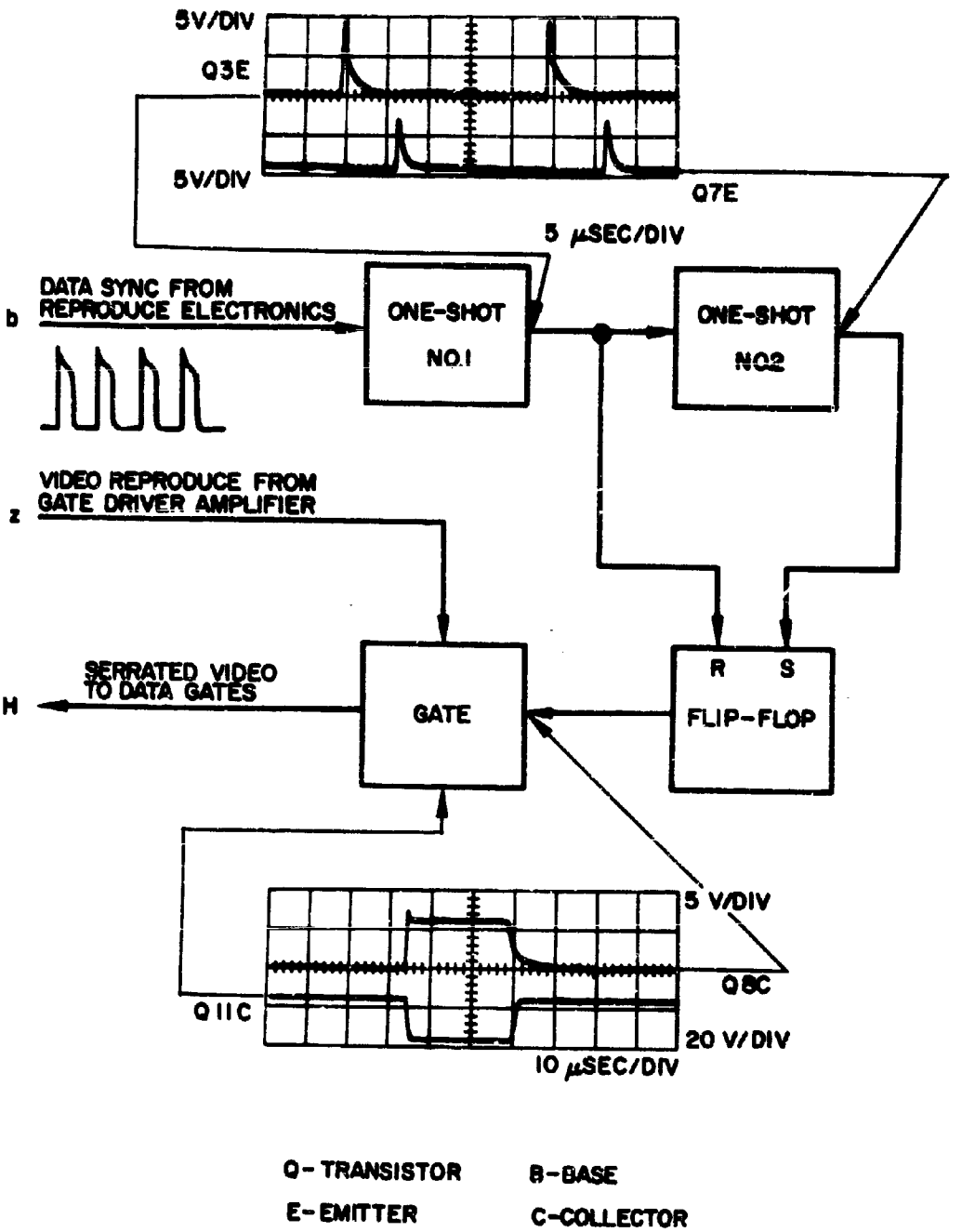


Fig. 8-31 Duty Cycle I Block Diagram

5. Check emitter of transistor Q3. Its output should be as shown in Fig. 8-31. If it is not, transistor Q3, resistor R10 or R11, or capacitor C7 is faulty.

6. Check emitter of transistor Q4. Its output should be the same as the output of the emitter of transistor Q3, as shown in Fig. 8-31. If it is not, transistor Q4 or resistor R12 is faulty.

7. Check collector of transistor Q6. Its output should be a typical one-shot waveform, i.e., negative from -3 (±2) volts, falling exponentially to -17 (±2) volts, and then rising to -3 (±2) volts with a rise time of less than 2 microseconds. If it is not, one-shot no. 2 is faulty. Refer to Paragraph 8.4.2 for corrective action.

8. Check emitter of transistor Q7. It should be as shown in Fig. 8-31. If it is not, transistor Q7, resistor R22 or R23, or capacitor C13 is faulty.

9. Check collector of transistor Q8. Its output should be as shown in Fig. 8-31. Check collector of transistor Q9. Its output should be the complement of the output at the collector of transistor Q8. If it is not, the flip-flop is faulty. Refer to Paragraph 8.4.3 for corrective action.

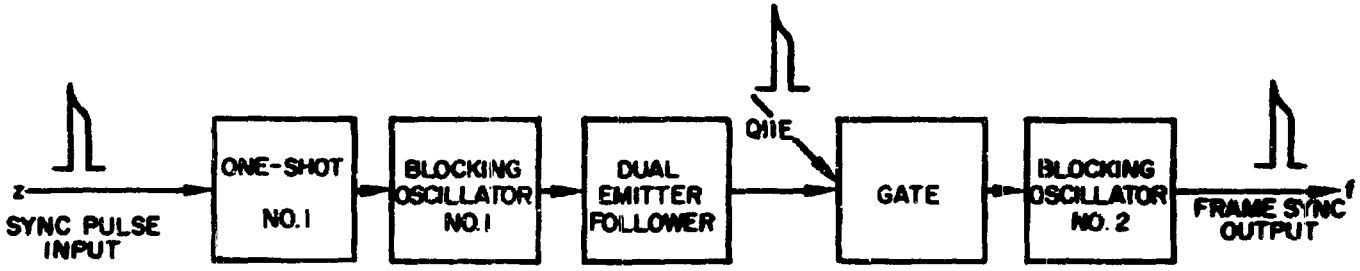
10. Check emitter of transistor Q10. Its output should be the same as that of the collector of transistor Q8, as shown in Fig. 8-31. If it is not, transistor Q10 or resistor R33 is faulty.

11. Check collector of transistor Q11. Its output should be as shown in Fig. 8-31. If it is not, transistor Q11 or resistor R35 or R36 is faulty.

12. Check transistors Q12 and Q13 by checking whether the input at pin Z (PAM signal from Datrac) is present. Then, check that there is a serrated output at pin H. If the serrated output is not present, one or both of the transistors is faulty.

8.39 FRAME SYNC DELAY REPRODUCE

The Frame Sync Delay Reproduce inserts a delay in the composite frame sync. A block diagram is in Fig. 8-32, and schematic diagrams are in Figs. A-33 and A-54. If there is trouble in the Frame Sync Delay Reproduce, proceed as follows:



Q - TRANSISTOR B - BASE
E - EMITTER C - COLLECTOR

Fig. 8-32 Frame Sync Delay Reproduce Block Diagram

1. Make sure that variable components are properly adjusted in accordance with Volume 1, Section 4.

2. Check supply voltage across decoupling capacitor C2. It should be 20 (±1) volts. If it is not, check decoupling networks.

3. Check pin Z for composite sync pulse input as shown in Fig. 8-32. If the signal is not present or is incorrect, refer to Paragraph 8.3 for corrective action.

4. Check cathode of diode CR1. Its output should be a positive spike that is in time phase with the leading edge of the input at pin Z. If not, the trouble is in diode CR1, resistor R1, or capacitor C1 or C3.

5. Check collector of transistor Q4. Its output should be a waveform that starts at +18 (±2) volts and falls off exponentially to +4 (±2) volts. It should be in time phase with the leading edge of the sync pulses on pin Z, and it should rise to +18 (±2) volts with a rise time of less than 2 microseconds after a nominal delay of 5 to 10 microseconds. If not, refer to Paragraph 8.4.2 for corrective action.

6. Check voltage of terminal 2 of transformer T1. It should be a positive blocking oscillator pulse of 8 (±2) volts. If not, refer to Paragraph 8.4.1 for corrective action.

7. Check emitter of transistor Q9. Its output should be a positive blocking oscillator pulse of 8 (±2) volts. If not, trouble is in transistor Q9, resistor R27, or R28.

8. Check the emitter of transistor Q11. Its output should be as shown in Fig. 8-32. If not, trouble is in transistor Q11, resistor R32 or R33.

9. Check signal at collector of transistor Q12. There should be a blocking oscillator pulse that is 2 (±1) volts high. If not, trouble is in transistor Q12, resistor R36 or R37, or capacitor C21.

10. Check the signal at pin f. It should be as shown in Fig. 8-32. If not, refer to Paragraph 8.4.1 for corrective action.

8.40 ANALOG-TO-DIGITAL CONVERTER

For instructions on isolating and repairing trouble in the Analog-to-Digital Converter, refer to the Epsco, Inc., manual of instructions. Schematic diagrams that show Lockheed modifications to the Analog-to-Digital Converter are in Figs. A-20 through A-24.

Two adjustments are available on the sample and hold circuitry and should be adjusted when the unit is first placed in operation. Data pulses should be present on terminal 32 of Chassis no. 1. Datrac command pulses should be present on terminal 12 of Chassis no. 2. Sampled output should be present on terminal 25 of Chassis no. 2. Offset adjustment resistor R7 of Chassis no. 1 and gain adjustment resistor R63 of Chassis no. 2 are set so that -10 volts on the data input corresponds to 0 volts on the sampled output. These voltages need only to be measured within 10 percent accuracy for the initial setting up of the sample and hold circuitry.

8.41 MAGNETIC TAPE RECORDER

For instructions on isolating and repairing trouble in the Magnetic Tape Recorder, refer to the Ampex Corp. manual of instructions.

8.42 POWER SUPPLY INTERLOCK

The Power Supply Interlock should perform with a minimum of maintenance. The relay contacts are more than adequate in capacity for the normal loads being carried. However, if trouble should develop, refer to Fig. A-34 and make the following checks:

1. Check inputs for appropriate signal.
2. Check relays and replace any that are faulty.
3. Check wiring continuity.

Section 9
VACUUM TUBE VOLTAGE CHART

Location	Part No.	Tube No.	Plate	Grid	Cathode
DC Amplifier	V1A	6201	+180 (±20)	0 (±0.5)	+5 (±5)
	V1B		+180 (±20)	0 (±1)	+5 (±5)
	V2A	6201	+300 (±10)	0 (±10)	+5 (±10)
	V2B		+180 (±20)	0 (±1)	+5 (±10)
	V3A	6201	+300 (±10)	0 (±10)	+5 (±10)
	V3B		+300 (±10)	0 (±10)	+5 (±10)
Noise Filter	V1A	6463	+300 (±10)	0 (±0.5)	+14 (±10)
	V1B		+300 (±10)	0 (±0.5)	+14 (±10)
	V2A	6463	0 (±10)	-115 (±20)	-100 (±20)
	V2B		0 (±10)	-115 (±20)	-100 (±20)
Noise Filter Amplifier	V1A	6201	+180 (±20)	0 (±0.5)	+5 (±10)
	V1B		+180 (+20)	0 (±1)	+5 (±10)
	V2A	6201	+300 (±10)	0 (±10)	+5 (±10)
	V2B		+180 (±20)	0 (±1)	+5 (±10)
	V3A	6463	+300 (±10)	0 (±10)	+14 (±10)
	V3B		+300 (±10)	+7 (±15)	+21 (±15)
Gate Driver Amplifier	V1A	6201	+180 (±20)	0 (+0.5)	+5 (±10)
	V1B		+180 (±20)	0 (±1)	+5 (+10)
	V2A	6463	+300 (±10)	-3 (±10)	+9 (±10)
	V2B		+300 (±10)	-3 (±10)	+9 (±10)

Notes: (1) Filament Voltage is 6.3 (±0.5) vdc.
(2) Voltages are with jumper between J2 and J3 removed.
(3) Voltages are with all interconnecting co-axial cables removed and only 6.3 (±5%) vdc, -150 (±1%) vdc, and +300 (±1%) vdc applied.

Section 10
WIRING

The wiring scheme for the PAM-FM Ground Station (Vibration and G-A) is illustrated in Figs. 10-1 through 10-6 in block diagram form. Record and reproduce modes of operation are included in these wiring diagrams.

Differences in the Magnetic Tape Recorders required modifications in the wiring system for squelch and analog control in the Ground Stations.

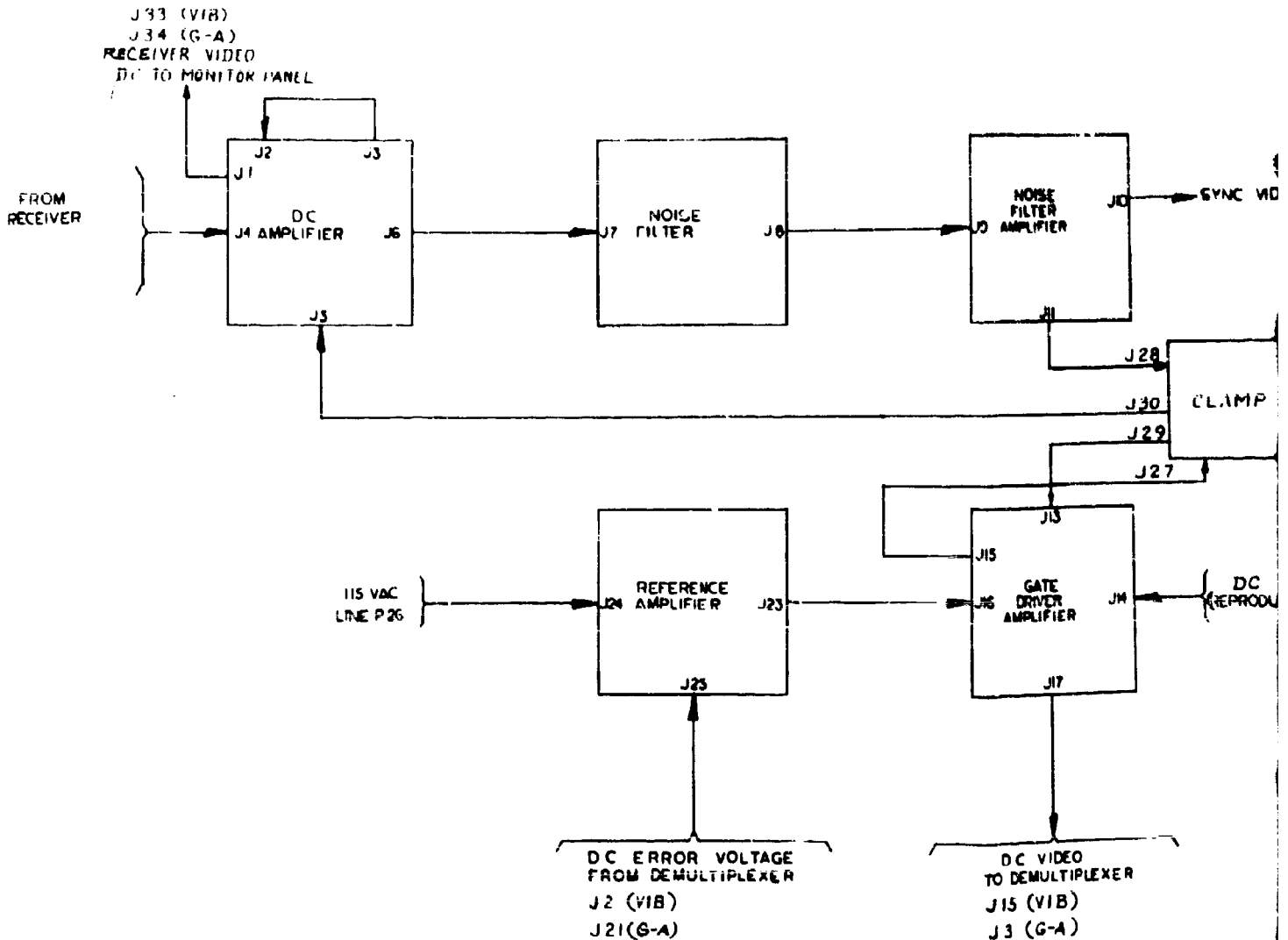
Magnetic Tape Recorder S/N 101 (used in Hawaii Station) did not have a jack J4 on the back of the blower rack. Cable 44975-03B was, therefore, wired into fanning strip no. 2 in the analog record rack. Since there was no internal wiring between the blower rack and any of the analog racks, primary power was supplied to the three analog racks by a 3-wire cable wired into the blower rack and terminating in the lower analog rack with a 4-pin Continental connector.

In adding the +120-vdc squelch wire from the Magnetic Tape Recorder control box to the analog racks, several methods were used.

(1) In Magnetic Tape Recorders S/N 102 (Vandenberg) and S/N 103 (AMR), a 5-pin female connector, jack J5, was mounted on the control box and pin A of this connector was wired to switched +120 vdc. A single wire cable was installed from jack J5 to fanning strip no. 2 terminal no. 6 in all analog racks.

(2) In Magnetic Tape Recorder S/N 101 (Hawaii), jack J5 was added to the control box as in S/N 102 and S/N 103. However, jack J5 was not used for S/N 101. Instead, a jumper was installed from pin A of jack J5 to previously blank pin B of jack J3 and a new wire was installed from jack J5 to fanning strip no. 2 terminal no. 6 in all analog racks.

(3) In Magnetic Tape Recorders S/N 104 (STC) and S/N 106 (Data Reduction), jack J5 was not installed in the control box. The switched +120 vdc for squelch was wired directly to pin B of jack J3 and a new wire installed in Cable 44975-03B. Plug P5 of the same cable was changed from a 4-pin to a 5-pin connector and the new wire connected to pin E of plug P4 and pin B of plug P3. All other wires in this cable kept their original pin designation. Jack J4 on the back of the blower rack was changed from a 4-pin male to a 5-pin male and pin E of this connector was tied to terminal no. 6 of fanning strip no. 2 in bottom analog rack. All other wires of jack J4 kept their original pin designations.



J2-J17-J27-J32 BNC
J18-J21 CONTINENTAL 7-20P
J22 MS3102A20-33P (C)
J23 AMPHENOL 57-20140
J24 AMPHENOL 57-30140
J25 CONTINENTAL 4-20S

- A - 150
- B + 300
- D GROUND
- E +20 (RELAYS)
- F, H 6.3 VAC

A

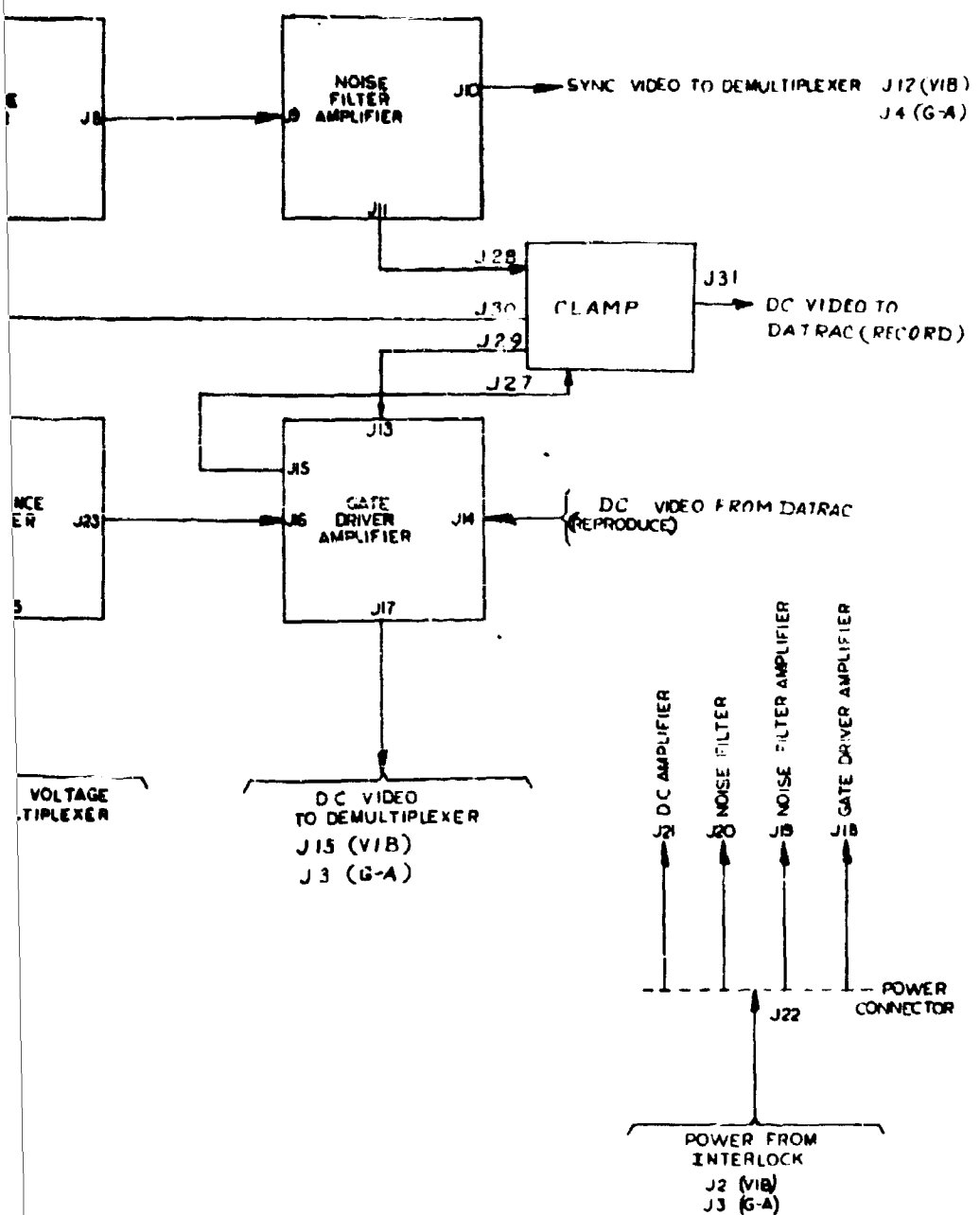
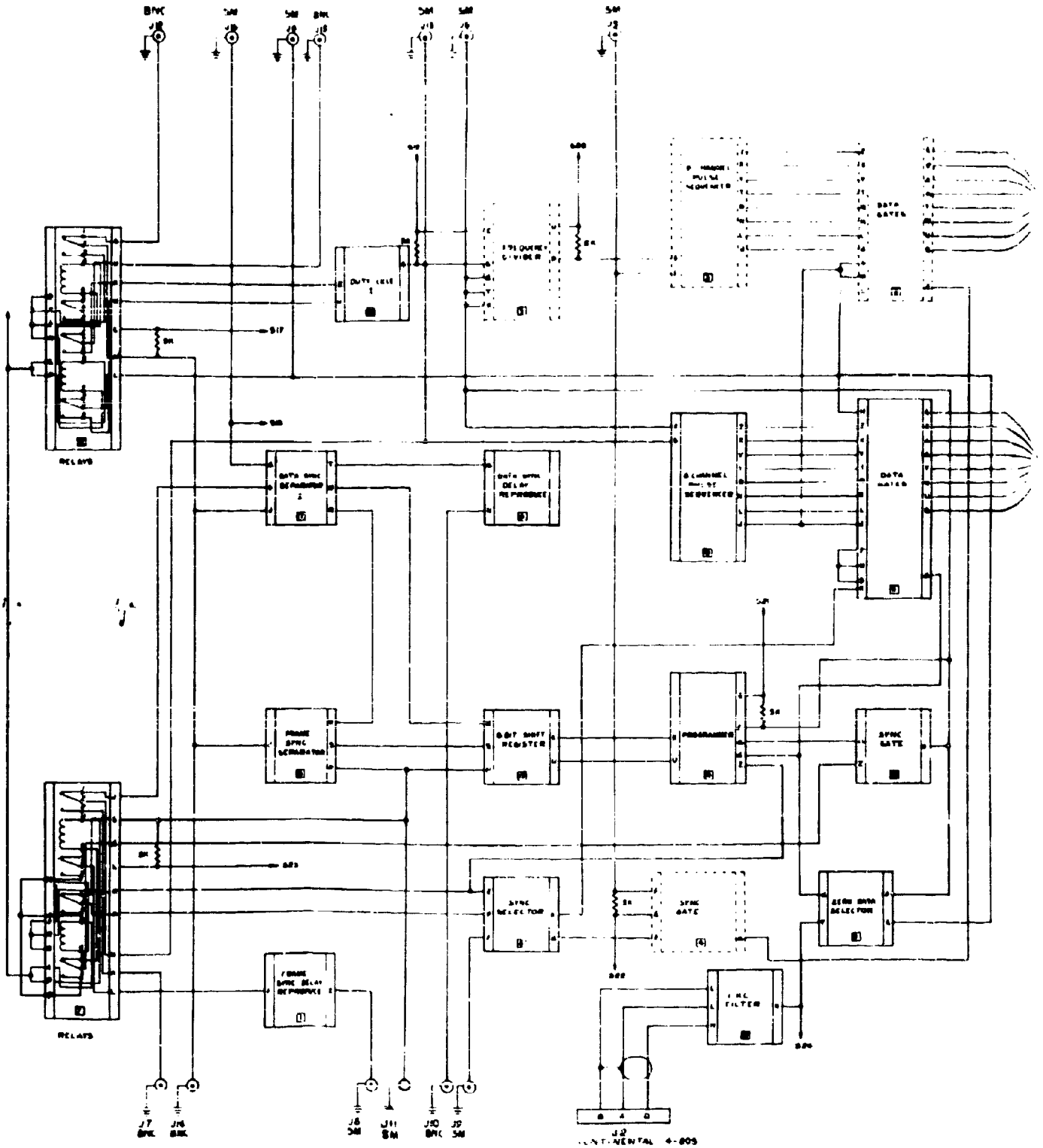


Fig. 10-1 Base Band Unit Wiring Block Diagram



A

NEW drawing - 25 June 1960

Replaces Fig. 10-2 and Fig. 10-3
pages 10-5 and 10-7

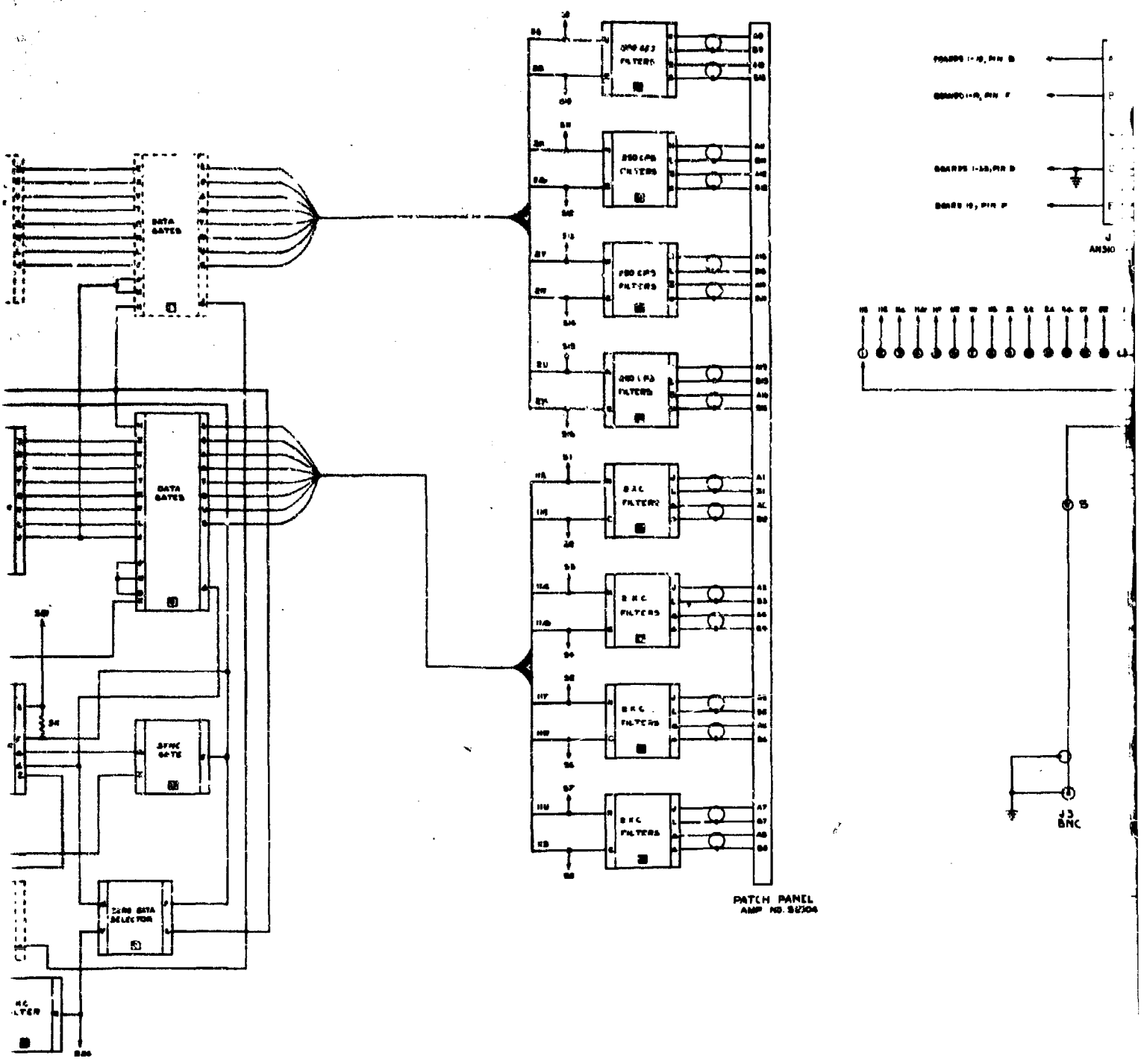


Fig. 10-2 Vibration D
Block Diag
Reproduce

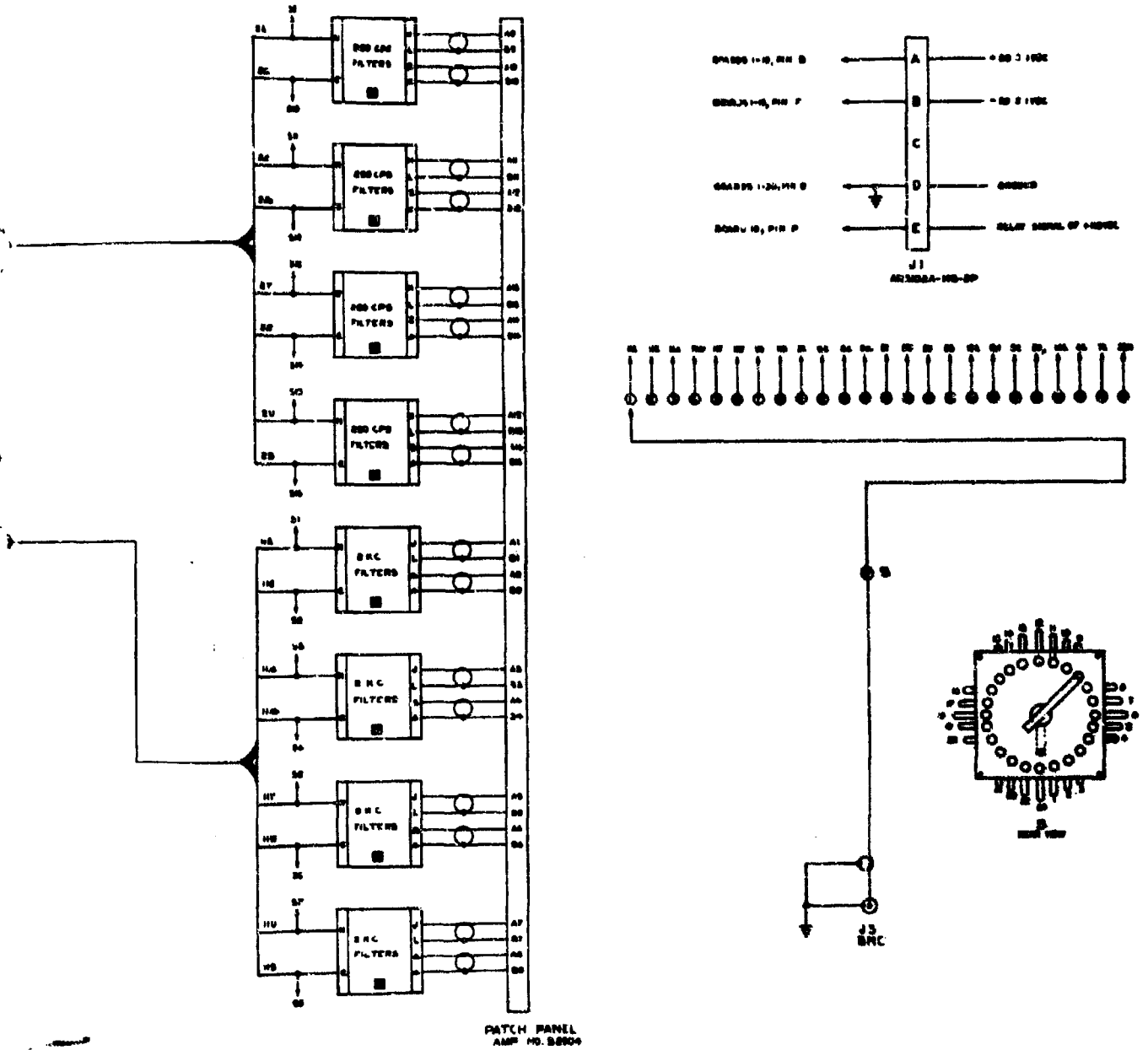
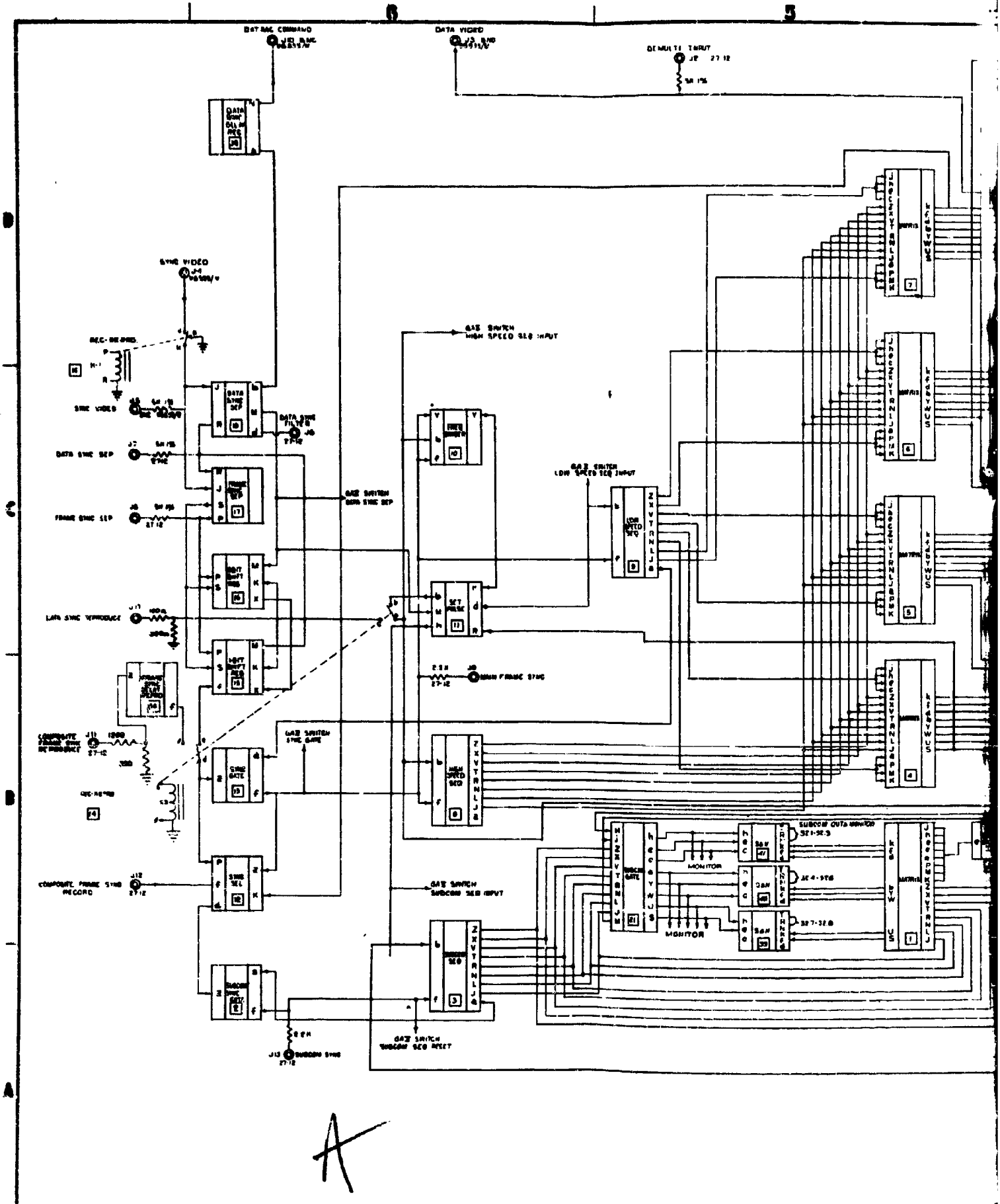
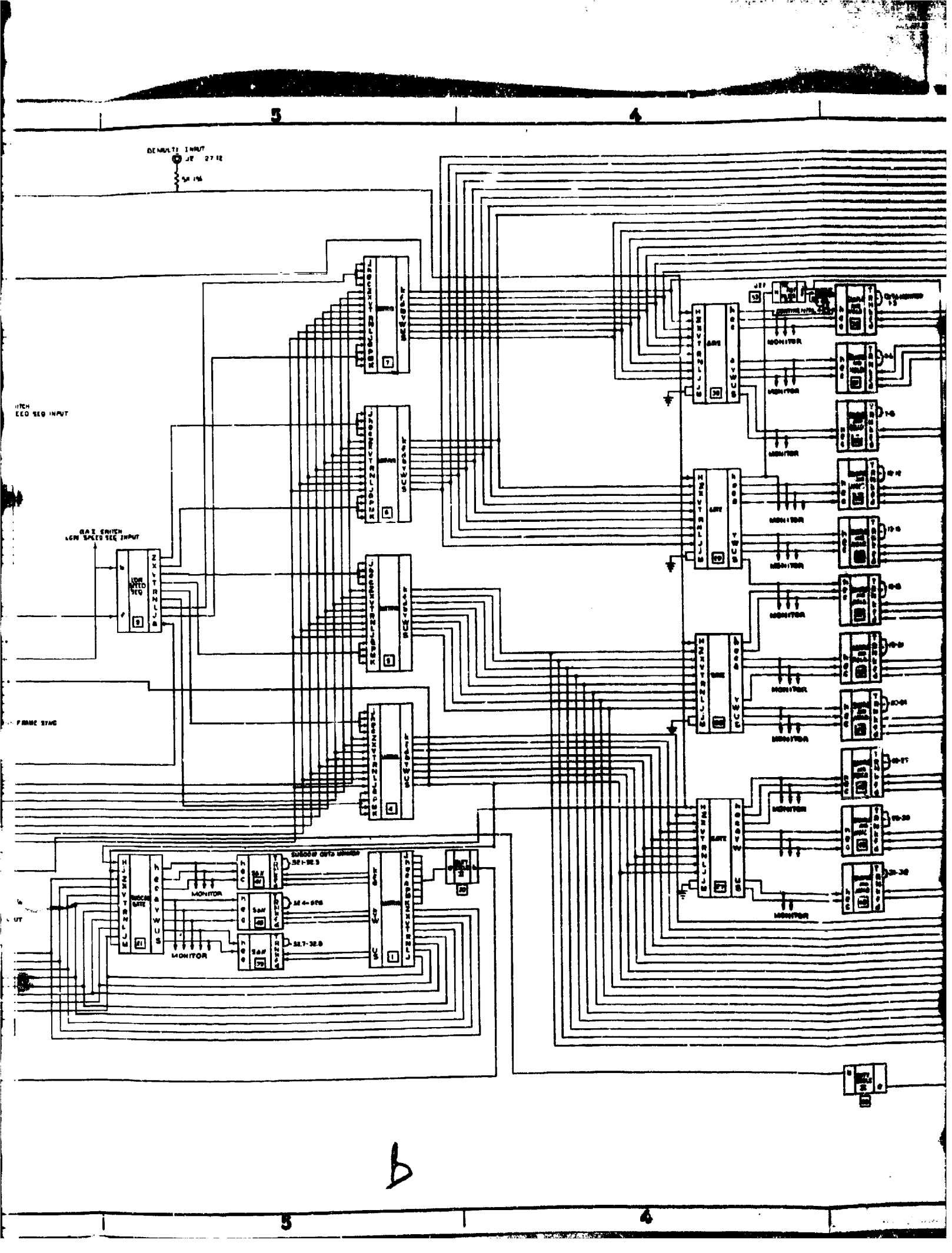


Fig. 10-2 Vibration Demultiplexer, Wiring Block Diagram, Record and Reproduce modes.


DATA VIDEO
SYNC VIDEO
DATA SYNC SEP
FRAME SYNC SEP
LINE SYNC REFERENCE
COMPOSITE FRAME SYNC RECORD
GAZ SWITCH HIGH SPEED SEQ INPUT
GAZ SWITCH LOW SPEED SEQ INPUT
GAZ SWITCH SUBCOM SEQ INPUT
SUBCOM OUTA MONITOR
MONITOR
MONITOR

A


5
4
MONITOR
MONITOR
MONITOR
MONITOR
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4

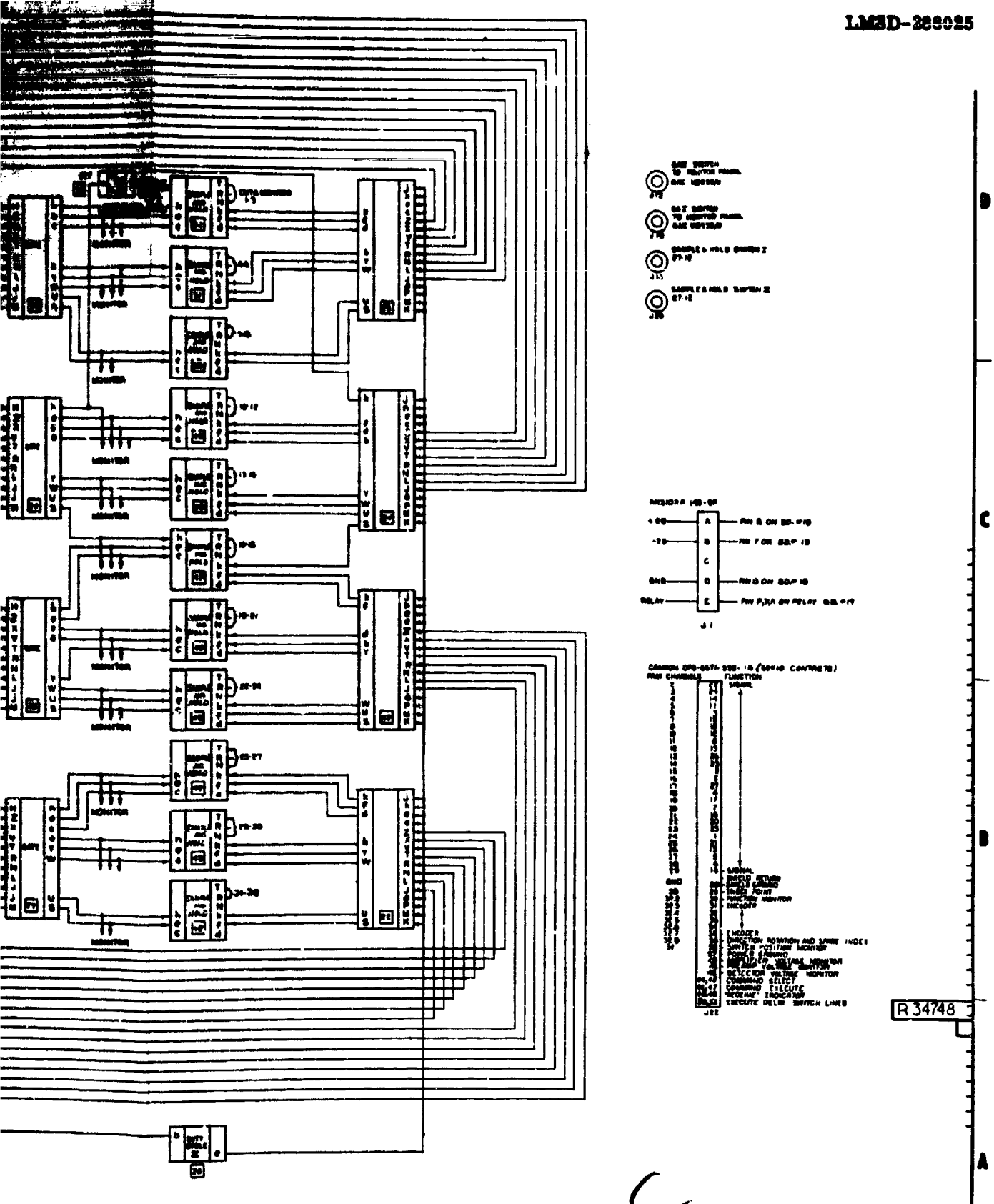


Fig. 10-4 G-A Demultiplexer Wiring Block Diagram

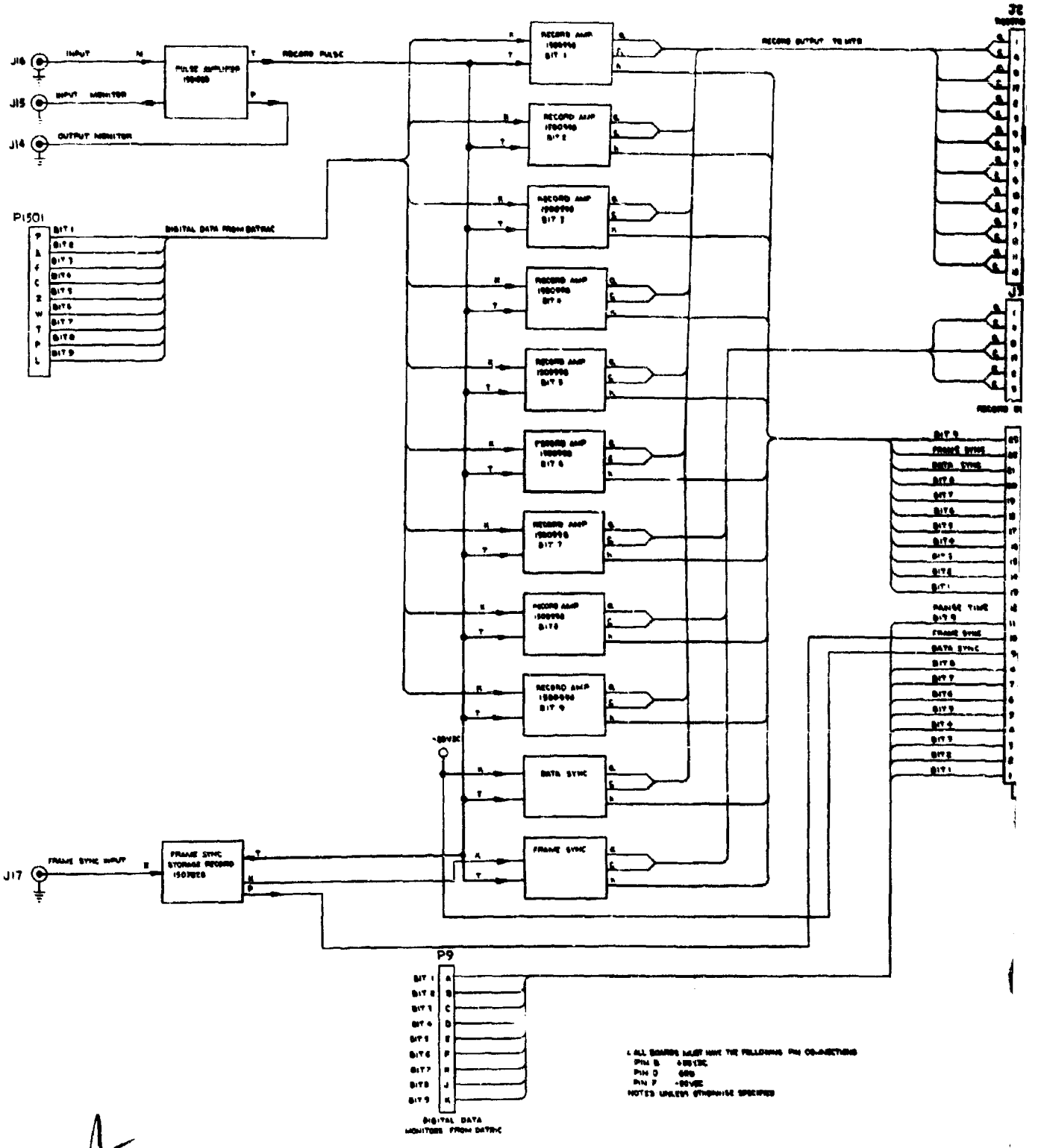

J16
INPUT
J15
INPUT MONITOR
J14
OUTPUT MONITOR
PULSE AMPLIFIER
RECORD PULSE
P1501
DIGITAL DATA FROM DATRAC
RECORD AMP
DATA SYNC
FRAME SYNC
J17
FRAME SYNC INPUT
FRAME SYNC STORAGE RECORD
P9
DIGITAL DATA MONITORS FROM DATRAC

Fig. 10-5

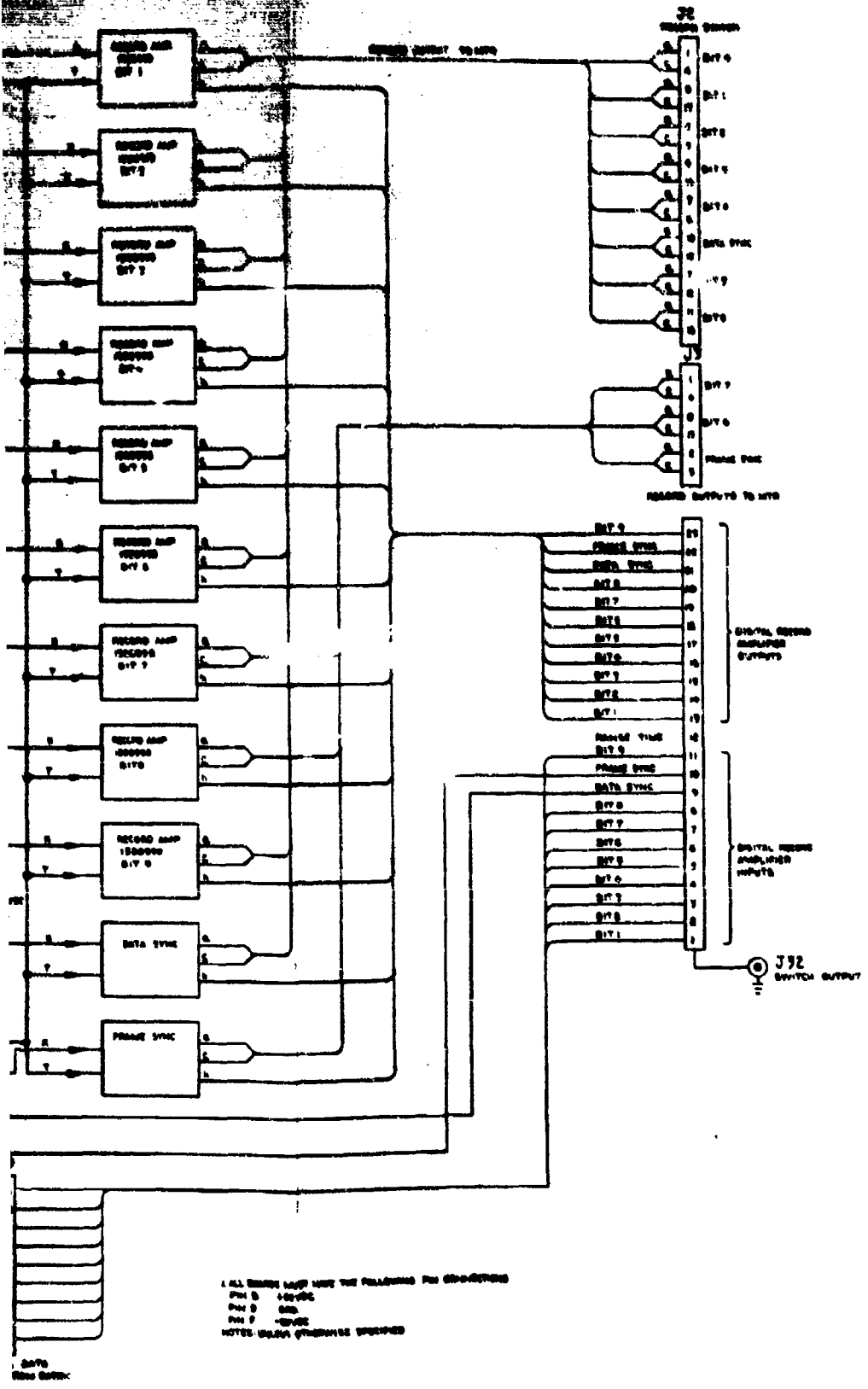
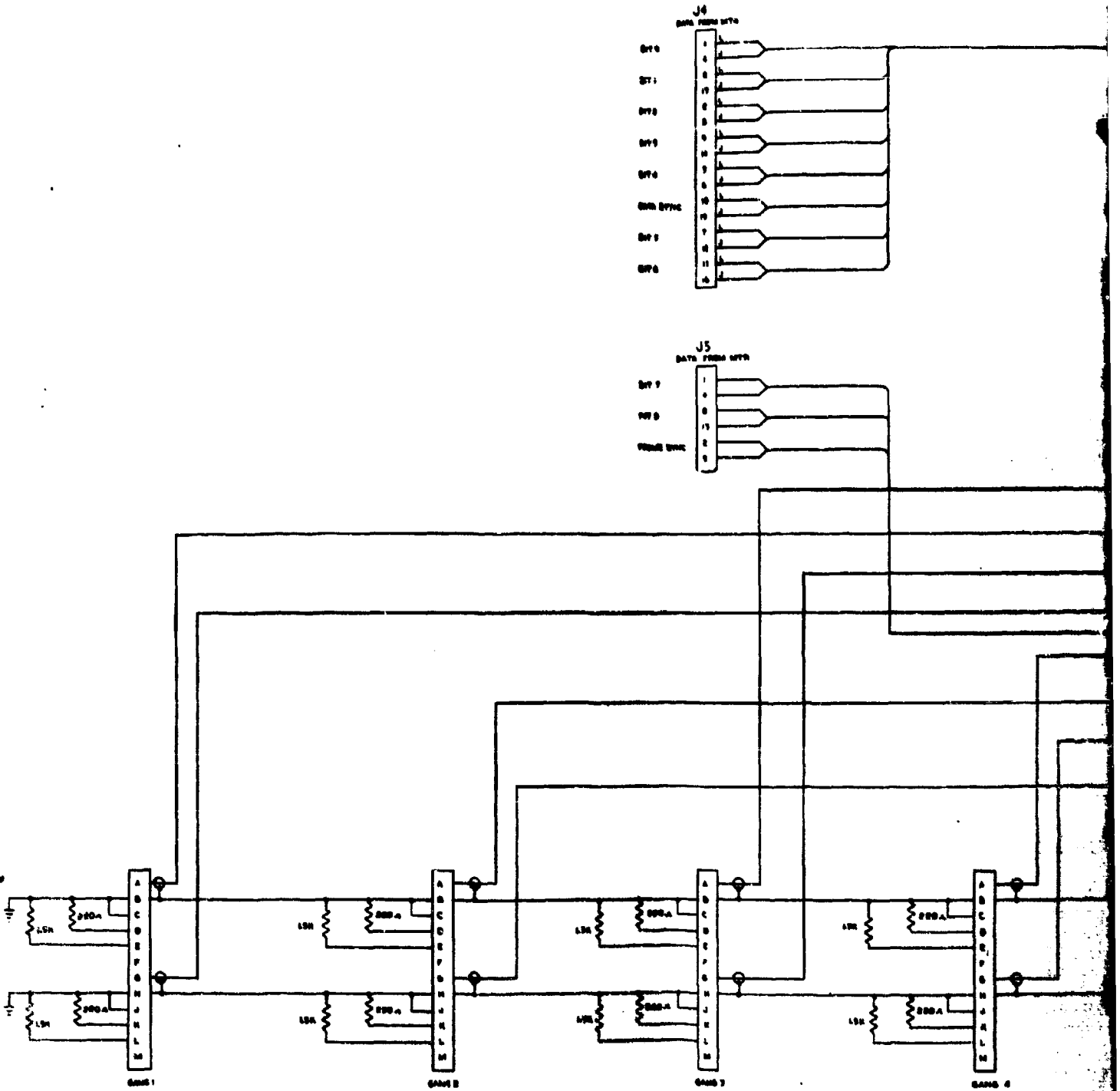
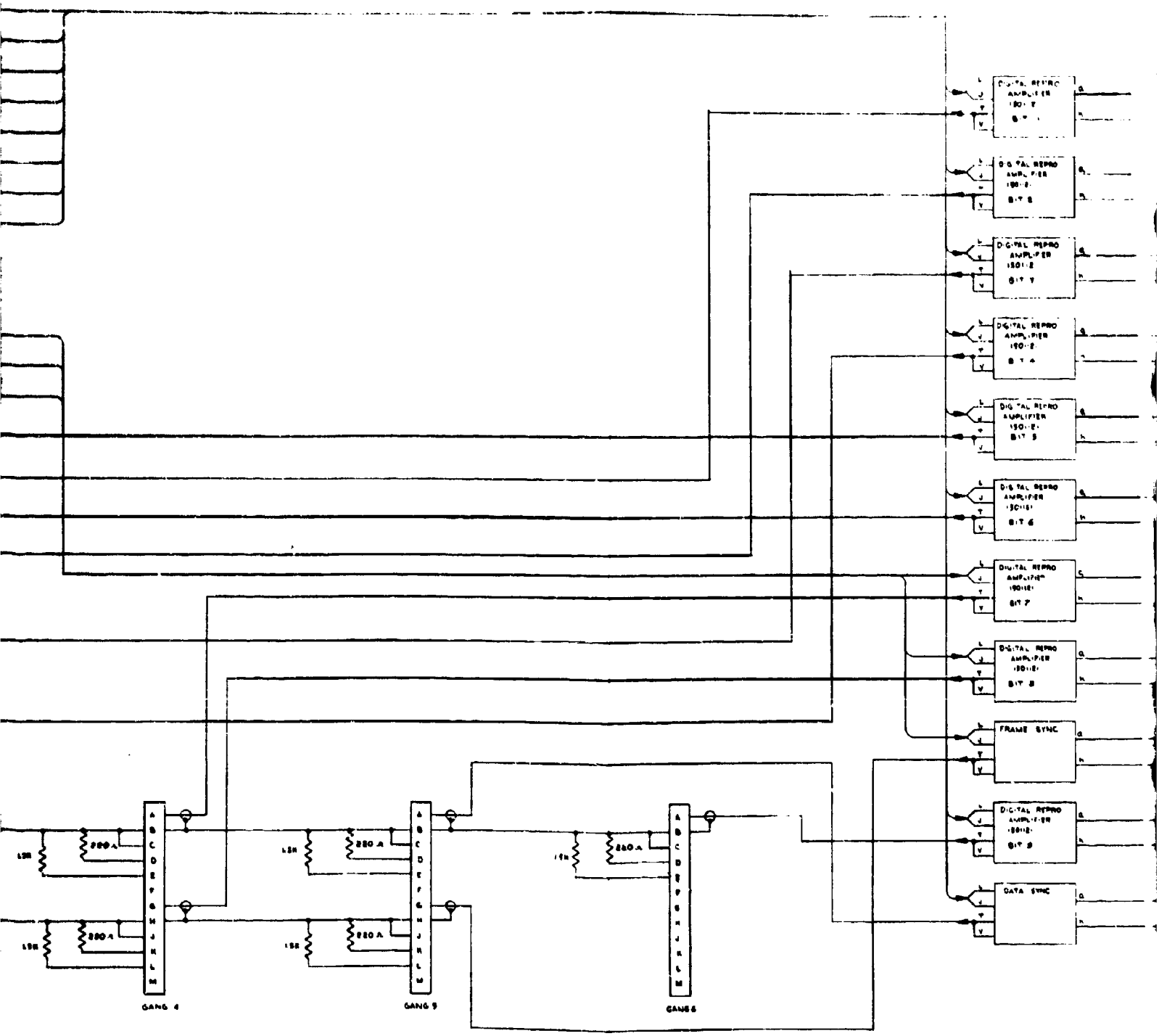


Fig. 10-5 Digital Record Electronics Wiring Block Diagram

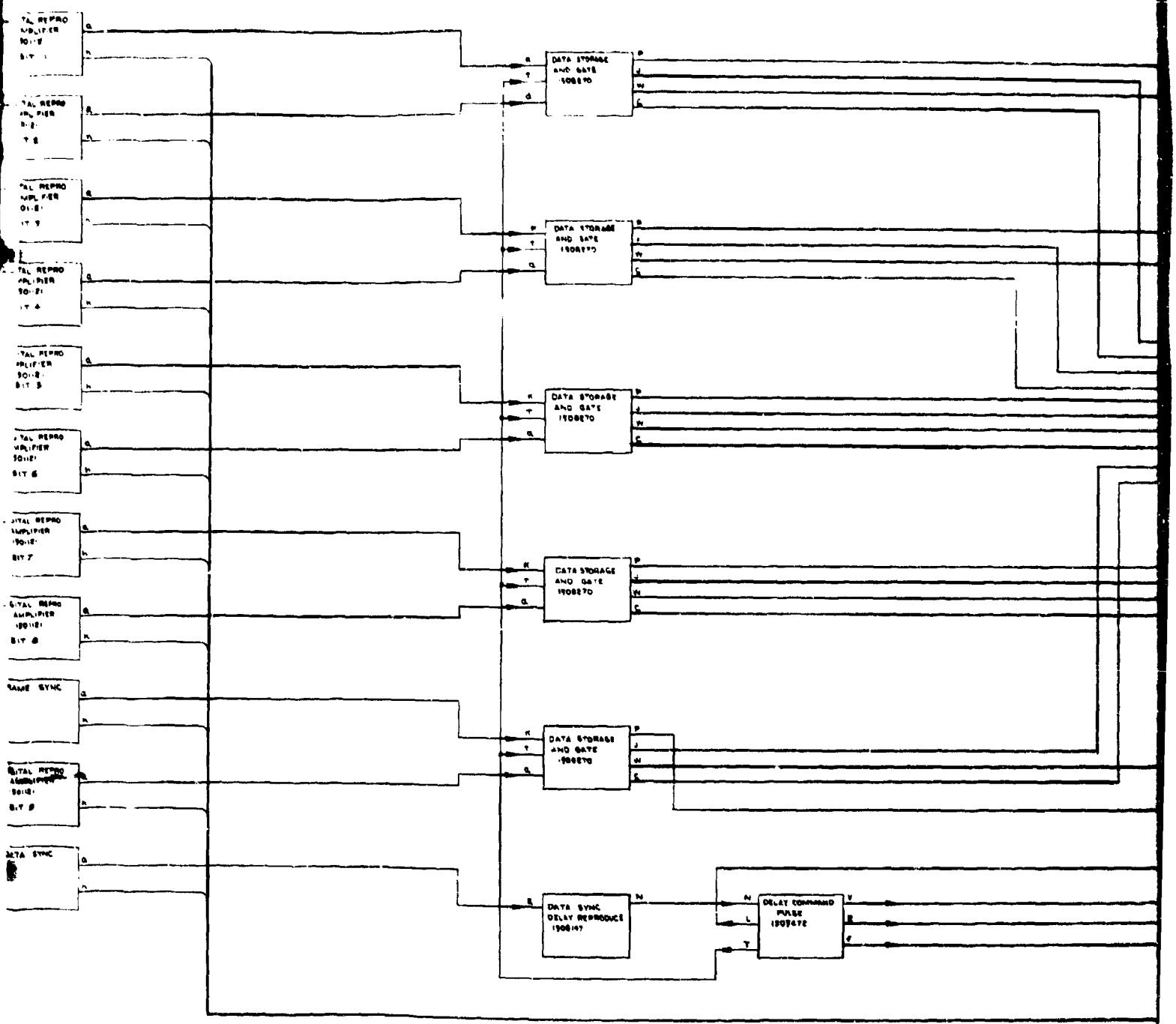


GAIN COMPENSATION SWITCH

A


DIGITAL REPRO AMPLIFIER 1501-E BIT 1
DIGITAL REPRO AMPLIFIER 1501-E BIT 2
DIGITAL REPRO AMPLIFIER 1501-E BIT 4
DIGITAL REPRO AMPLIFIER 1501-E BIT 5
DIGITAL REPRO AMPLIFIER 1501-E BIT 6
DIGITAL REPRO AMPLIFIER 1501-E BIT 7
DIGITAL REPRO AMPLIFIER 1501-E BIT 8
FRAME SYNC
DIGITAL REPRO AMPLIFIER 1501-E BIT 9
DATA SYNC
LSB
MSB
220 Ω
GANG 4
GANG 5
GANG 6

B


DATA STORAGE AND GATE 1908270
DATA STORAGE AND GATE 1908270
DATA STORAGE AND GATE 1908270
DATA STORAGE AND GATE 1908270
DATA STORAGE AND GATE 1908270
DATA SYNC DELAY REPRODUCE 1908197
DELAY COMMAND PULSE 1907672

C

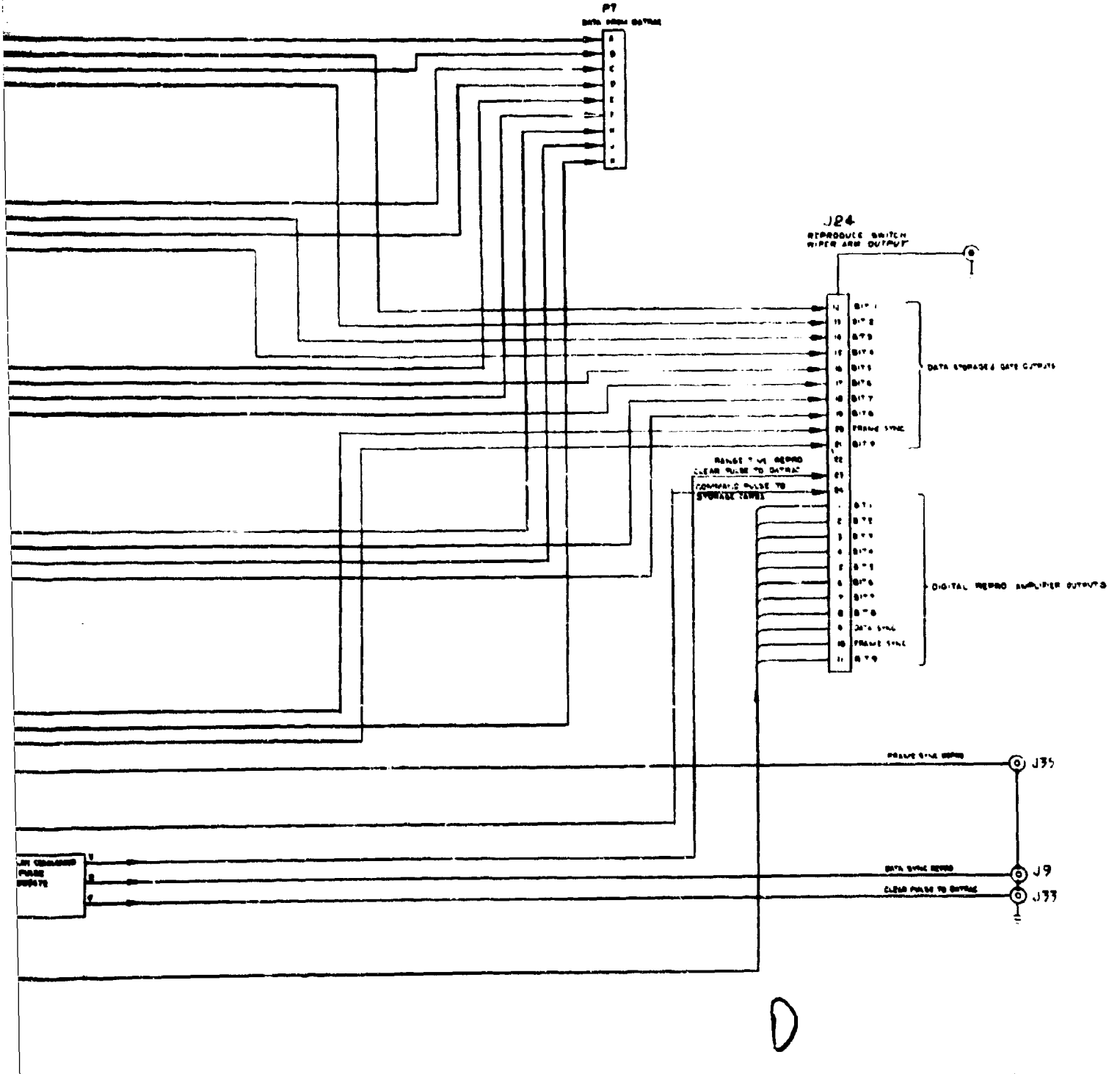
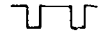
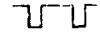
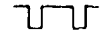
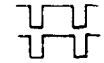
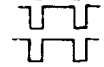
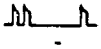
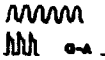


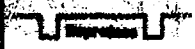
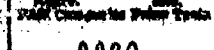
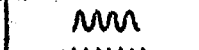
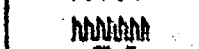
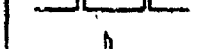
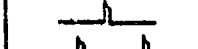
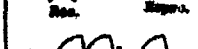
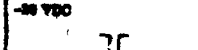
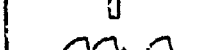
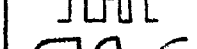
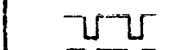
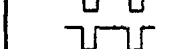
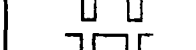
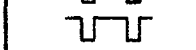
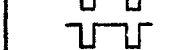
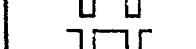
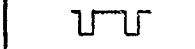
Fig. 10-6 Digital Reproducer Electronics Wiring Block Diagram

Section 11
MONITOR SWITCH OUTPUTS

MONITOR SWITCH OUTPUTS			
Switch Title and Position	Output From	Typical Output Waveform	Input To
MONITOR PANEL			
Switch A			
RCVR VID DC	Receiver	PAM Composite Pulse Train	Base Band Unit
DATRAC VID DC	Base Band Unit Noise Filter Amplifier	PAM Composite Pulse Train	Datrac
DATRAC COMMAND	Data Sync Delay Record (Demultiplexer)		Datrac
COMP FR SYNC	Sync Selector (Demultiplexer)		Frame Sync Storage Record (Record Electronics)
DATRAC BER OUTPUT	Datrac	Series of pulse groups every 50 msec (62.5 for G-A). Each group consists of 6-9 pulses, 3 μsec apart.	Monitor Point Only
DEMUL INPUT	Gate Driver Amplifier (Base Band Unit)	PAM Composite Pulse Train	Demultiplexer
REPRO AMPL - BIT 1	Digital Reproduce Amplifier - Bit 1		Data Storage and Gate - Bits 1 and 2
REPRO AMPL - BIT 2	Digital Reproduce Amplifier - Bit 2		Data Storage and Gate - Bits 1 and 2
REPRO AMPL - BIT 3	Digital Reproduce Amplifier - Bit 3		Data Storage and Gate - Bits 3 and 4
REPRO AMPL - BIT 4	Digital Reproduce Amplifier - Bit 4		Data Storage and Gate - Bits 3 and 4
REPRO AMPL - BIT 5	Digital Reproduce Amplifier - Bit 5		Data Storage and Gate - Bits 5 and 6
REPRO AMPL - BIT 6	Digital Reproduce Amplifier - Bit 6		Data Storage and Gate - Bits 5 and 6
REPRO AMPL - BIT 7	Digital Reproduce Amplifier - Bit 7		Data Storage and Gate - Bits 7 and 8
REPRO AMPL - BIT 8	Digital Reproduce Amplifier - Bit 8		Data Storage and Gate - Bits 7 and 8
REPRO AMPL - DATA SYNC	Digital Reproduce Amp Data Sync		Data Sync Delay Reproduce
REPRO AMPL - FR SYNC	Digital Reproduce Amplifier - Frame Sync		Data Storage and Gate - Frame Sync and Bit 9
REPRO AMPL - BIT 9	Digital Reproduce Amplifier - Bit 9		Data Storage and Gate - Frame Sync and Bit 9
REPRO AMPL - ANALOG VIDEO	Analog Reproduce Amplifier	Backup Only - PAM Composite Pulse Train	
SAMPLE AND HOLD - I	Switch 1 on Sample and Hold Monitor Panel	-	-
SAMPLE AND HOLD - II	Switch 2 on Sample and Hold Monitor Panel	-	-
Switch B			
RCVR VID DC	Receiver	PAM Composite Pulse Train	Base Band Unit
DATRAC VID DC	Base Band Unit Noise Filter Amplifier	PAM Composite Pulse Train	Datrac
DATRAC COMMAND	Data Sync Delay Record (Demultiplexer)		Datrac
COMP FR SYNC	Sync Selector (Demultiplexer)		Frame Sync Storage Record (Record Electronics)
VIB	Vibration Patch and Switch Panel	-	-
G-A-I	Switch G-A-I on G-A Monitor Switch Panel	-	-
G-A-II	Switch G-A-II on G-A Monitor Switch Panel	-	-
RECORD	RECORD SWITCH on Record and Reproduce Monitor Switch Panel	-	-
REPRODUCE	REPRODUCE SWITCH on Record and Reproduce Monitor Switch Panel	-	-
SYNC VID	Noise Filter Amplifier (Base Band Unit)	PAM Composite Pulse Train	Demultiplexer Sync Circuits
FR SYNC SEP	Frame Sync Separator (Demultiplexer)		Sync Logic
DATA SYNC FILTER	Envelope Filter of Data Sync Separator (Demultiplexer)		Monitor Point Only
DATA SYNC SEP	Data Sync Separator (Demultiplexer)	Vib. G-A 	Pulse Sequencers, Freq. Divider
PULSE AMPL INPUT	Datrac		Pulse Amplifier (Record Electronics)
PULSE AMPL OUTPUT	Pulse Amplifier		Digital Record Amplifiers

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11-2

	Frame Sync Storage Record		Digital Record Amplifier - Frame Sync
	Gated		Gate Driver Amplifier (Serial Read Unit)
	Data Gates - Main		Interpolation Filters and Display
	Data Gates - Main		Interpolation Filters and Display
	Data Gates - Telemetry		Interpolation Filters and Display
	Sync Gates (Demultiplexer)		Demultiplexer Sync Circuits
	Bit Sync Regenerator (Demultiplexer)		Monitor Point Only
	Data Sync Regenerator (Demultiplexer)		Pulse Sequencer, Freq. Divider (Demultiplexer)
	Frame Sync Regenerator (Demultiplexer)		Subcom Pulse Sequencer (Demultiplexer)
MAIN FR SYNC	Sync Gate (Demultiplexer)		Pulse Seq., Freq. Div., Progra.mmer, Zero Data Sel., (Demultiplexer)
SUBCOM FR SYNC	Subcom Sync Gate		Subcom Pulse Seq. (Demultiplexer)
FR SYNC REP MAIN DATA SEL	Frame Sync Reg. (Demultiplexer) Zero Data Sel. (Demultiplexer)		8-Bit Shift Reg., Sync Sel., (Demultiplexer) 1-Hz Filter of D C Ref. Feedback Loop
DIGITAL RECORD AMPLIFIER INPUT - BITS 1 THROUGH 8	Decom Digital Output		Digital Record Amplifier Bits 1 through 8
DIGITAL RECORD AMPLIFIER INPUT - DATA SYNC		-30 VDC	Digital Record Amplifier Data Sync
DIGITAL RECORD AMPLIFIER INPUT - FR SYNC	Frame Sync Storage Record (Record Electronics)		Digital Record Amplifier Frame Sync
DIGITAL RECORD AMPLIFIER INPUT - BIT 9	Decom Digital Output		Digital Record Amplifier - Bit 9
DIGITAL RECORD AMPLIFIER OUTPUT - BITS 1 THROUGH 8	Digital Record Amplifier Bits 1 through 8		Magnetic Tape Recorder Record Head
DIGITAL RECORD AMPLIFIER OUTPUT - DATA SYNC	Digital Record Amplifier - Data Sync		Magnetic Tape Recorder Record Head
DIGITAL RECORD AMPLIFIER OUTPUT - FR SYNC	Digital Record Amplifier - Frame Sync		Magnetic Tape Recorder Record Head
DIGITAL RECORD AMPLIFIER OUTPUT - BIT 9	Digital Record Amplifier - Bit 9		Magnetic Tape Recorder Record Head
DIGITAL REPRODUCE AMPLIFIER OUTPUT - BIT 1	Digital Reproduce Amplifier - Bit 1		Data Storage and Gate - Bits 1 and 2
DIGITAL REPRODUCE AMPLIFIER OUTPUT - BIT 2	Digital Reproduce Amplifier - Bit 2		Data Storage and Gate - Bits 1 and 2
DIGITAL REPRODUCE AMPLIFIER OUTPUT - BIT 3	Digital Reproduce Amplifier - Bit 3		Data Storage and Gate - Bits 3 and 4
DIGITAL REPRODUCE AMPLIFIER OUTPUT - BIT 4	Digital Reproduce Amplifier - Bit 4		Data Storage and Gate - Bits 3 and 4
DIGITAL REPRODUCE AMPLIFIER OUTPUT - BIT 5	Digital Reproduce Amplifier - Bit 5		Data Storage and Gate - Bits 5 and 6
DIGITAL REPRODUCE AMPLIFIER OUTPUT - BIT 6	Digital Reproduce Amplifier - Bit 6		Data Storage and Gate - Bits 5 and 6
DIGITAL REPRODUCE AMPLIFIER OUTPUT - BIT 7	Digital Reproduce Amplifier - Bit 7		Data Storage and Gate - Bits 7 and 8
DIGITAL REPRODUCE AMPLIFIER OUTPUT - BIT 8	Digital Reproduce Amplifier - Bit 8		Data Storage and Gate - Bits 7 and 8
DIGITAL REPRODUCE AMPLIFIER OUTPUT - DATA SYNC	Digital Reproduce Amplifier - Data Sync		Data Sync Delay Reproduce
DIGITAL REPRODUCE AMPLIFIER OUTPUT - FR SYNC	Digital Reproduce Amplifier - Frame Sync		Data Storage and Gate - Frame Sync and Bit 9
DIGITAL REPRODUCE AMPLIFIER OUTPUT - BIT 9	Digital Reproduce Amplifier - Bit 9		Data Storage and Gate - Frame Sync and Bit 9
DATA STORAGE AND GATE OUTPUT - BIT 1	Data Storage and Gate - Bits 1 and 2		Decom Digital Input

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11-4

MONITOR SWITCH OUTPUTS			
Switch Title and Position	Output From	Typical Output Waveform	Input To
DATA STORAGE AND GATE OUTPUT – BIT 1	Data Storage and Gate – Bits 1 and 2		Bstrom Digital Input
DATA STORAGE AND GATE OUTPUT – BIT 2	Data Storage and Gate – Bits 3 and 4		Bstrom Digital Input
DATA STORAGE AND GATE OUTPUT – BIT 4	Data Storage and Gate – Bits 5 and 6		Bstrom Digital Input
DATA STORAGE AND GATE OUTPUT – BIT 5	Data Storage and Gate – Bits 5 and 8		Bstrom Digital Input
DATA STORAGE AND GATE OUTPUT – BIT 6	Data Storage and Gate – Bits 9 and 8		Bstrom Digital Input
DATA STORAGE AND GATE OUTPUT – BIT 7	Data Storage and Gate – Bits 9 and 8		Bstrom Digital Input
DATA STORAGE AND GATE OUTPUT – BIT 8	Data Storage and Gate – Bits 7 and 8		Bstrom Digital Input
DATA STORAGE AND GATE OUTPUT – FR SYNC	Data Storage and Gate – Frame Sync and Bit 8		Sync Selector, Sync Gate (Demultiplexer)
DATA STORAGE AND GATE OUTPUT – BIT 9	Data Storage and Gate – Frame Sync and Bit 8		Bstrom Digital Input
CLEAR PULSE TO DATRAC	Delay Command Pulse (Reproducer Electronics)		Bstrom
COMMAND PULSE TO STORAGE CARDS	Delay Command Pulse (Reproducer Electronics)		Data Storage and Gate (Reproducer Electronics)
C-A MONITOR SWITCH PANEL			
S-A-J			
HIGH FREQUENCY DATA GATES 1 THROUGH 32	Data Gates (Demultiplexer)	Record / Repro.	Sample and Hold (Demultiplexer)
S-A-H			
HIGH FREQUENCY DATA GATES 34 THROUGH 63	Data Gates (Demultiplexer)	Record / Repro.	Sample and Hold (Demultiplexer)
SUB COMM DATA GATES 1 THROUGH 8	Data Gates (Demultiplexer)	Record / Repro.	Sample and Hold (Demultiplexer)
SYNC GATE	Sync Gate (Demultiplexer)		Pulse Sequencer (Demultiplexer)
DATA SYNC SEP	Data Sync Separator (Demultiplexer)		6-Bit Shift Register and Pulse Set (Demultiplexer)
HIGH SPEED SEQ INPUT	Data Sync Separator (Demultiplexer)		High-Speed Pulse Sequencer (Demultiplexer)
LOW SPEED SEQ INPUT	Pulse Set and Frequency Divider (Demultiplexer)		Low-Speed Pulse Sequencer (Demultiplexer)
SUB COMM SEQ INPUT	Pulse Set and Low-Speed Pulse Sequencer (Demultiplexer)		Subcom Pulse Sequencer (Demultiplexer)
SUB COMM SEQ RESET	Subcom Sync Gate (Demultiplexer)		Subcom Pulse Sequencer (Demultiplexer)
SAMPLE AND HOLD MONITOR PANEL			
Switch 1			
HIGH FREQUENCY CHANNELS 1 THROUGH 32	High Frequency Data Gates (Demultiplexer)		Sample and Hold (Demultiplexer)
Switch 2			
HIGH FREQUENCY CHANNELS 34 THROUGH 63	High Frequency Data Gates (Demultiplexer)		Sample and Hold (Demultiplexer)
SUB COMM CHANNELS 1 THROUGH 8	Subcom Data Gates (Demultiplexer)		Sample and Hold (Demultiplexer)

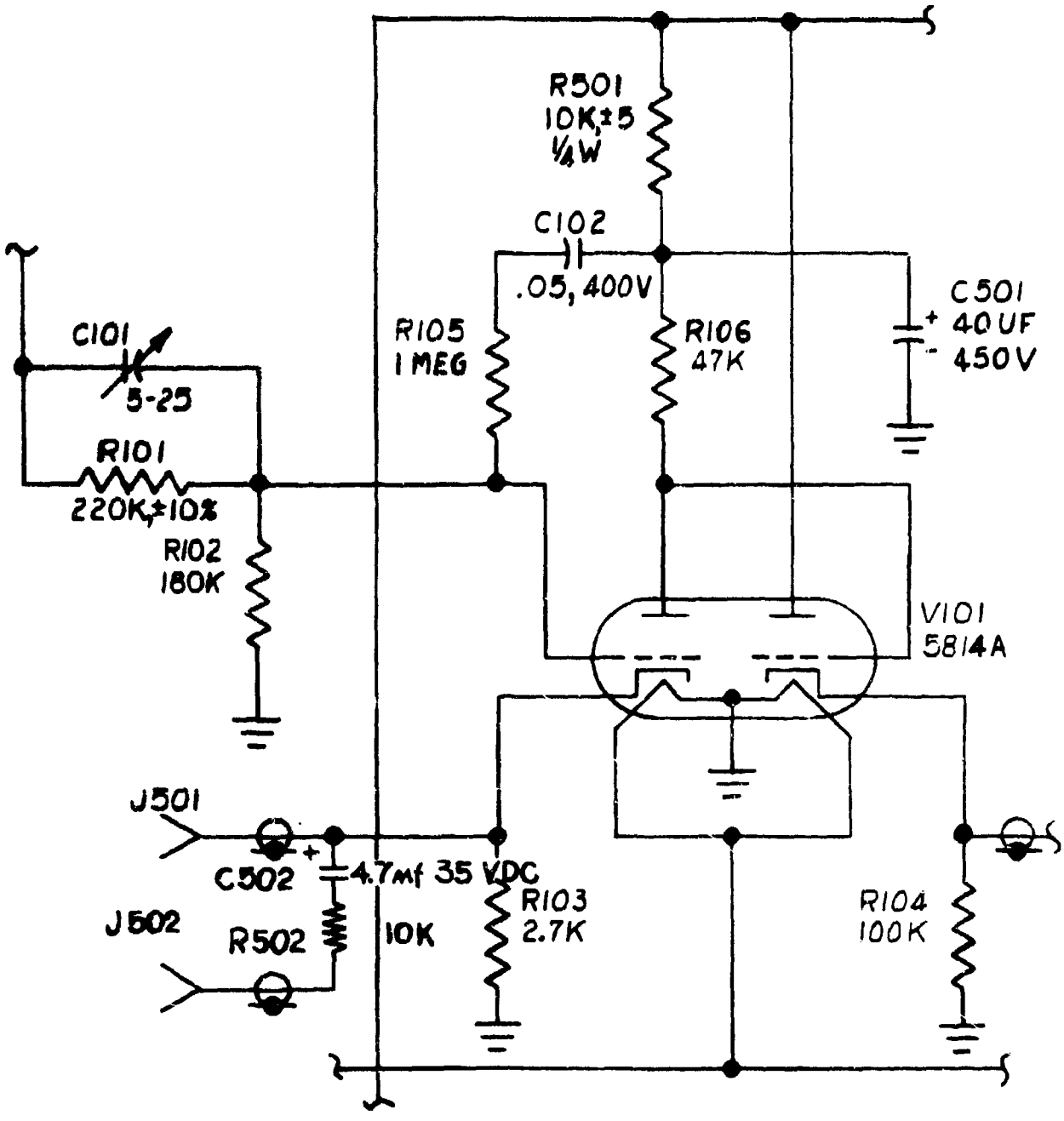
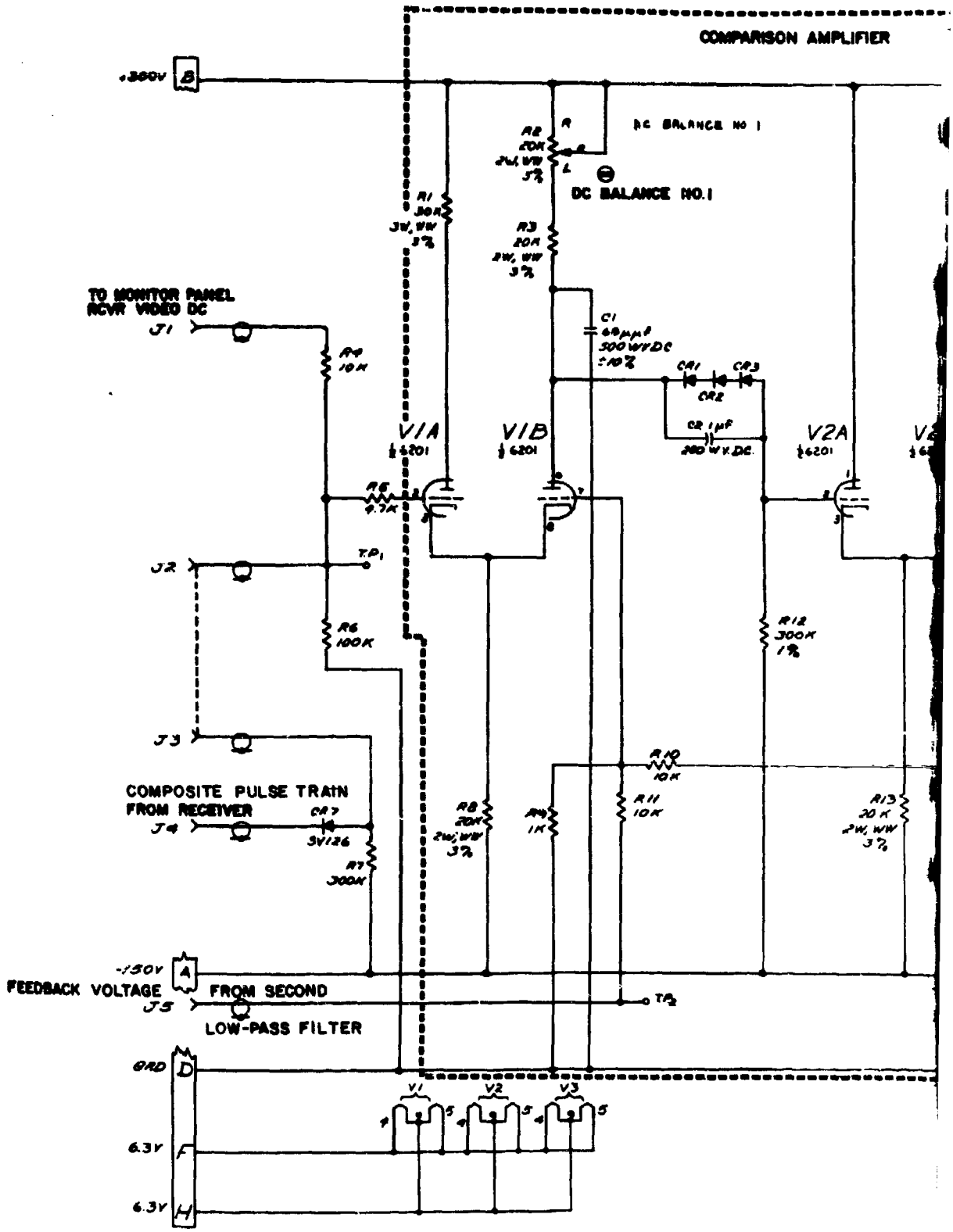


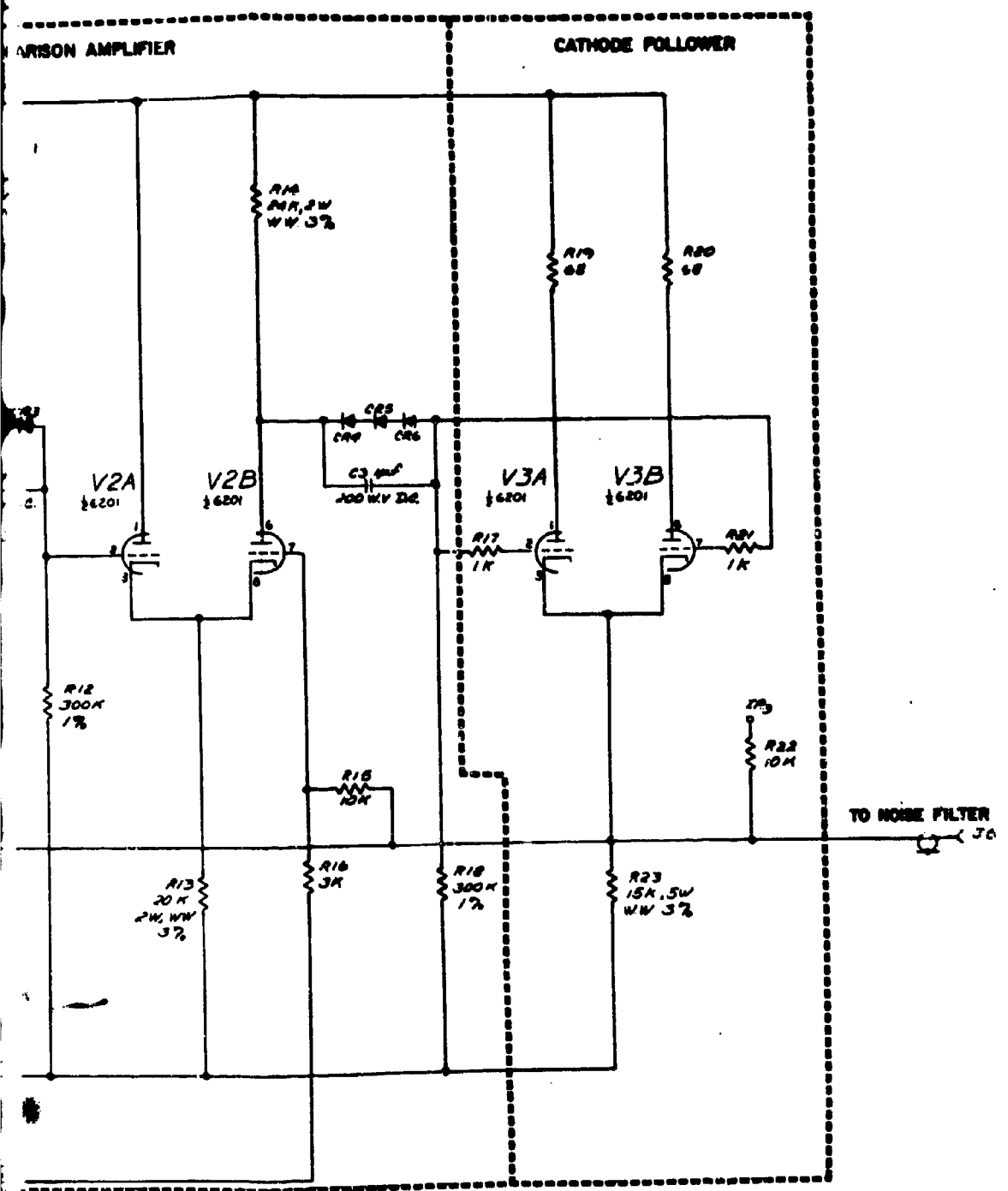
Fig. A-1 Receiver Modifications

PARTS LIST

Reference Designation	Part No.	Vendor or MIL Spec.
C1	DM15-680	El Menco, Los Angeles, Calif.
C2, 3	PM2W1	Cornell-Dubilier, Plainfield, N.J.
CR1 thru 6	1N1323	Hoffman Electronics, Los Angeles, Calif.
CR7	SV126	Transitron, Wakefield, Mass.
V1, 2, 3	6201 5 Star	G. E. , Owensboro, Ky.
J1 thru J6	BNC	Amphenol, Chicago, Ill.
R1	RLS-2	Dale Products, Columbus, Nebraska
R2	43C2-20K	Clarostat Mfg. Co., Dover, N. H.
R3, 8, 13	RLS-2A	Dale Products, Columbus, Nebraska
R4, 10, 11, 15, 22	RC20GF	Allen-Bradley, Milwaukee, Wisc.
R5	RC20GF	Allen-Bradley, Milwaukee, Wisc.
R6	RC20GF	Allen-Bradley, Milwaukee, Wisc.
R7	RC20GF	Allen-Bradley, Milwaukee, Wisc.
R9, 17, 21	RC20GF	Allen-Bradley, Milwaukee, Wisc.
R12, 18	DCMH-1/2	Dale Products, Columbus, Nebr.
R14	RLS-2A	Dale Products, Columbus, Nebr.
R16	RC20GF	Allen-Bradley, Milwaukee, Wisc.
R19, 20	RC20GF	Allen-Bradley, Milwaukee, Wisc.
R23	RLS-5	Dale Products, Columbus, Nebr.


COMPARISON AMPLIFIER
+300V
B
R2 20K 2W, WW 3%
R
L
DC BALANCE NO 1
DC BALANCE NO.1
R1 30K 3W, WW 3%
R3 20K 2W, WW 3%
TO MONITOR PANEL RCVR VIDEO DC
J1
R4 10K
C1 68μμF 500 WV DC ±10%
CR1
CR3
CR2
CR 1μF 200 W.V. DC.
V1A
½ 6201
V1B
½ 6201
V2A
½ 6201
R5 9.7K
J2
T.P.1
R6 100K
R12 300K 1%
J3
R10 10K
COMPOSITE PULSE TRAIN FROM RECEIVER
J4
CR7
3V126
R7 300K
R8 20K 2W, WW 3%
R9 1K
R11 10K
R13 20 K 2W, WW 3%
-150V
A
FEEDBACK VOLTAGE
FROM SECOND
J5
LOW-PASS FILTER
T.P.2
GRD
D
6.3V
F
6.3V
H
V1
V2
V3

B



NOTES: UNLESS OTHERWISE SPECIFIED

1. TP- TEST POINT
2. ⊕ INDICATES SCREWDRIVER CONTROL
3. ALL RESISTANCE VALUES ARE IN OHMS, 1/2 WATT 5% (K=1000)
4. DIODES ARE IN1323

Fig. A-2 DC Amplifier

FRQ
AMP

PARTS LIST

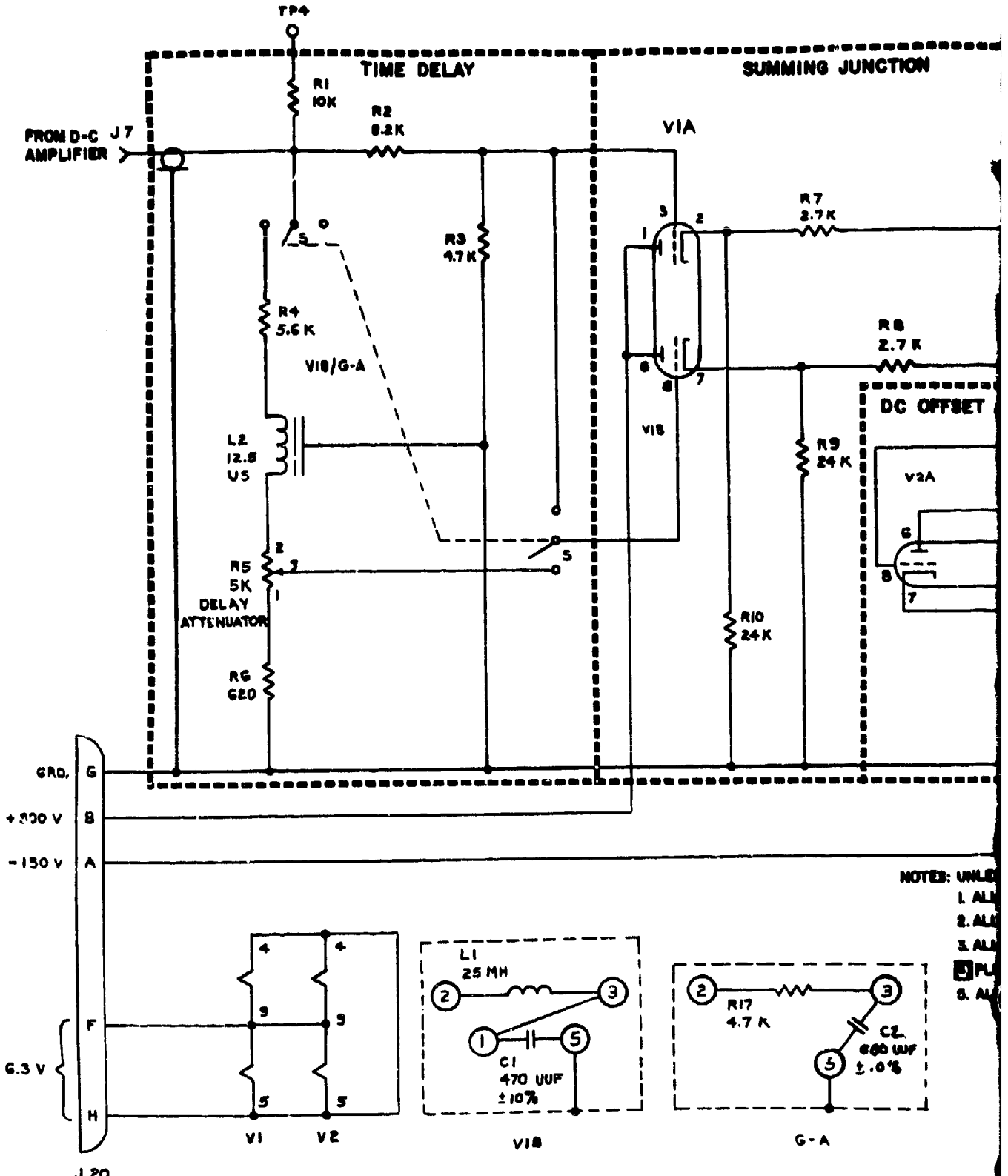
Reference Designation	Part No.	Vendor or MIL Spec
C1, 2	DM15	El Menco, Los Angeles, Calif.
C3	14OR12	Johnson Co. Waseca, Minn.
V1, 2	6463 5 Star	G. E. Owensboro, Ky.
L1	T1884	Freed Transformer Co., Brooklyn, N. Y.
L2	457G	Admiral, Palo Alto, Calif.
R1	MS35043-111	MIL-R-11
R2	MS35043-109	MIL-R-11
R3, 17	MS35043-103	MIL-R-11
R4	MS35043-105	MIL-R-11
R5	Series A with shaft lock and slotted shaft Helipot	
R6	MS35043-621	MIL-R-11
R7, 8, 14	MS35043-272	MIL-R-11
R9, 10	MS35043-120	MIL-R-11
R11	13F150	Ohmite Mfg. Co., Skokie, Ill.
R12	MS35043-682	MIL-R-11
R13	JLU	Allen-Bradley, Milwaukee, Wisconsin
R15	MS35043-104	MIL-R-11
R16	MS35043-511	MIL-R-11

GR

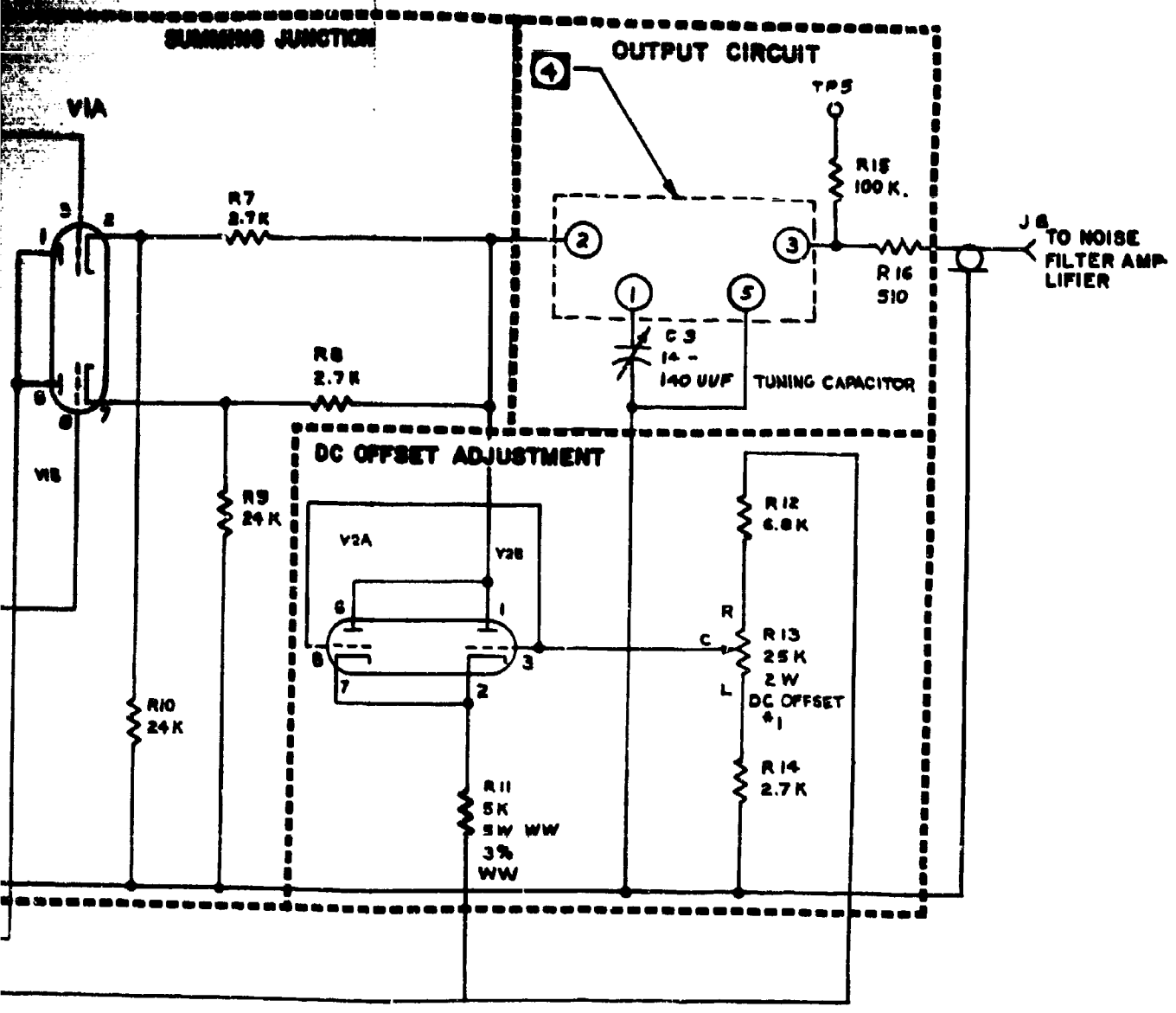
+ 300 V

- 150

6.3 V

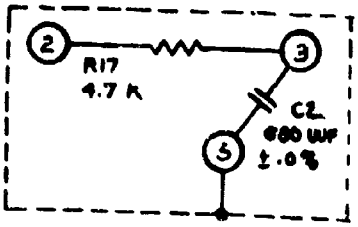

TP4
TIME DELAY
SUMMING JUNCTION
R1
10K
R2
8.2K
FROM D-C AMPLIFIER J7
VIA
R7
2.7K
R3
4.7K
R4
5.6K
V1B/G-A
R8
2.7K
DC OFFSET
L2
12.5
U5
V1B
R9
24K
V2A
R5
5K
DELAY
ATTENUATOR
R10
24K
RG
620
GRD. G
+300 V B
-150 V A
6.3 V F
H
J 20
V1
V2
L1
25 MH
C1
470 UUF
±10%
V1B
R17
4.7 K
C2
680 UUF
±.0%
G-A
NOTES: UNLE
1. ALL
2. ALL
3. ALL
5. PL
6. AL

B



NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTANCE VALUES IN OHMS (K=1000)
2. ALL CAPACITANCE VALUES IN MICROMICROFARADS
3. ALL RESISTORS 1/2 WATT CARBON ±5% TOL.
4. PLUG IN VIBRATION UNIT OR G-A UNIT HERE
5. ALL TUBES TYPE 6463



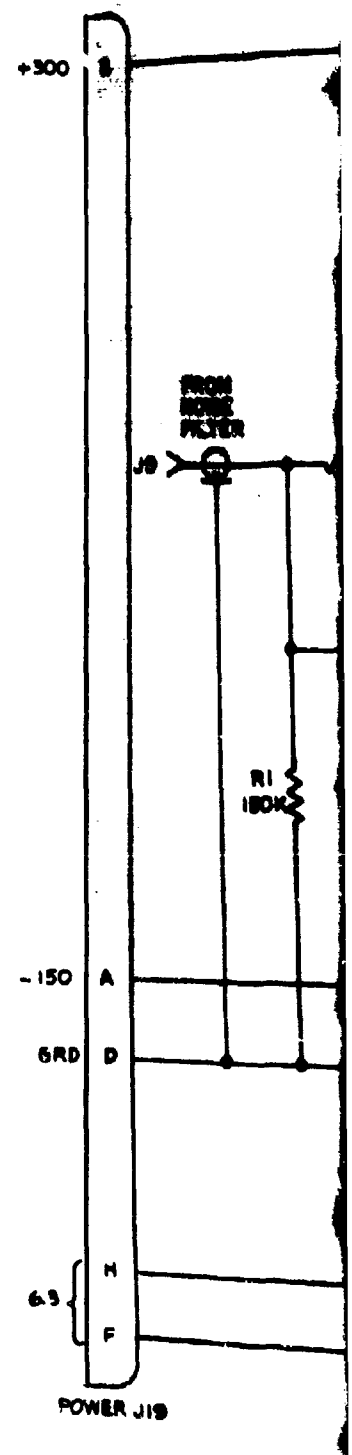
G-A

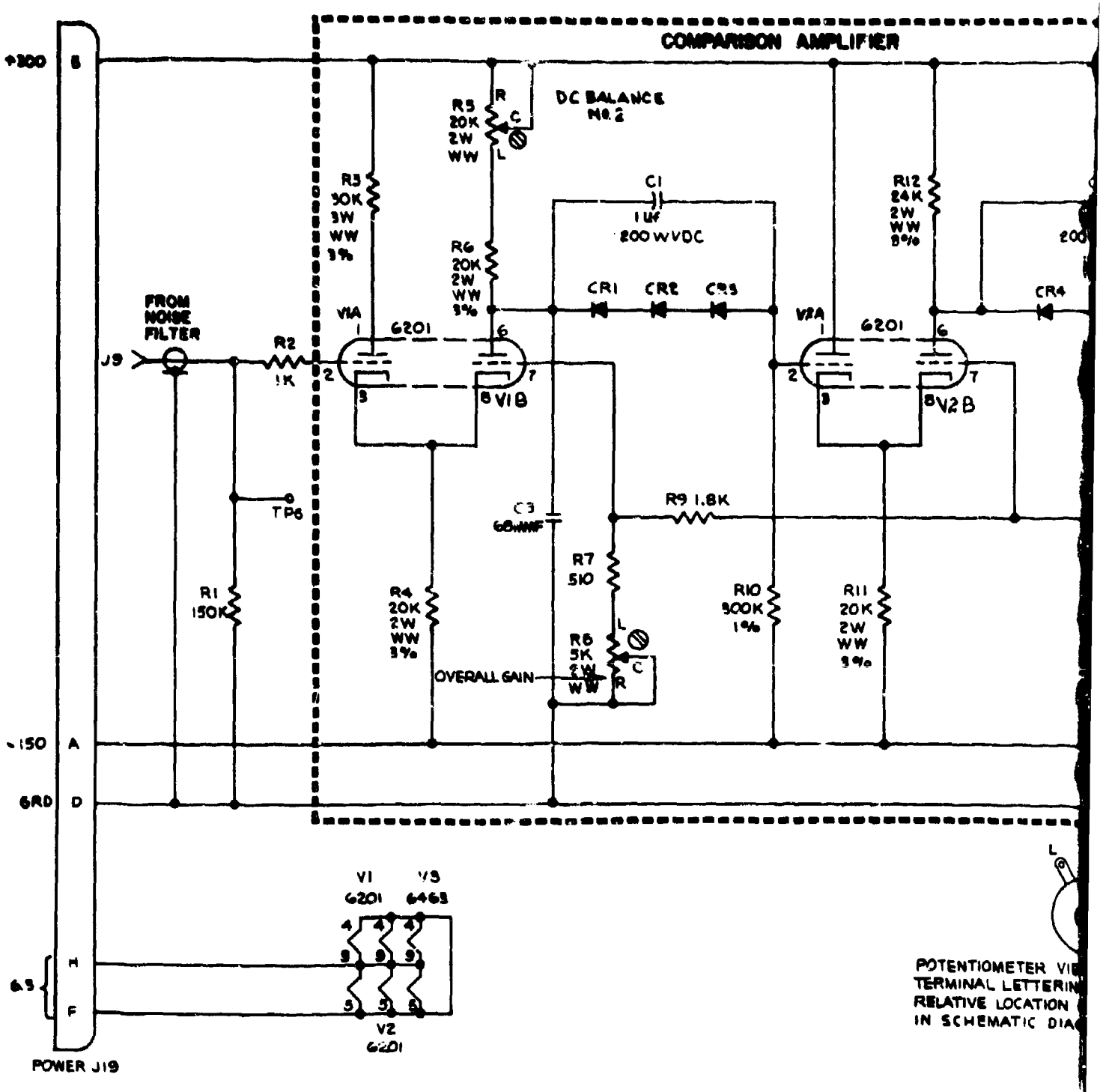
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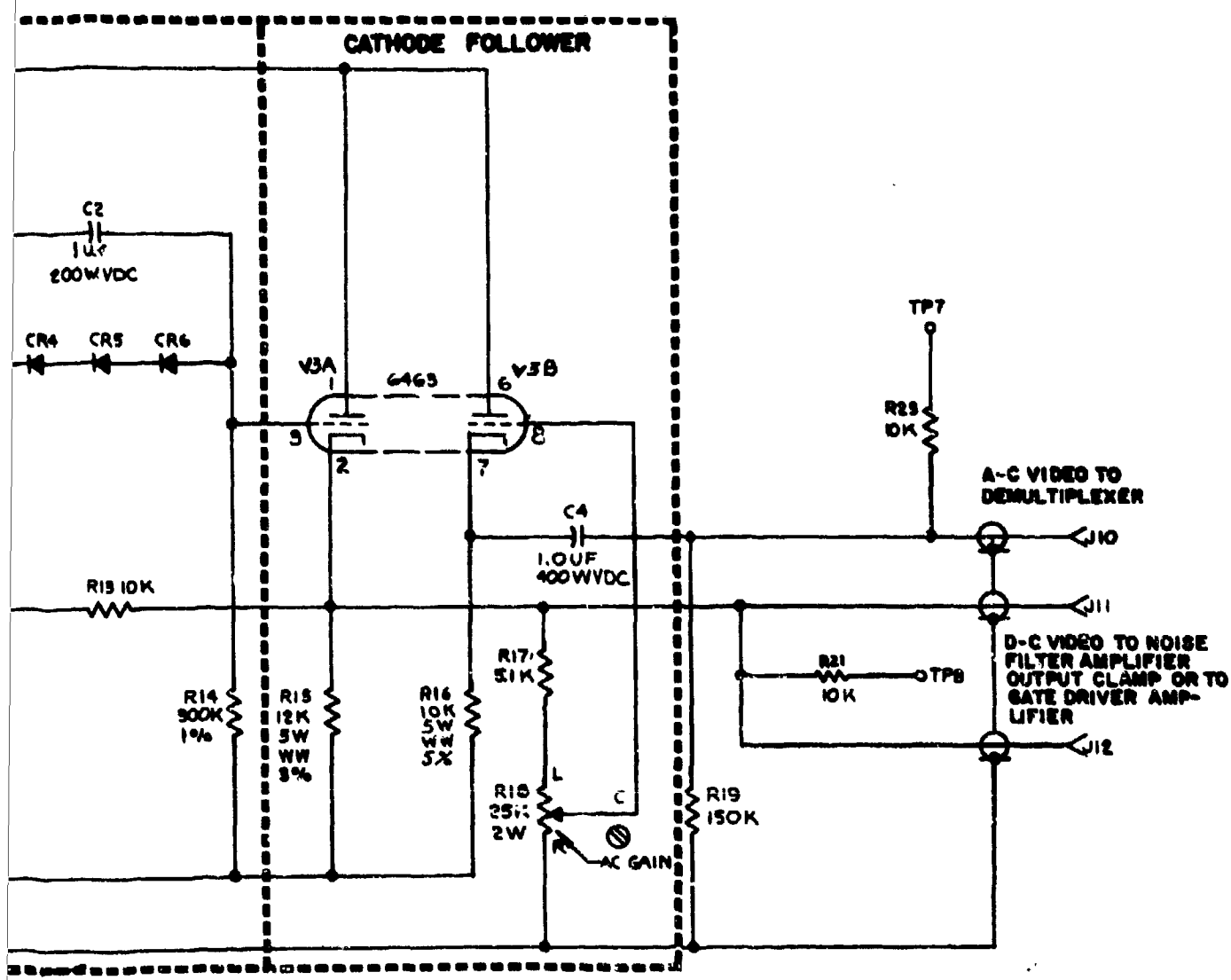
Fig. A-3 Noise Filter

PARTS LIST

Reference Designation	Part No.	Vendor or MIL Spec
C1, 2	PM2W1	Cornell-Dubilier, Plainfield, N. J.
C3	DM15-680	El Menco, Los Angeles, Calif.
C4	PM4W1	Cornell-Dubilier, Plainfield, N. J.
CR1 thru 6	ZA-60-2	Hoffman Electronics, Los Angeles, Calif.
V1, 2	6201	General Electric, Owensboro, Ky.
V3	6463	General Electric, Owensboro, Ky.
R1, 19	MS35043-139	MIL-R-11
R2	MS35043-87	MIL-R-11
R3	RLS-2	Dale Products, Columbus, Nebr.
R4, 6, 11	RLS-2A	Dale Products, Columbus, Nebr.
R5	43C2-20K	Clarostat Mfg. Co., Dover, N. H.
R7	MS35043-118	MIL-R-11
R8	JLU5021	Allen-Bradley, Milwaukee, Wisc.
R9	MS35043-93	MIL-R-11
R10, 14	MS35043-146	MIL-R-11
R12, 13, 21, 23	MS35043-111	MIL-R-11
R15	RLS-5	Dale Products, Columbus, Nebr.
R16	13F150	Ohmite, Chicago, Ill.
R17	MS35043-87	MIL-R-11
R18	JLU2531	Allen-Bradley, Milwaukee, Wisc.




COMPARISON AMPLIFIER
+300
B
DC BALANCE
R5
20K
2W
WW
R
C
L
R3
30K
3W
WW
3%
C1
1 UF
200 WVDC
R12
24K
2W
WW
3%
R6
20K
2W
WW
3%
CR1
CR2
CR3
CR4
FROM
NOISE
FILTER
J9
R2
1K
V1A
6201
V1B
V2A
6201
V2B
TP6
C3
68MMF
R9 1.8K
R7
510
R8
5K
2W
WW
OVERALL GAIN
R1
150K
R4
20K
2W
WW
3%
R10
900K
1%
R11
20K
2W
WW
3%
-150
A
GRD
D
H
6.3
F
POWER J19
V1
6201
V3
6463
V2
6201
POTENTIOMETER VI
TERMINAL LETTERIN
RELATIVE LOCATION
IN SCHEMATIC DIA





TER VIEWED FROM SHAFT END.
ETTERING FOR REFERENCE ONLY.
CATION OF TERMINALS SHOWN
TIC DIAGRAM.

NOTES: UNLESS OTHERWISE SPECIFIED
1-⊘ INDICATES SCREWDRIVER CONTROL
2- ALL RESISTORS 1/2 WATT 5%

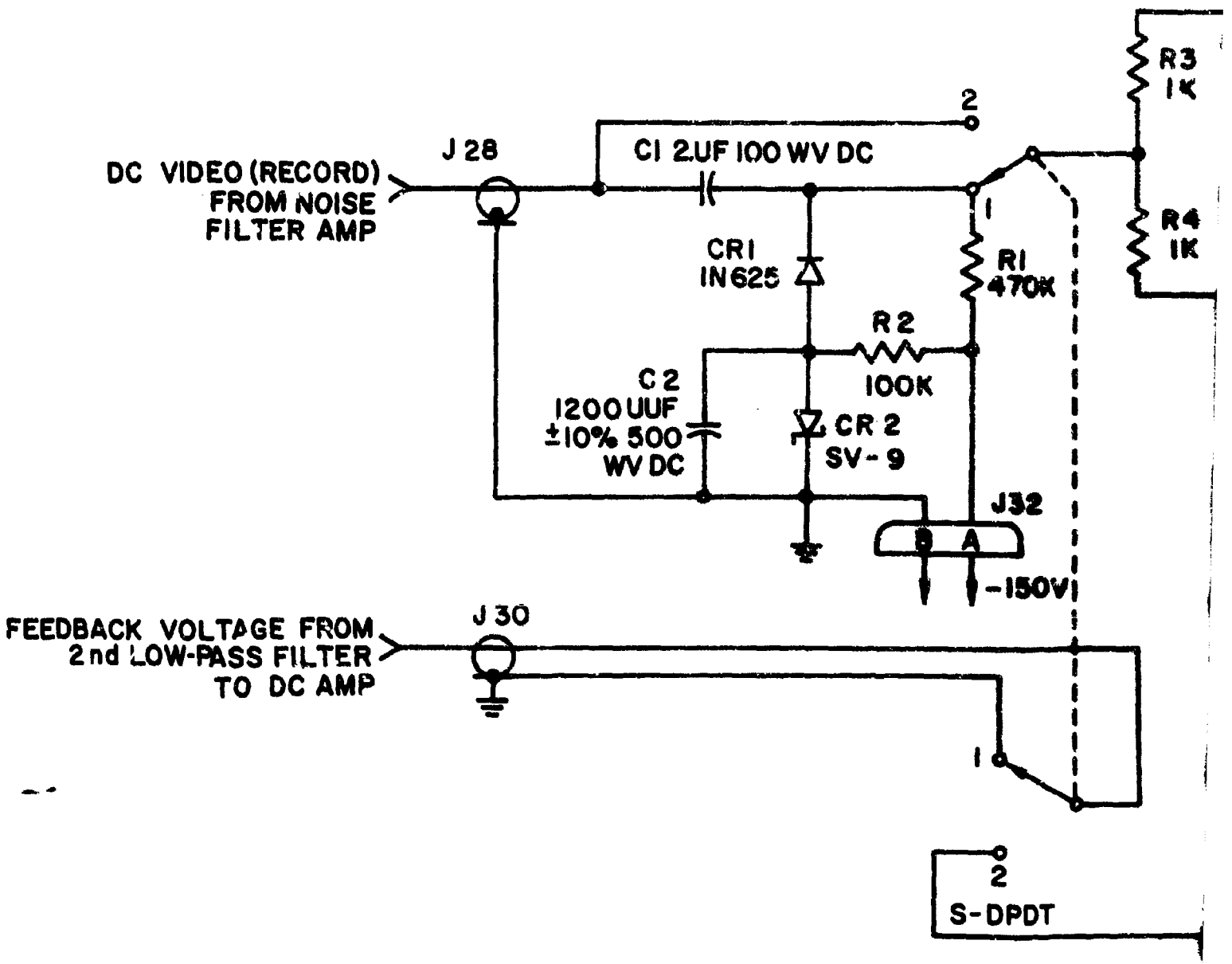
Fig. A-4 Noise Filter Amplifier

PARTS LIST

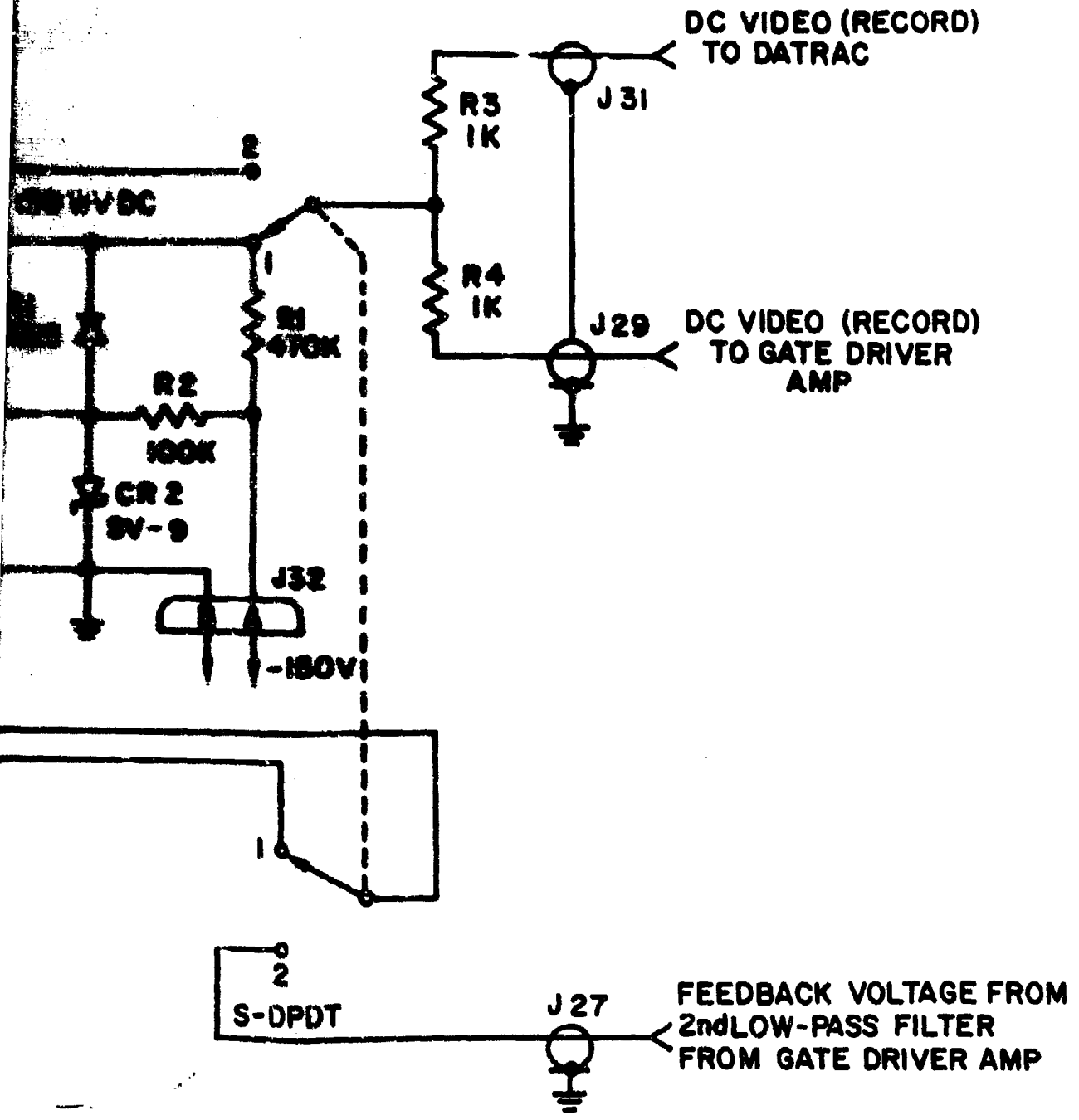
Reference Designation	Part No.	Vendor or MIL Spec
C1	E1-205-D	Electron Products Co., Pasadena, Calif.
C2	DM19E122K	El Menco, Willimantic, Conn.
CR1	1N325	Pacific Semiconductor, Culver City, Calif.
CR2	SV-9	Transitron, Wakefield, Mass.
R1	MS35043-151	MIL-R-11
R2	MS35043-135	MIL-R-11
E1	1423	Litton Ind., Los Angeles, Calif.
F1	1410-6	Herman H. Smith Co., Brooklyn, N.Y.
K1	8825K5	Cutler-Hammer Controls, Milwaukee, Wisc.
J27 thru 31	UG-1094/U	Tru Connector Co., Lynn, Mass.
J32	MPR 4P-LR	Winchester Electronics, Norwalk, Conn.

FEE

A


DC VIDEO (RECORD)
FROM NOISE
FILTER AMP
J 28
C1 2.UF 100 WV DC
2
1
R3
1K
R4
1K
CR1
IN625
R1
470K
R2
100K
C2
1200 UUF
±10% 500
WV DC
CR 2
SV-9
J32
B
A
-150V
FEEDBACK VOLTAGE FROM
2nd LOW-PASS FILTER
TO DC AMP
J 30
1
2
S-DPDT

B



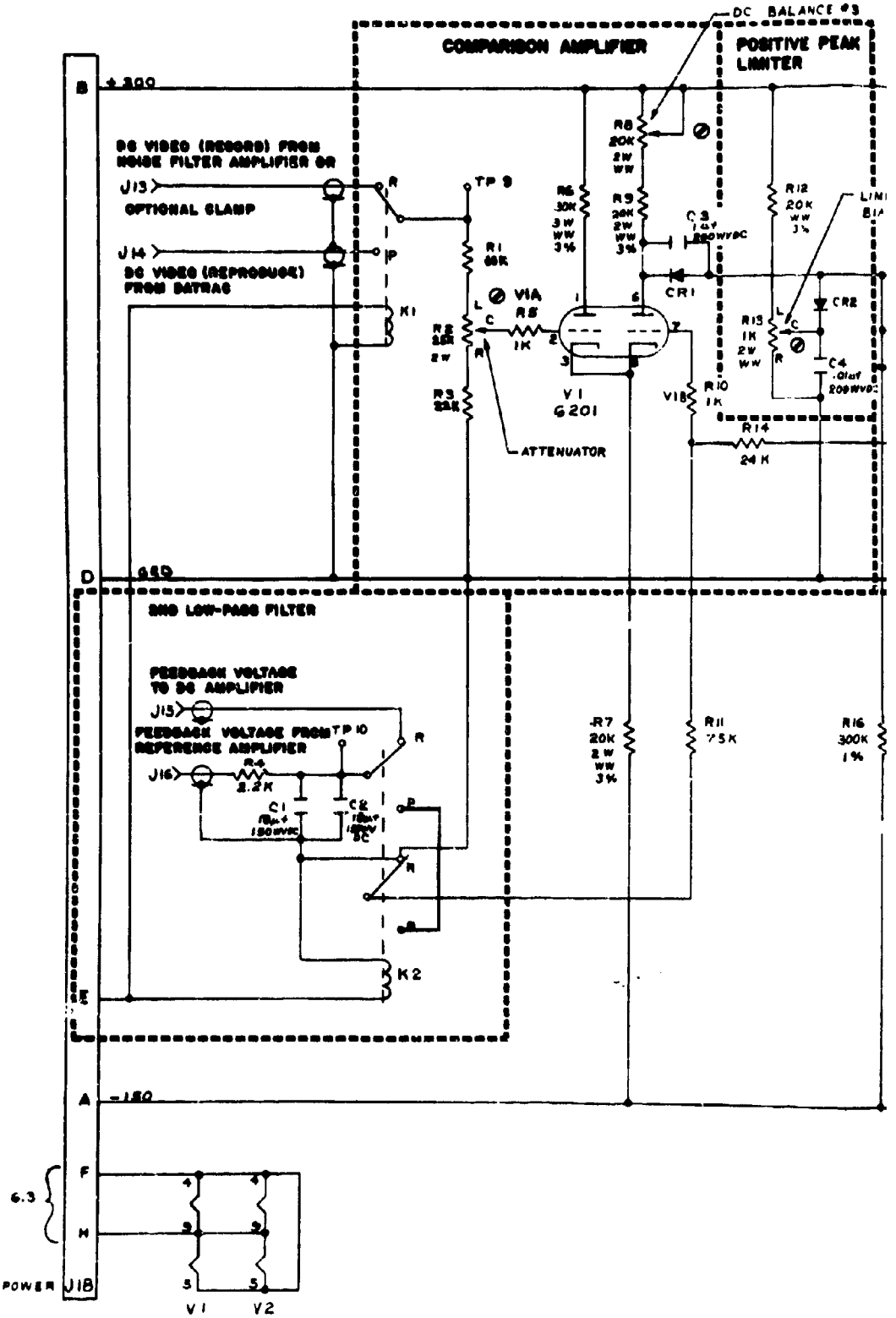
C

Fig. A-5 Reference Voltage Optional Clamp

PARTS LIST

Reference Designation	Part No.	Vendor or MIL Spec.
C1, 2	121P18691R5S2	Sprague Electric Co., North Adams, Mass.
C3	96P1059252	Sprague Electric Co., North Adams, Mass.
C4	96P1039252	Sprague Electric Co., North Adams, Mass.
CR1	1M175Z	Motorola, Phoenix, Arizona
CR2	1N457	Hughes Products, Los Angeles, Calif.
CR3 thru 5	SV905	Transitron, Wakefield, Mass.
CR7	SV910	Transitron, Wakefield, Mass.
V1	6201, 5 Star	General Electric, Owensboro, Ky.
V2	6463	General Electric, Owensboro, Ky.
K1	GHE-1C-2500D	Advance, Elgin, Ill.
K2	KRP11D	Potter and Brumfield, Princeton, Ind.
R1	RC20GF	MIL-R-11C
R2	JLU	Allen-Bradley, Milwaukee, Wisconsin
R3	RC20GF	MIL-R-11C
R4	RC20GF222J	MIL-R-11C
R5, 10, 15, 21	RC20GF102J	MIL-R-11C
R6	RLS2	Dale Products, Columbus, Nebraska
R7, 9	RLS2A	Dale Products, Columbus, Nebraska
R8	43C2-20K	Clarostat Mfg. Co., Dover, N. H.
R11	RC20GF753J	MIL-R-11C
R12	RLS10	Dale Products, Columbus, Nebraska
R13	43C2-1000	Clarostat Mfg. Co., Dover, N. H.
R14	RC20GF243J	MIL-R-11C
R16	DCMH-1/2	Dale Products, Columbus, Nebraska
R17, 20	RC20GF680J	MIL-R-11C
R18	JLU2521	Allen-Bradley Co., Milwaukee, Wisconsin
R19	RLS10	Dale Products, Columbus, Nebraska
R22	RC20GF103J	MIL-R-11C

Arizona


COMPARISON AMPLIFIER
POSITIVE PEAK LIMITER
DC BALANCE #3
+300
DC VIDEO (RECORD) FROM NOISE FILTER AMPLIFIER OR
J13
OPTIONAL CLAMP
J14
DC VIDEO (REPRODUCE) FROM DATRAC
TP 9
R1 68K
R2 25K 2W
R3 22K
R4 2.2K
R5 30K 3W WW 3%
R6 20K 2W WW 3%
R7 20K 2W WW 3%
R8 20K 2W WW
R9 20K 2W WW 3%
R10 1K
R11 7.5K
R12 20K WW 3%
R13 1K 2W WW
R14 24K
R15 300K 1%
C1
C2
C3 .1 uf 250 WVDC
C4 .01 uf 200 WVDC
CR1
CR2
V1A
V1B
V1 6201
ATTENUATOR
K1
K2
+200
0 VDC
2ND LOW-PASS FILTER
FEEDBACK VOLTAGE TO DC AMPLIFIER
J15
FEEDBACK VOLTAGE FROM REFERENCE AMPLIFIER
TP 10
J16
-150
6.3
POWER
J18
V1
V2

B

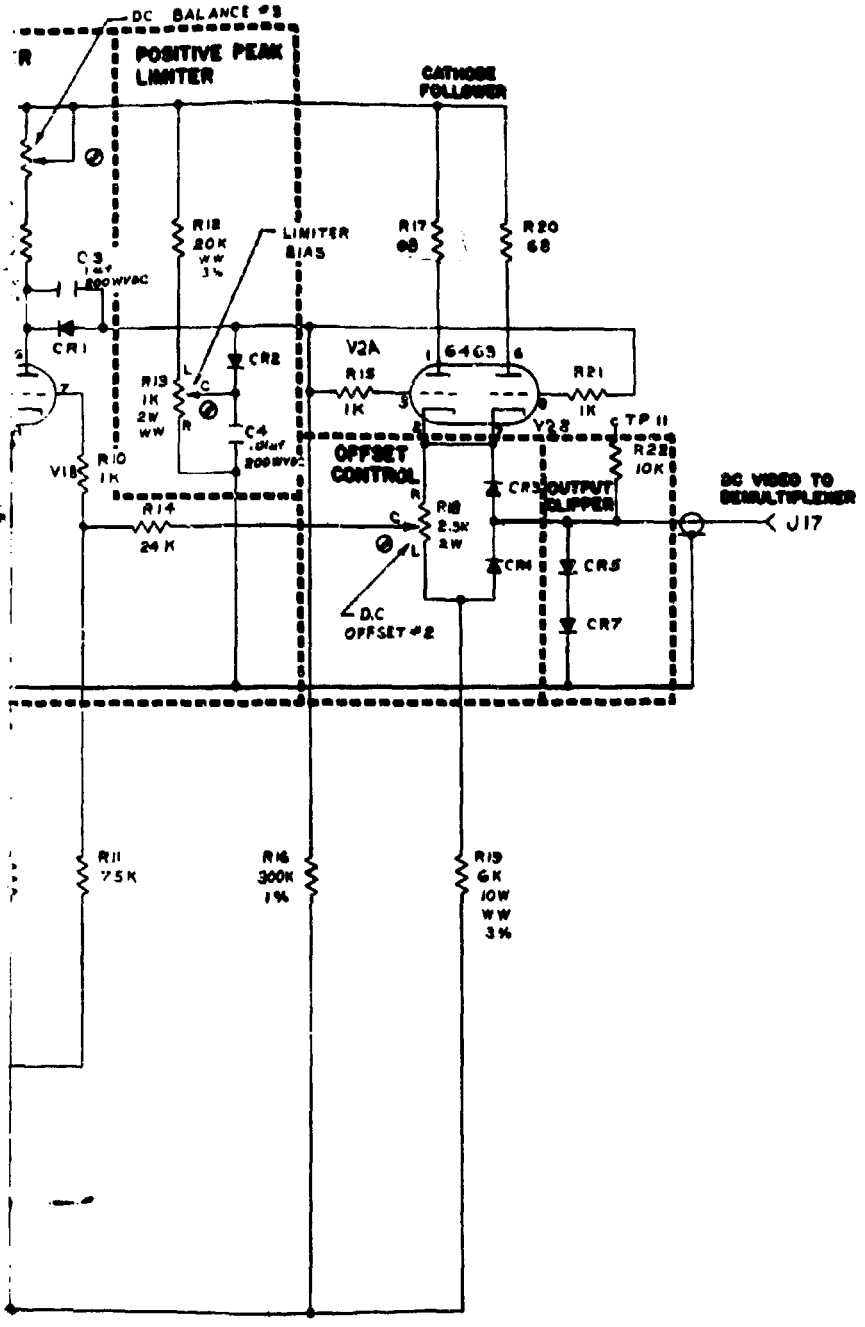
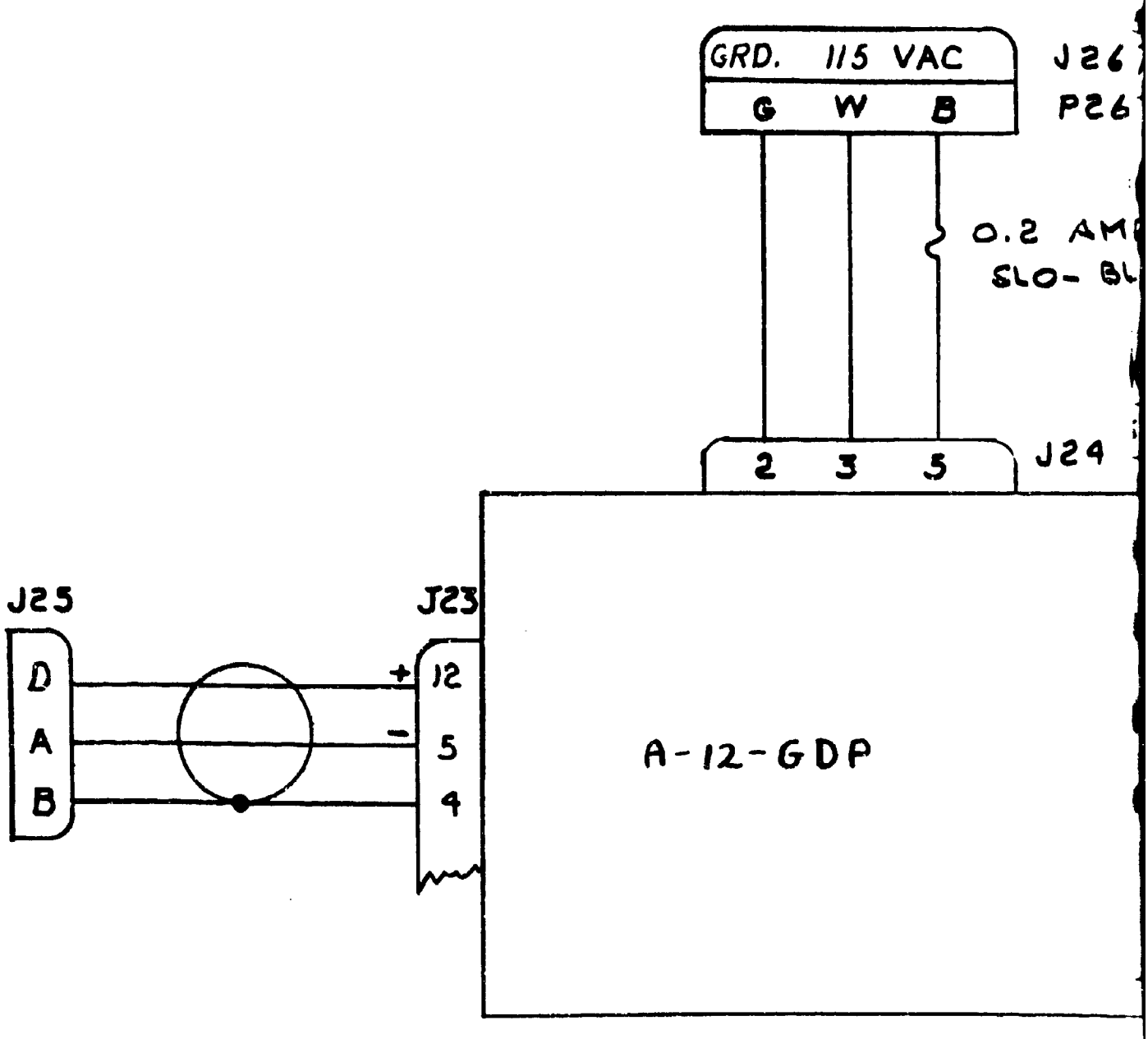


Fig. A-6 Gate Driver Amplifier


GRD. 115 VAC
J26
G W B
P26
0.2 AM
SLO- BL
2 3 5
J24
J25
J23
D
A
B
+ 12
- 5
4
A-12-GDP

A

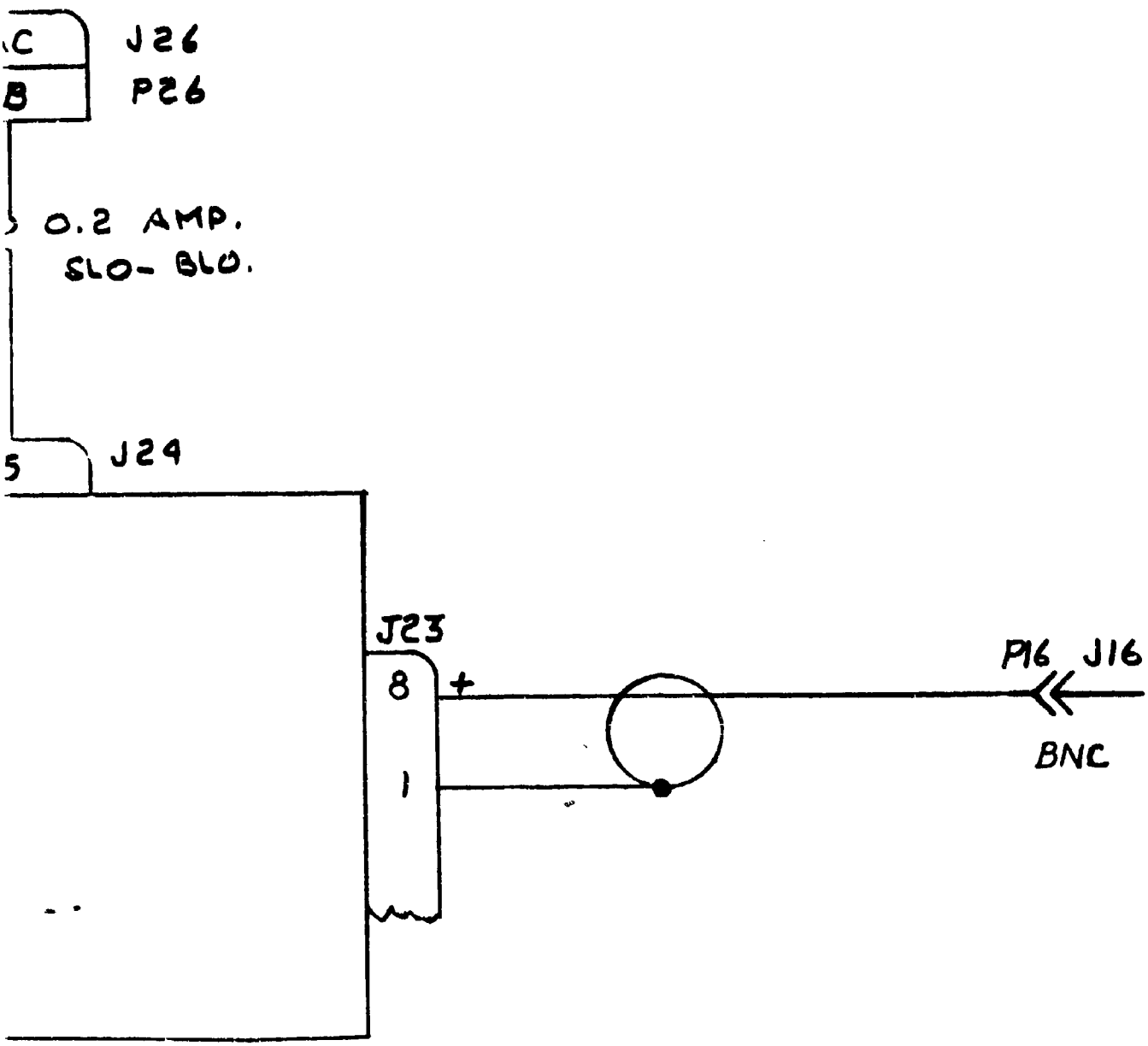
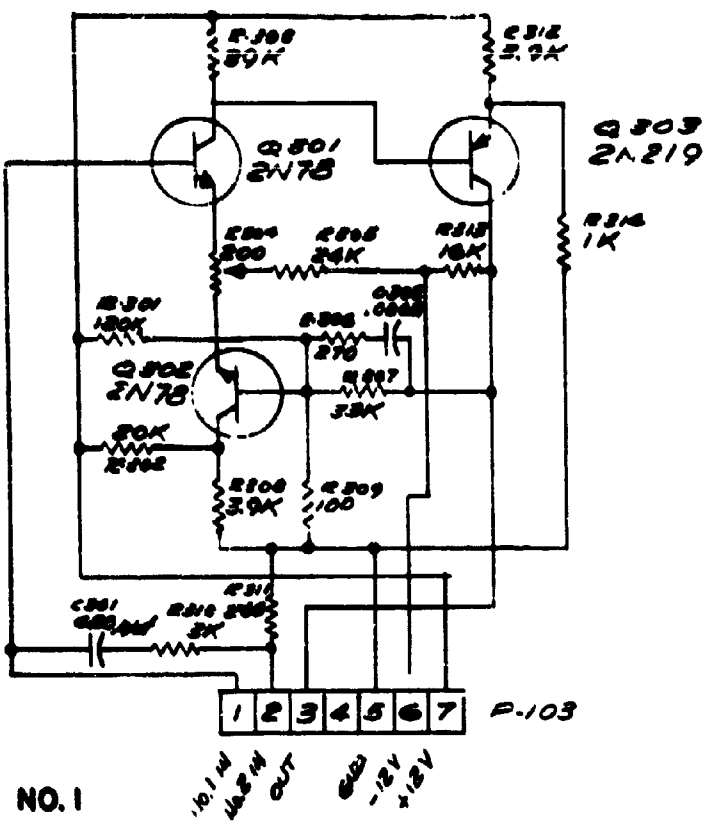
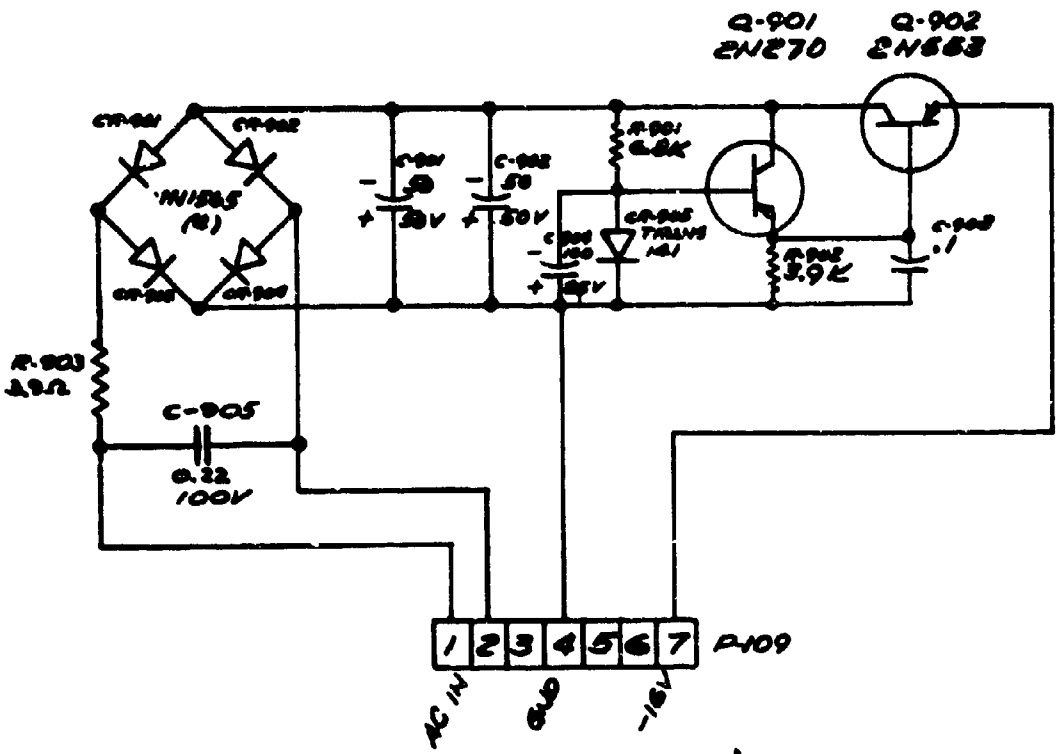


Fig. A-7 Reference Amplifier (Sheet 1 of 3)

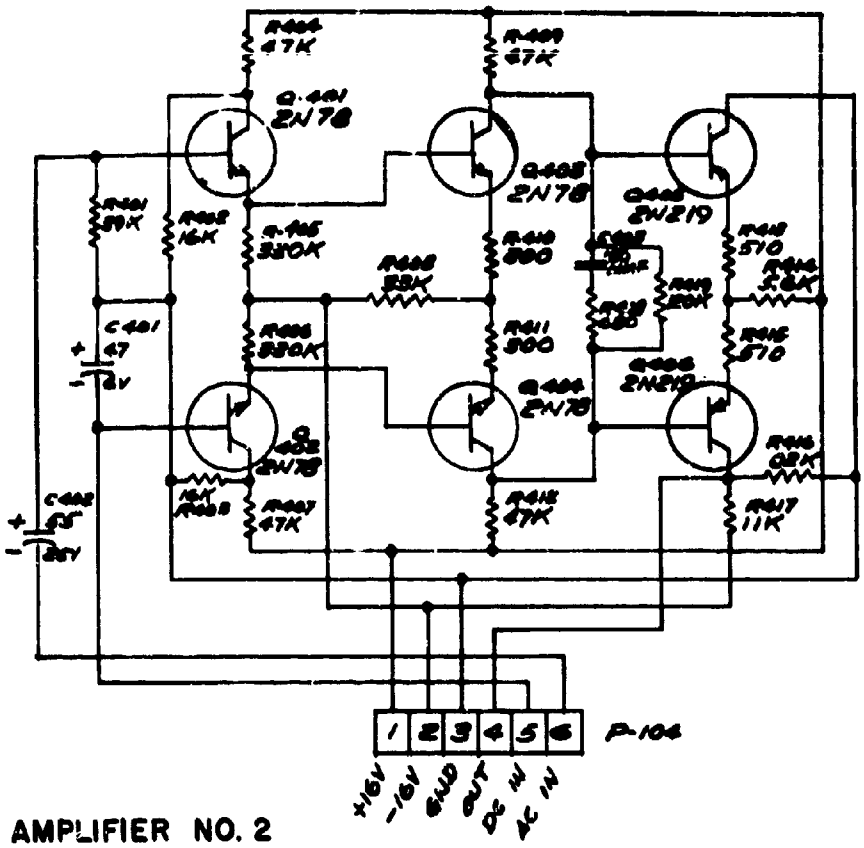


AMPLIFIER NO. 1

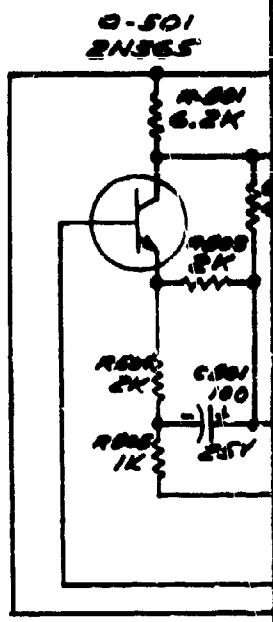


-16-VOLT REGULATOR

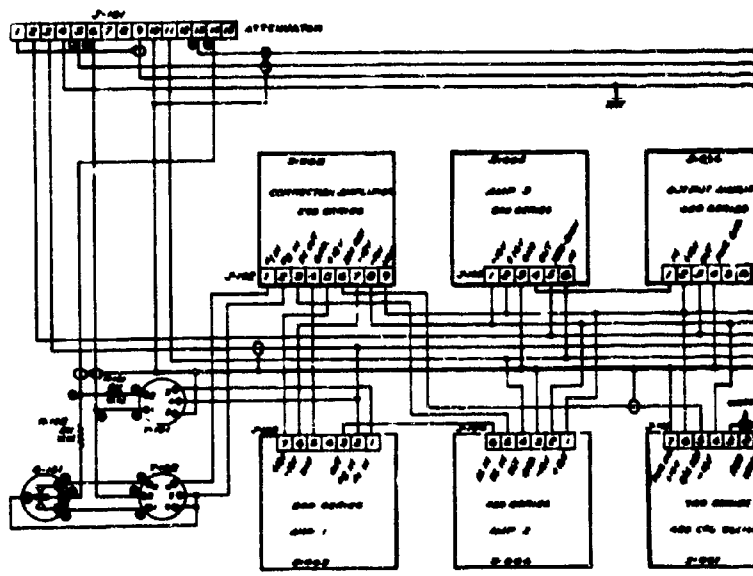
A



AMPLIFIER NO. 2



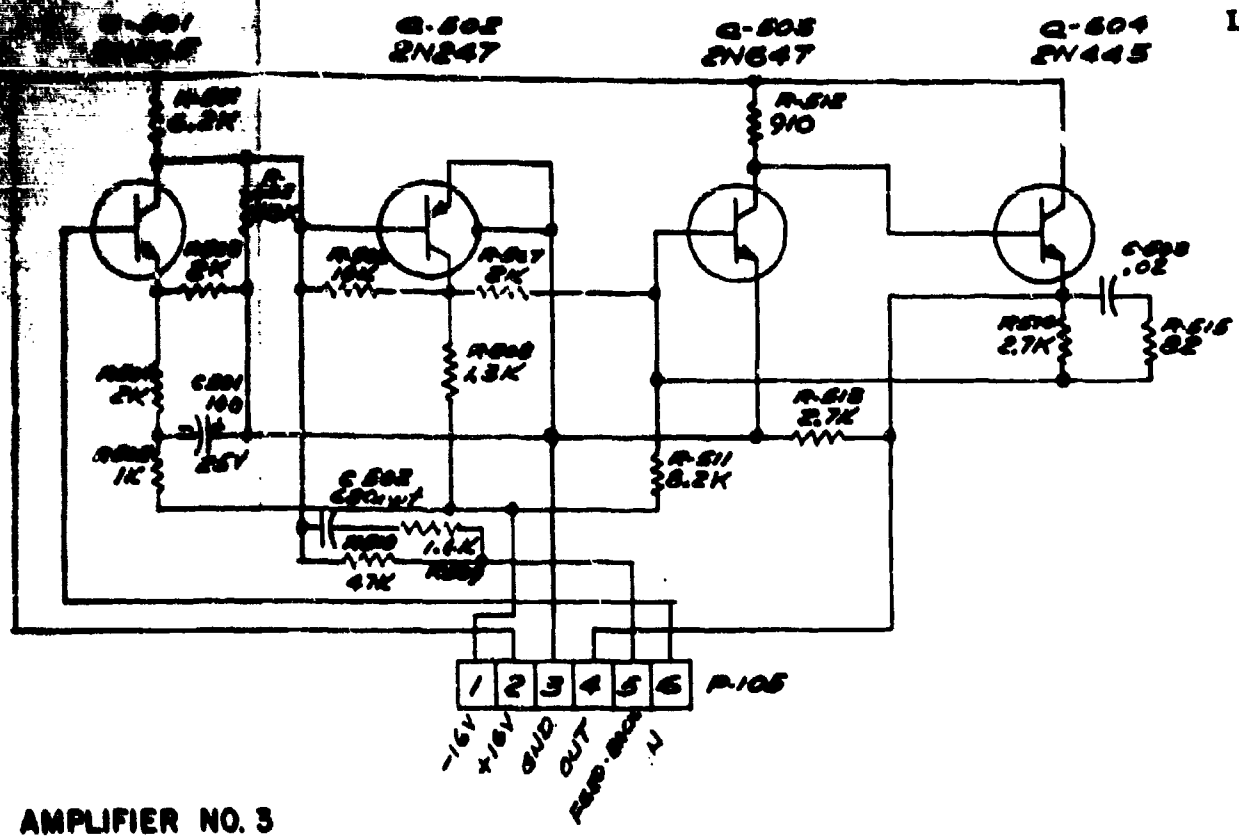
AMPLIFIER NO. 3



NOTES

B

WIRING BLOCK DIAGRAM



AMPLIFIER NO. 3

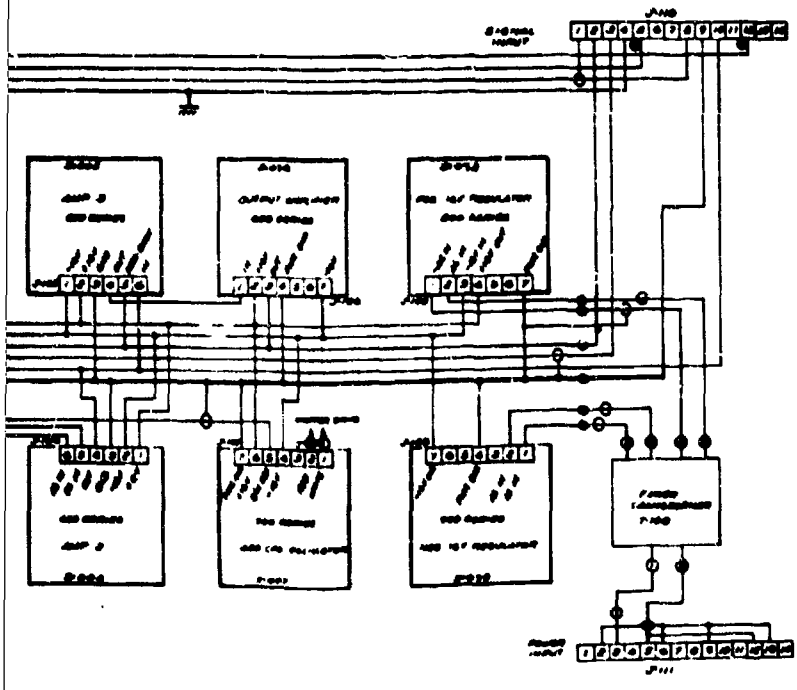
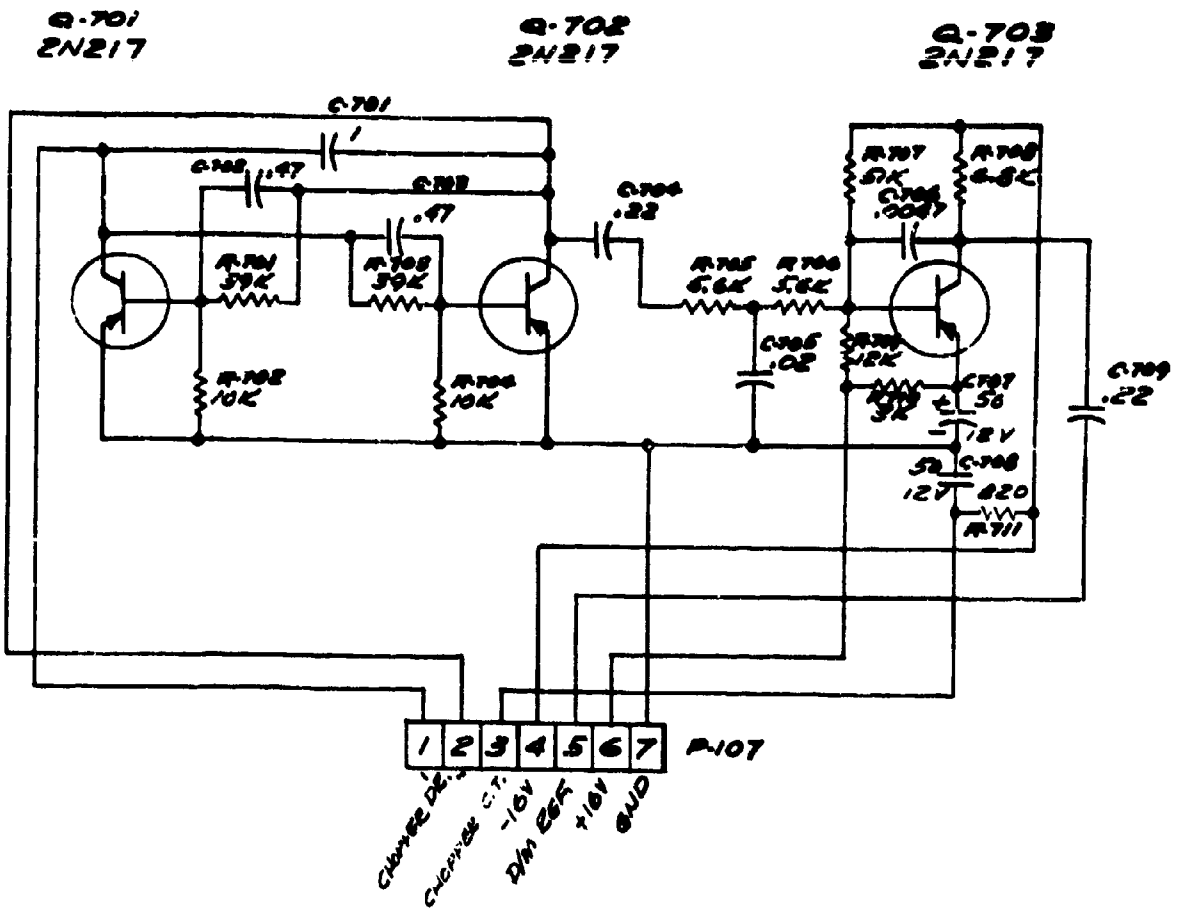
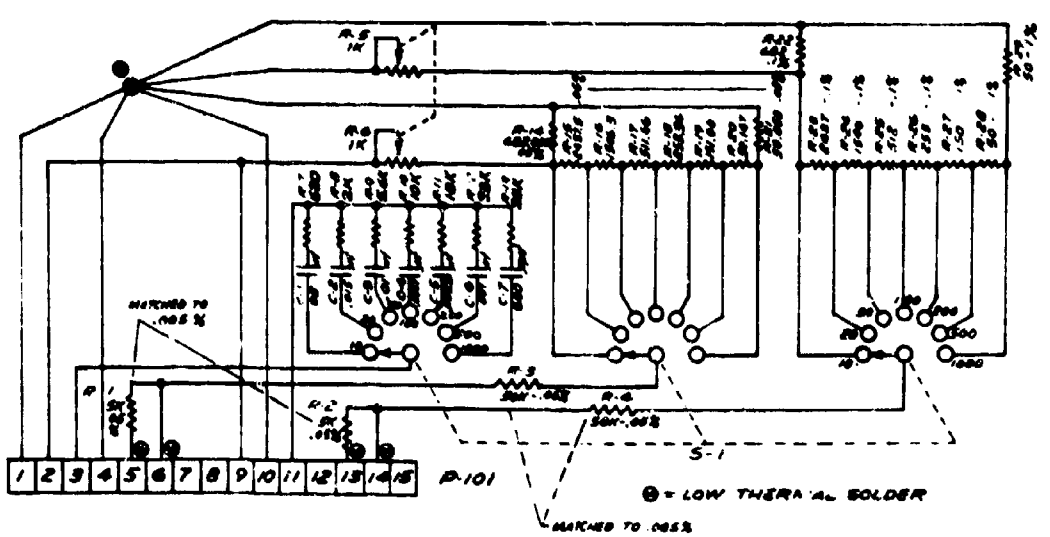


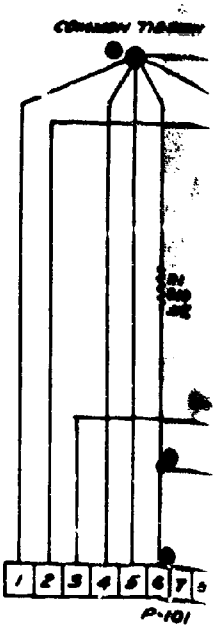
Fig. A-7 Reference Amplifier (Sheet 2 of 3)



450-CYCLE OSCILLATOR

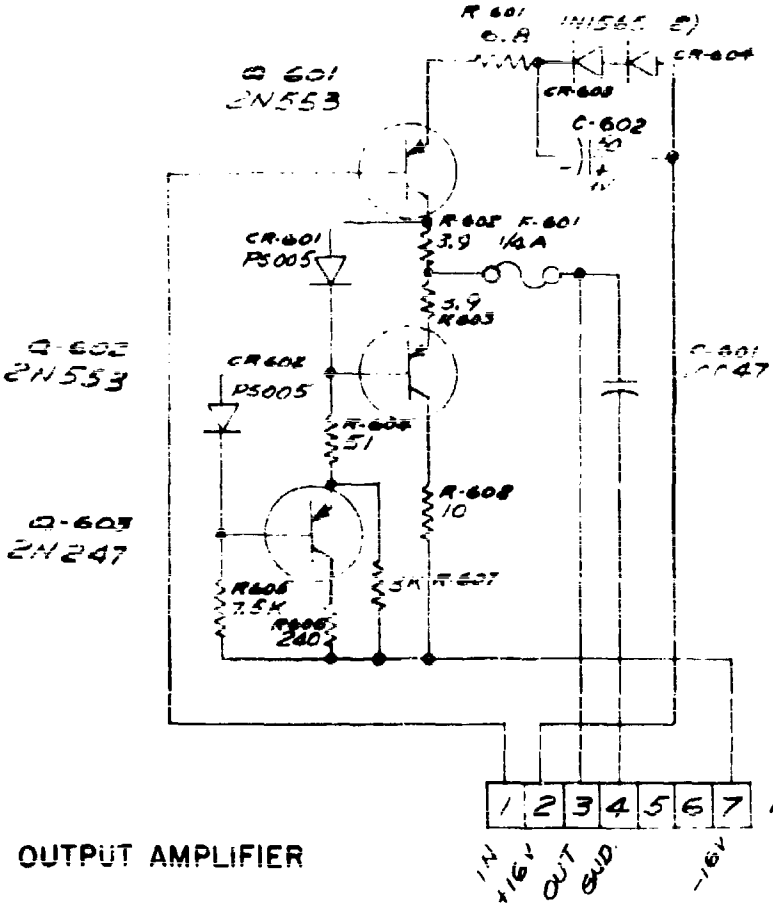


ATTENUATOR

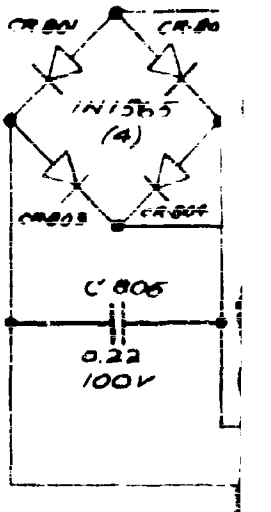


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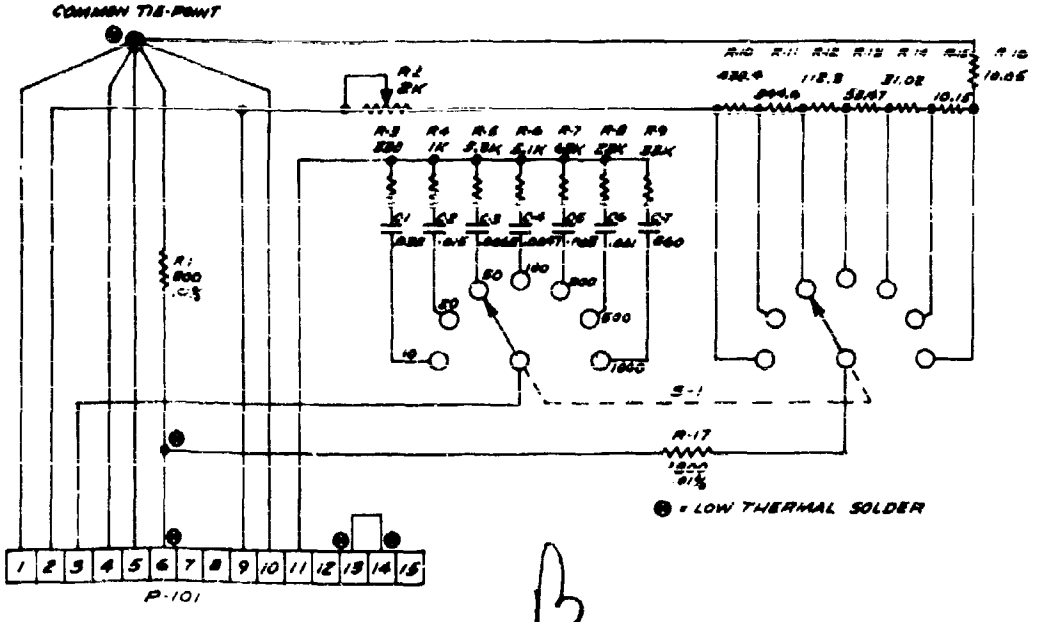
A



OUTPUT AMPLIFIER

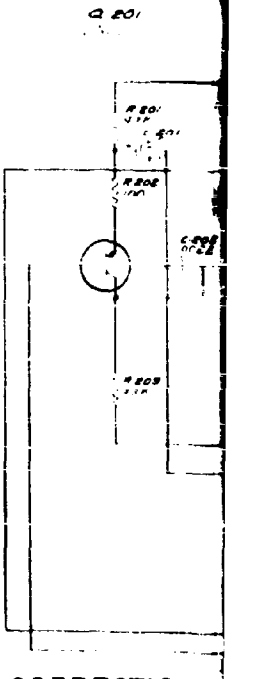


+16-VOLT REG

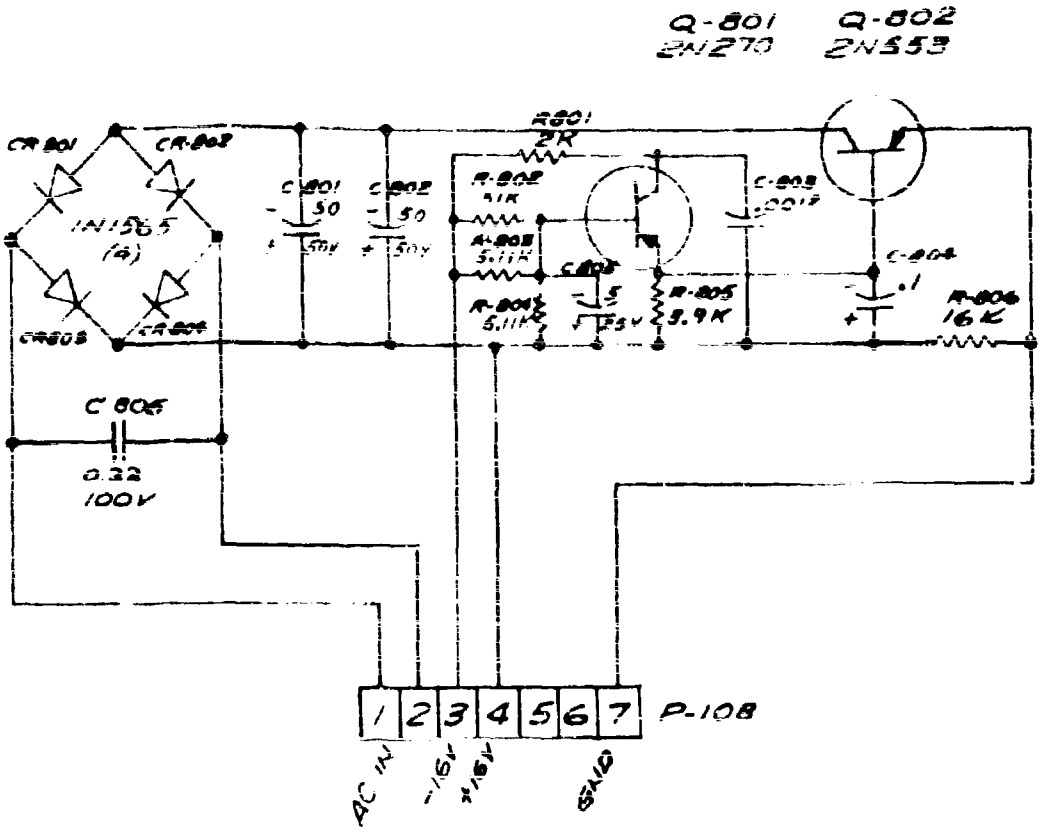


ATTENUATOR

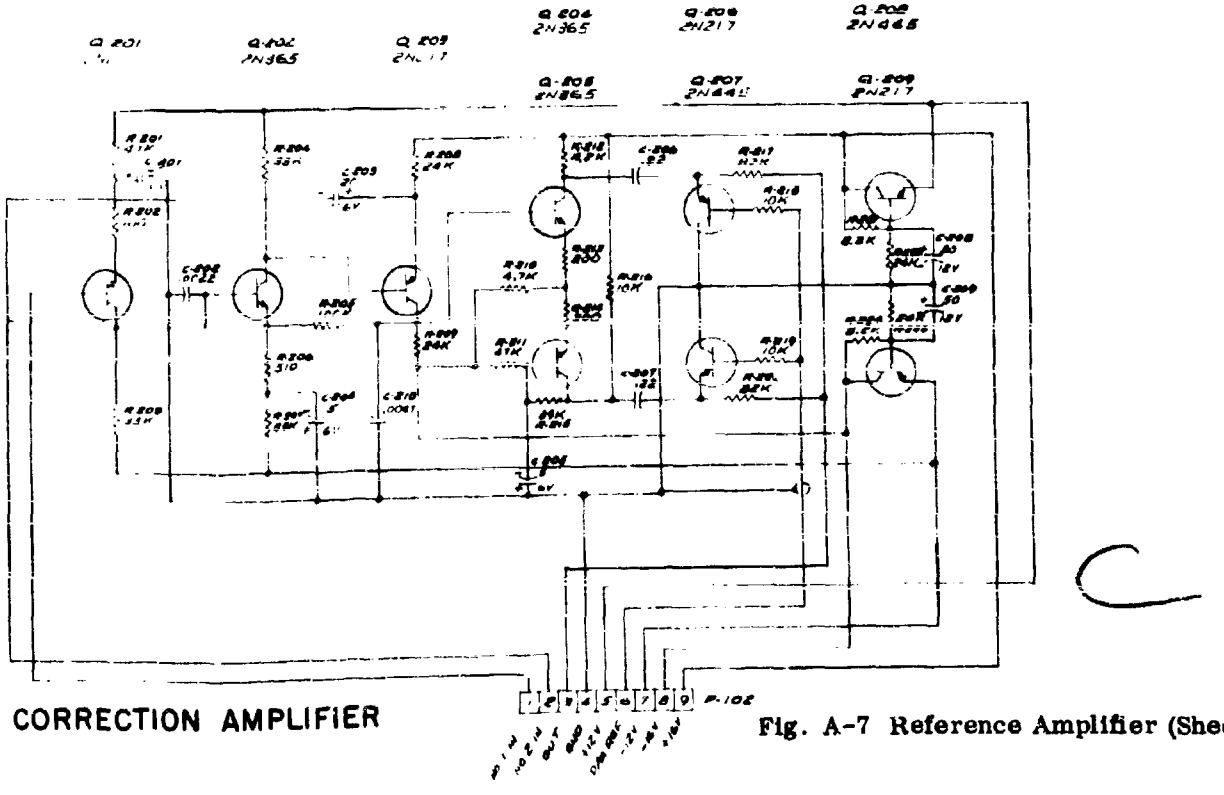
A-12 CSP



CORRECTION

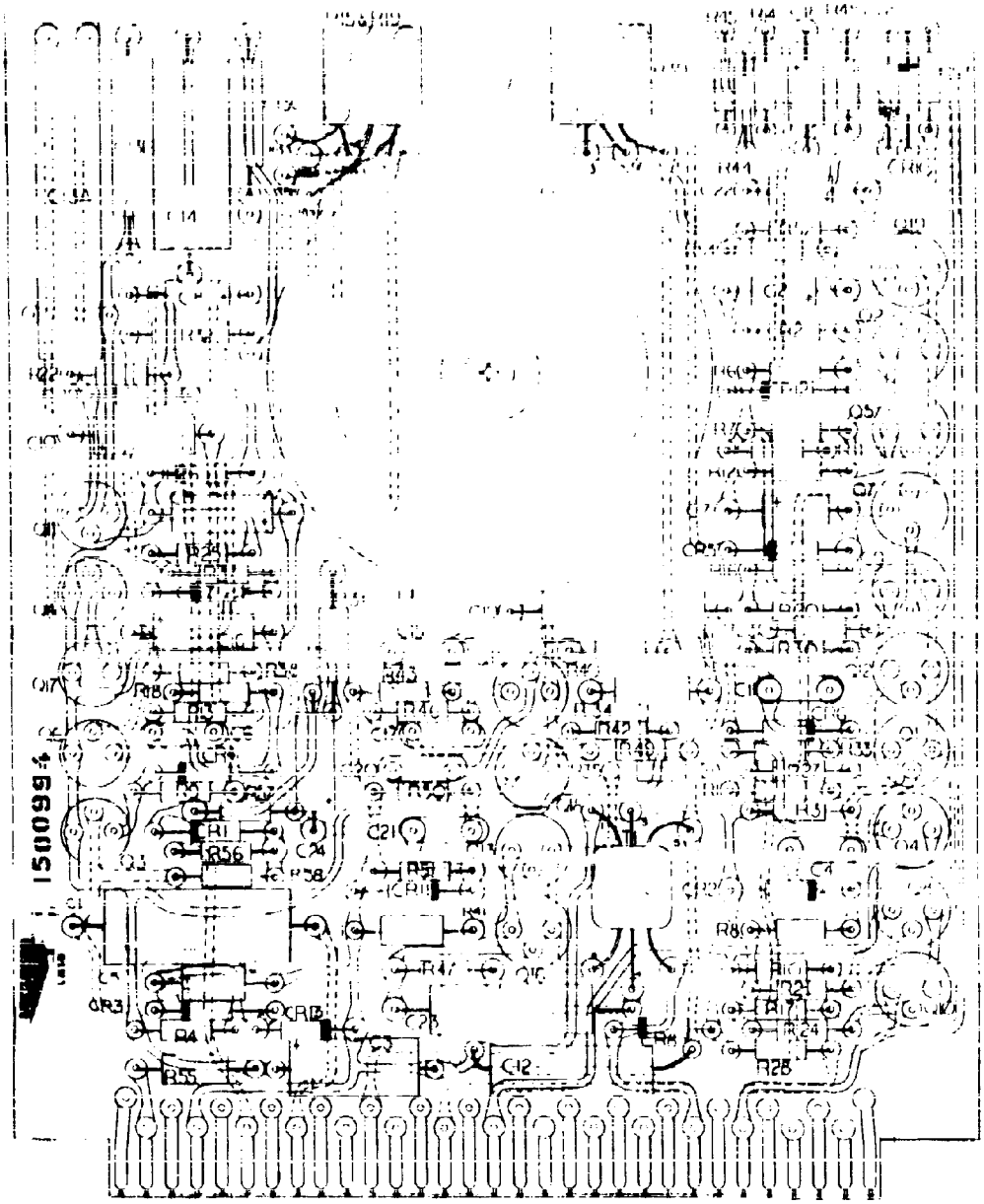


+16-VOLT REGULATOR



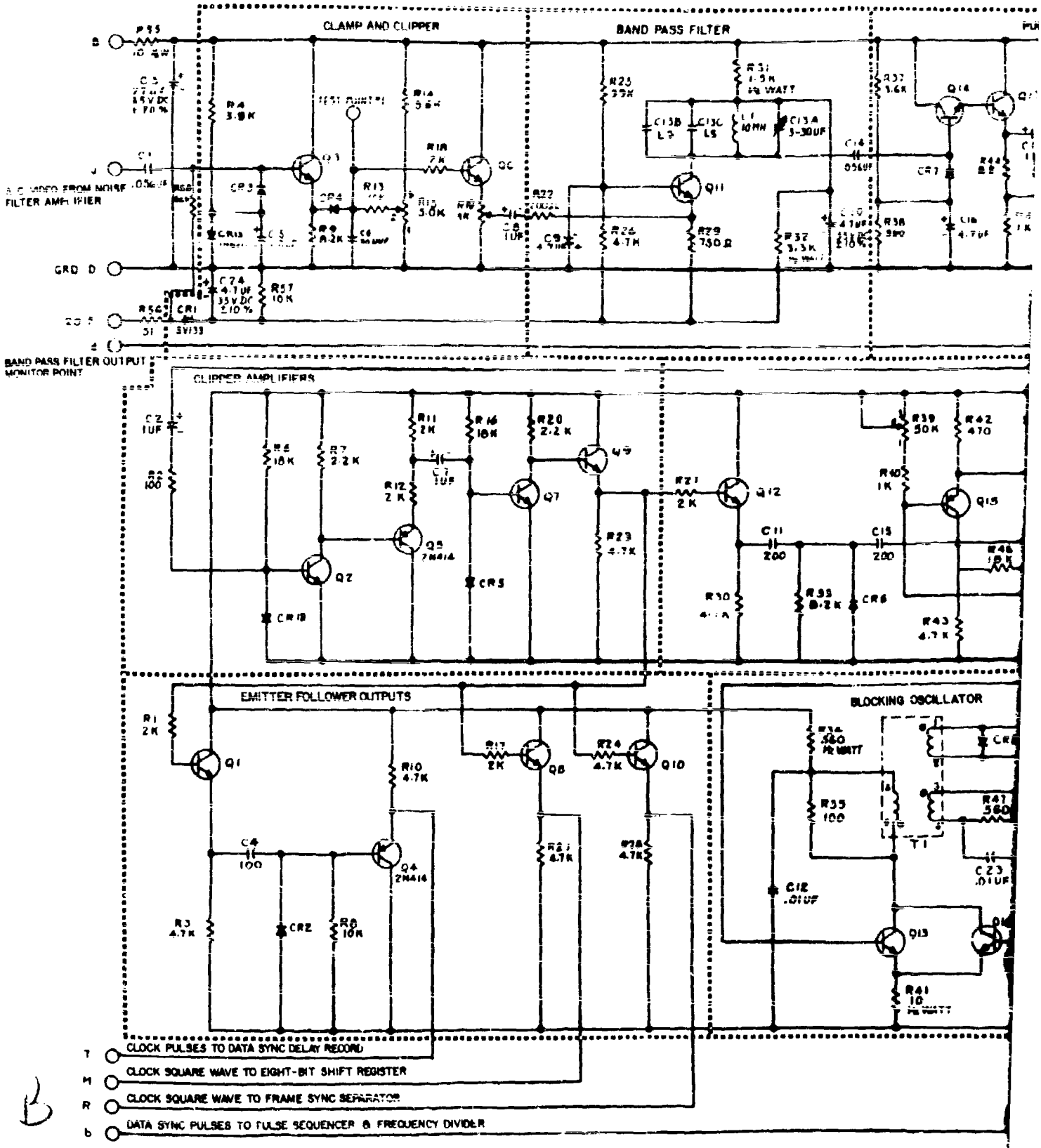
CORRECTION AMPLIFIER

Fig. A-7 Reference Amplifier (Sheet 3 of 3)



PARTS LIST

Reference Designation	Part No.	Vendor or Mfr. Name


CLAMP AND CLIPPER
BAND PASS FILTER
A.C. VIDEO FROM NOISE FILTER AMPLIFIER
GRD D
BAND PASS FILTER OUTPUT MONITOR POINT
CLIPPER AMPLIFIERS
EMITTER FOLLOWER OUTPUTS
BLOCKING OSCILLATOR
T CLOCK PULSES TO DATA SYNC DELAY RECORD
M CLOCK SQUARE WAVE TO EIGHT-BIT SHIFT REGISTER
R CLOCK SQUARE WAVE TO FRAME SYNC SEPARATOR
b DATA SYNC PULSES TO PULSE SEQUENCER & FREQUENCY DIVIDER

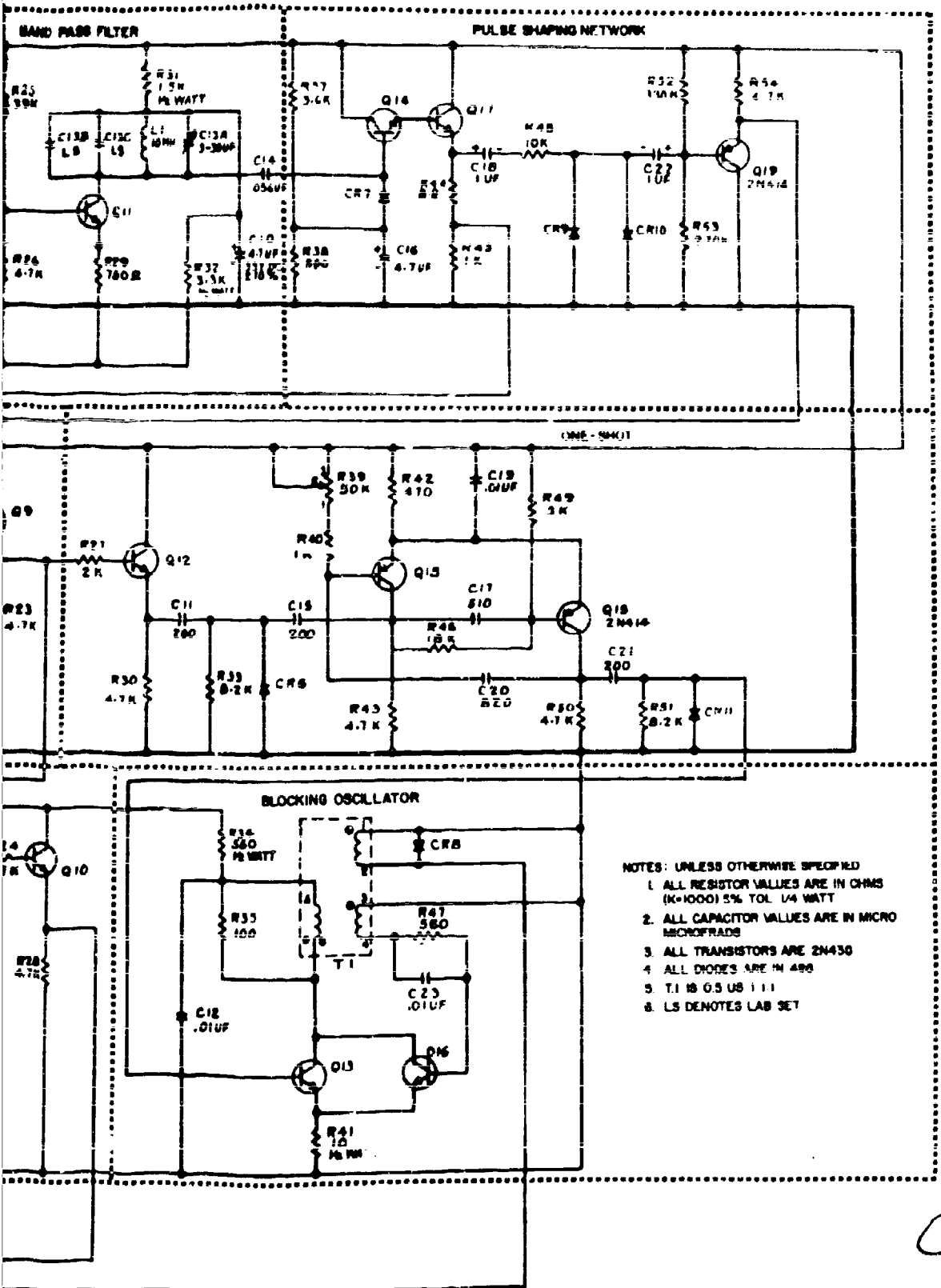
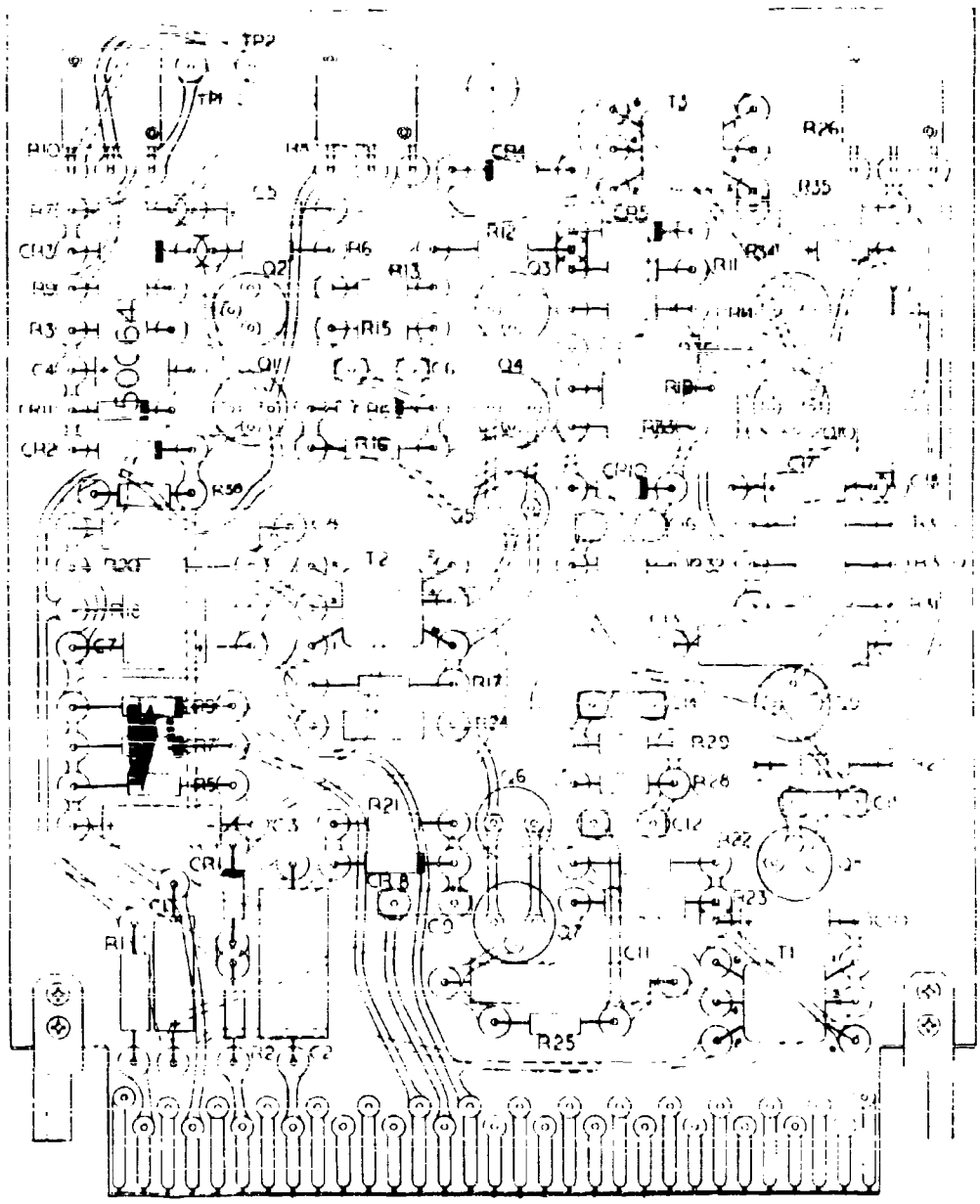


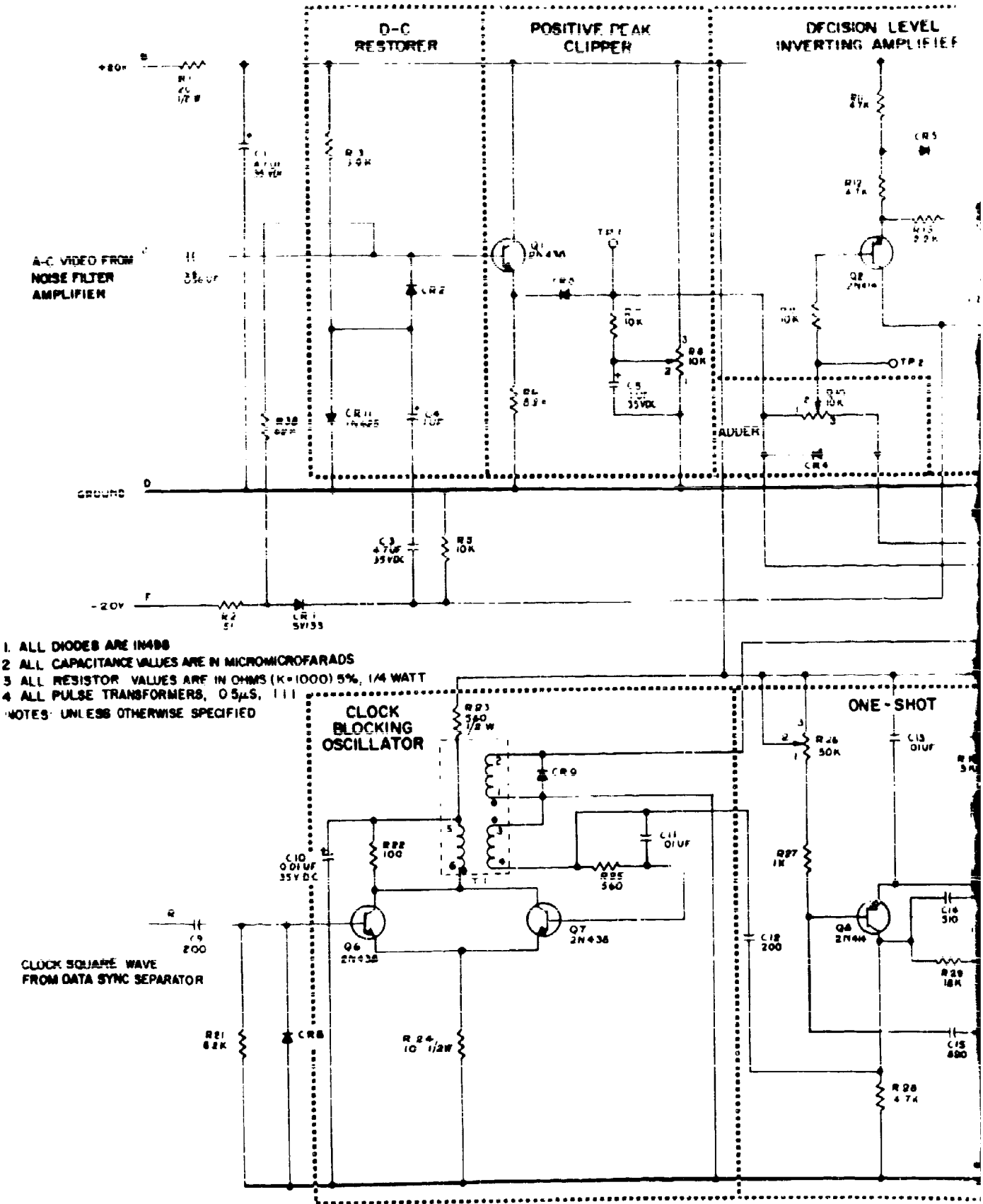
Fig. A-8 Data Sync Separator, Vibration



PARTS LIST

Reference Designation	Part No.	Vendor or Mfg. Desig.
C1, 9		
C2, 3		
C4, 5, 12, 13		
C7, 10, 11		
C8, 11, 12, 14		
C15		
C16		
C17 thru 19		
C20, 21		
C22, 4 thru 7, 10, 11		
C23, 8, 9, 0		
R1, 10		
R2, 3		
R4, 7, 8		
R5, 14, 20, 34		
R6, 16		
R11, 18, 30, 33		
R12, 15		
R13, 17, 28		
R19, 22		
R21, 23, 24, 25, 26, 27, 29, 31, 32, 35		
T1, 2, 3		

A


D-C RESTORER
POSITIVE PEAK CLIPPER
DECISION LEVEL INVERTING AMPLIFIER
A-C VIDEO FROM NOISE FILTER AMPLIFIER
GROUND
-20V
ADDER
CLOCK BLOCKING OSCILLATOR
ONE-SHOT
CLOCK SQUARE WAVE FROM DATA SYNC SEPARATOR
1. ALL DIODES ARE IN498
2 ALL CAPACITANCE VALUES ARE IN MICROMICROFARADS
3 ALL RESISTOR VALUES ARE IN OHMS (K=1000) 5%, 1/4 WATT
4 ALL PULSE TRANSFORMERS, 0.5μS, 1:1
NOTES: UNLESS OTHERWISE SPECIFIED

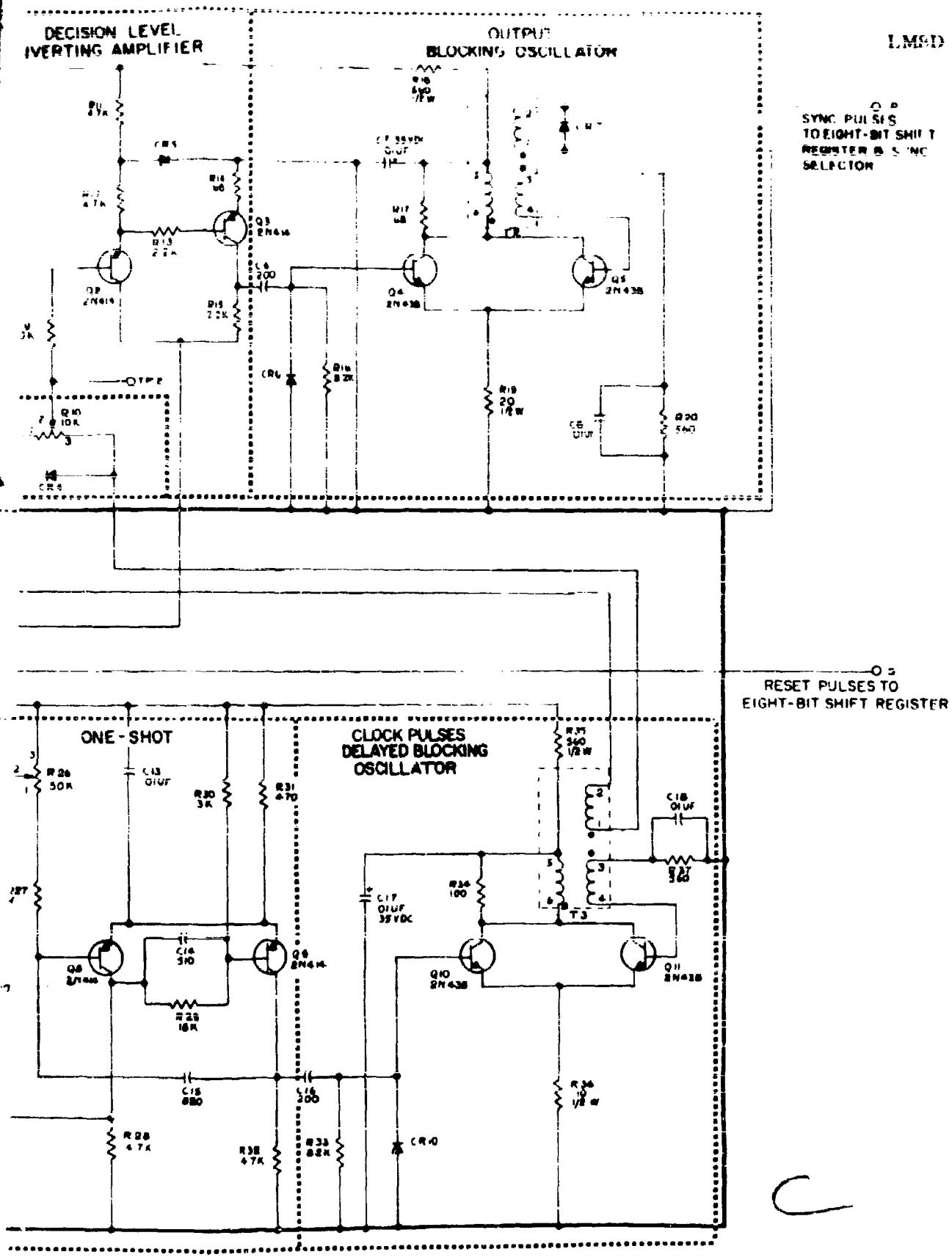
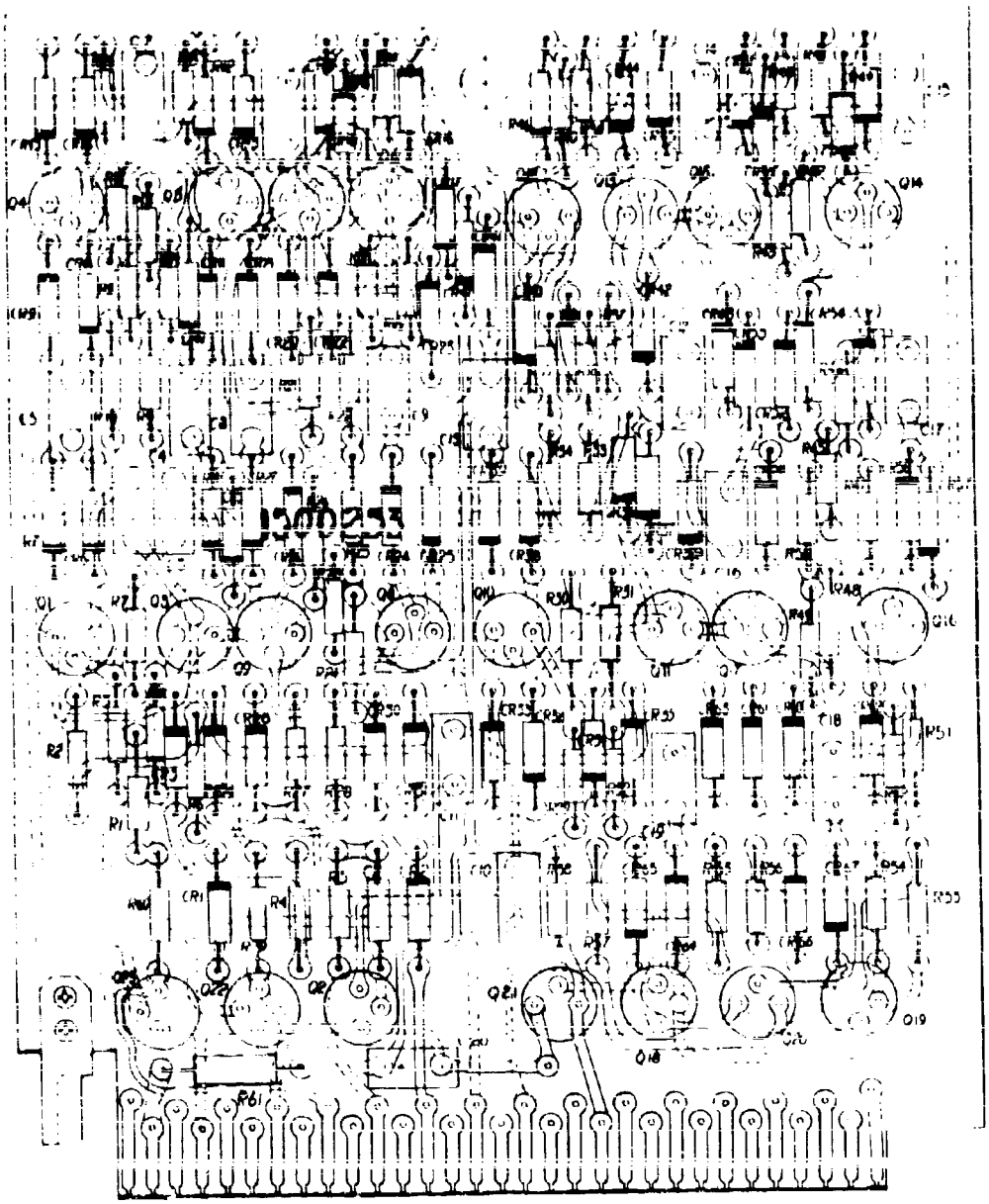
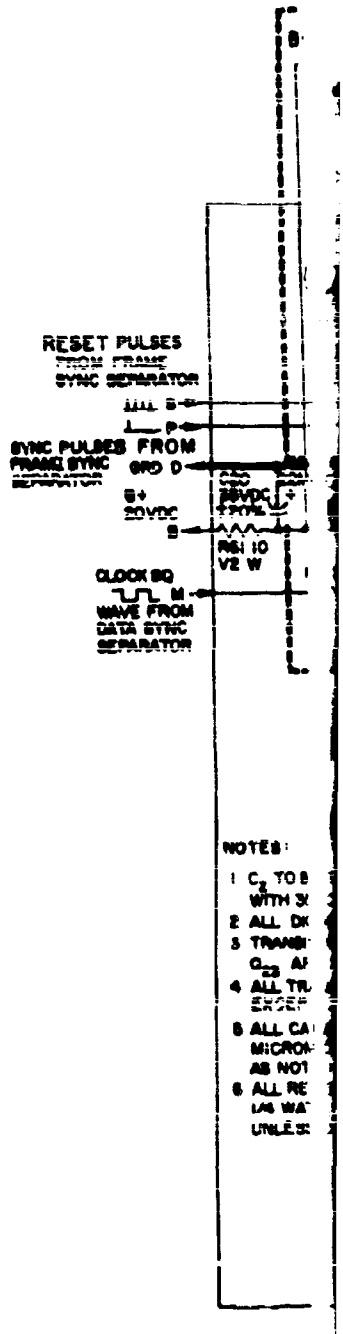


Fig. A-9 Frame Sync Separator, Vibration



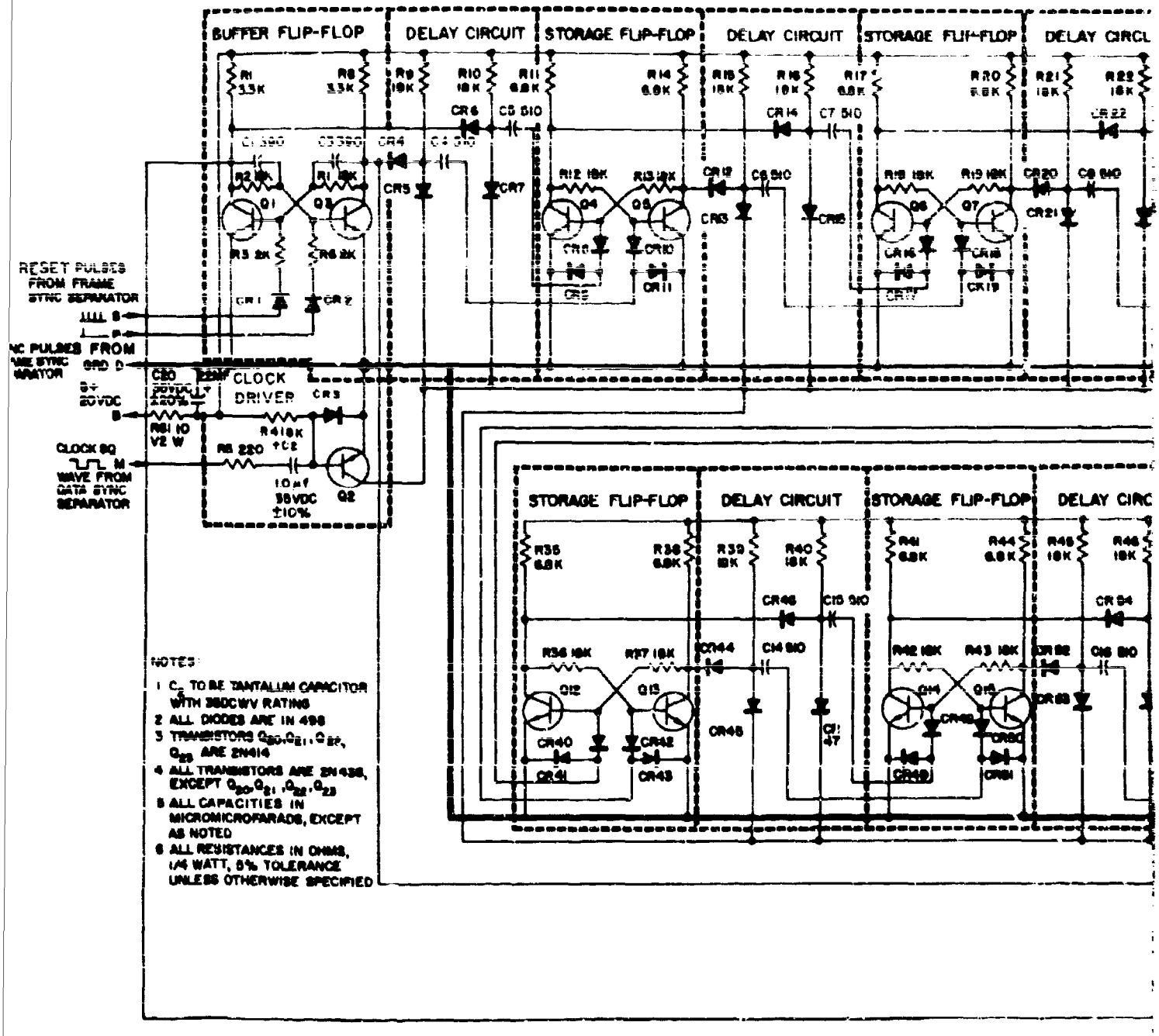


PARTS LIST

Reference Designation	Part No.	Vendor or MIL Spec
C1-3		
C4		
C5 thru 10		
C11		
C12 thru 17		
Q20 thru 23		
R1-6		
R8-9-10-11-12-13		
26-27-28-29-30-31		
32-33-34-35-39-40		
42-43-44-46-48-49		
R3-4		
R7		
R11-14-17-20-23-26		
29-32-35-36-41-44		
47-50-53-54		
R61		

NOTES:

1. C_2 TO B
WITH 3
2. ALL DI
3. TRANSI
Q_{23} A
4. ALL TR
EXCEP
5. ALL CA
MICRON
AS NOT
6. ALL RE
LAS WA
UNLESS


BUFFER FLIP-FLOP
DELAY CIRCUIT
STORAGE FLIP-FLOP
DELAY CIRCUIT
STORAGE FLIP-FLOP
DELAY CIRCUIT
STORAGE FLIP-FLOP
DELAY CIRCUIT
CLOCK DRIVER
RESET PULSES FROM FRAME SYNC SEPARATOR
FROM
CLOCK SQ WAVE FROM DATA SYNC SEPARATOR
NOTES:
1 C5 TO BE TANTALUM CAPACITOR WITH 350C WV RATING
2 ALL DIODES ARE IN 498
3 TRANSISTORS Q20, Q21, Q22, Q23 ARE 2N414
4 ALL TRANSISTORS ARE 2N438, EXCEPT Q20, Q21, Q22, Q23
5 ALL CAPACITIES IN MICROMICROFARADS, EXCEPT AS NOTED
6 ALL RESISTANCES IN OHMS, 1/4 WATT, 5% TOLERANCE UNLESS OTHERWISE SPECIFIED

B

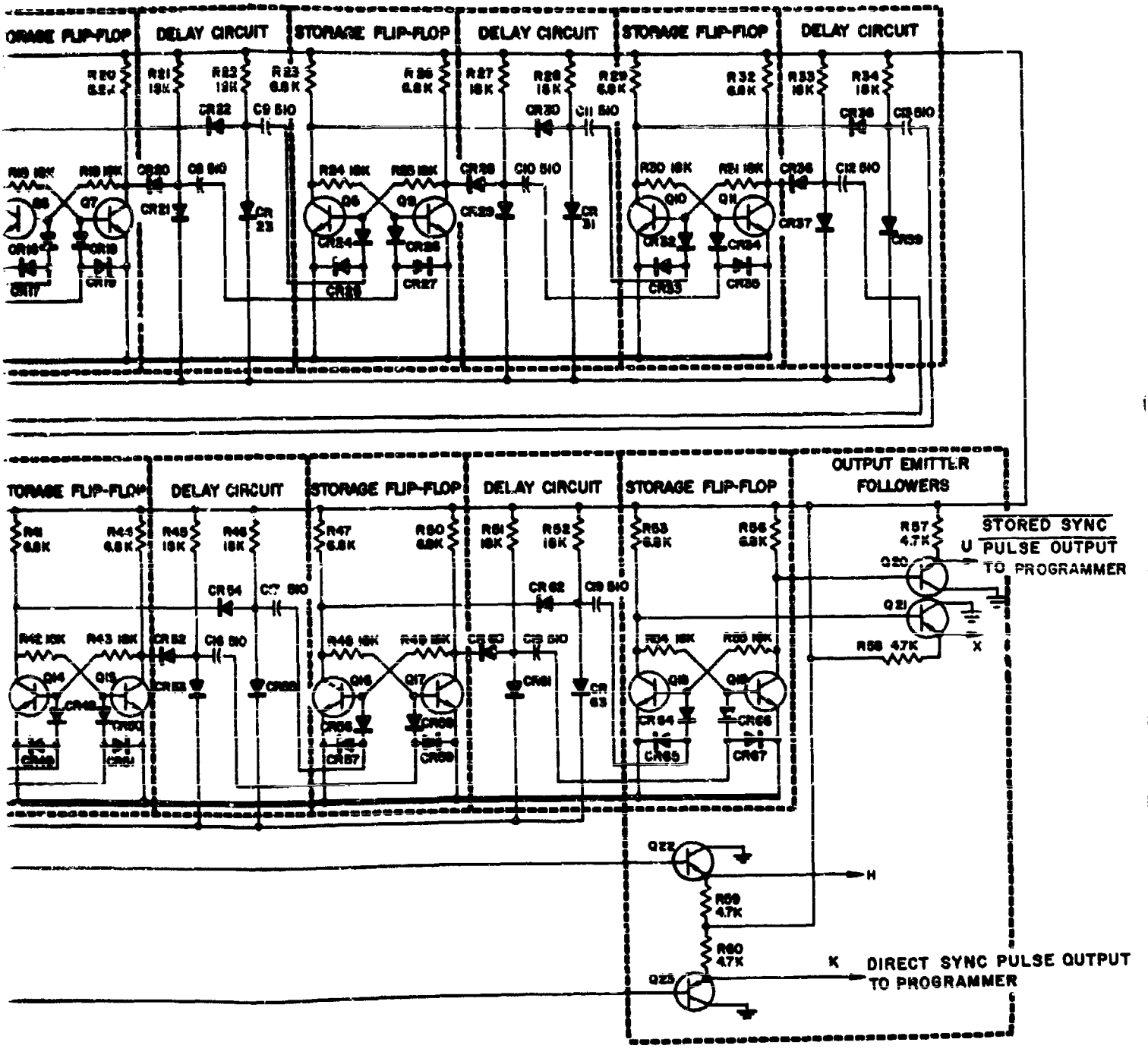
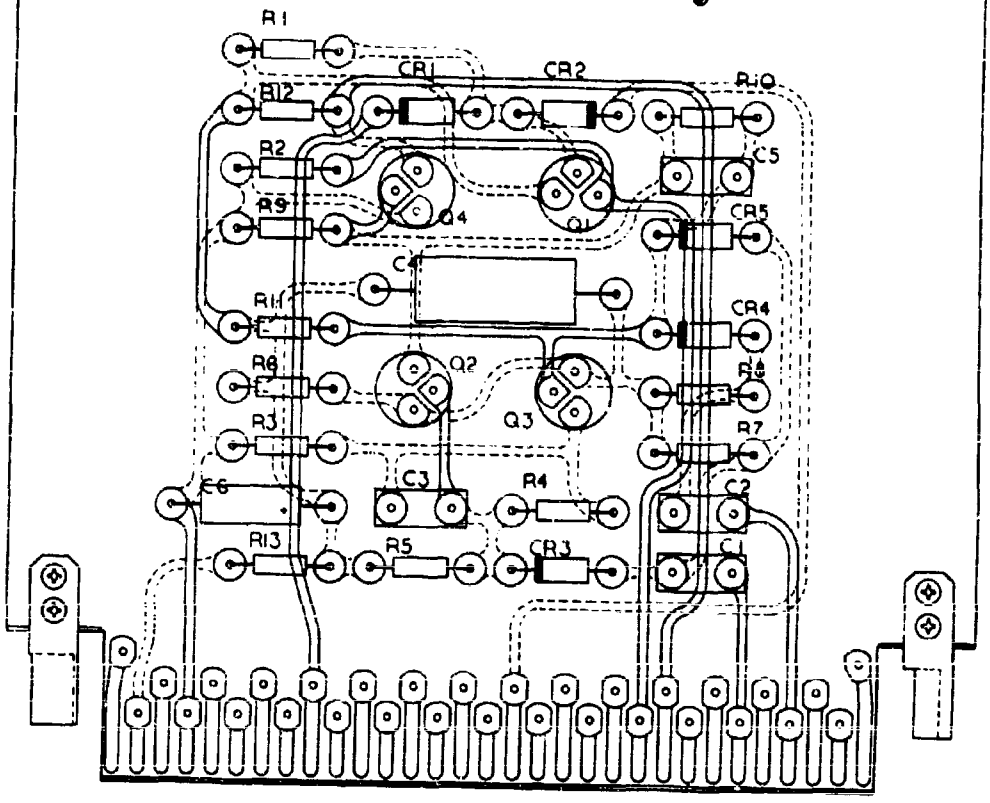


Fig. A-10 Eight-Bit Shift Register, Vibration

1500775

LOCKHEED

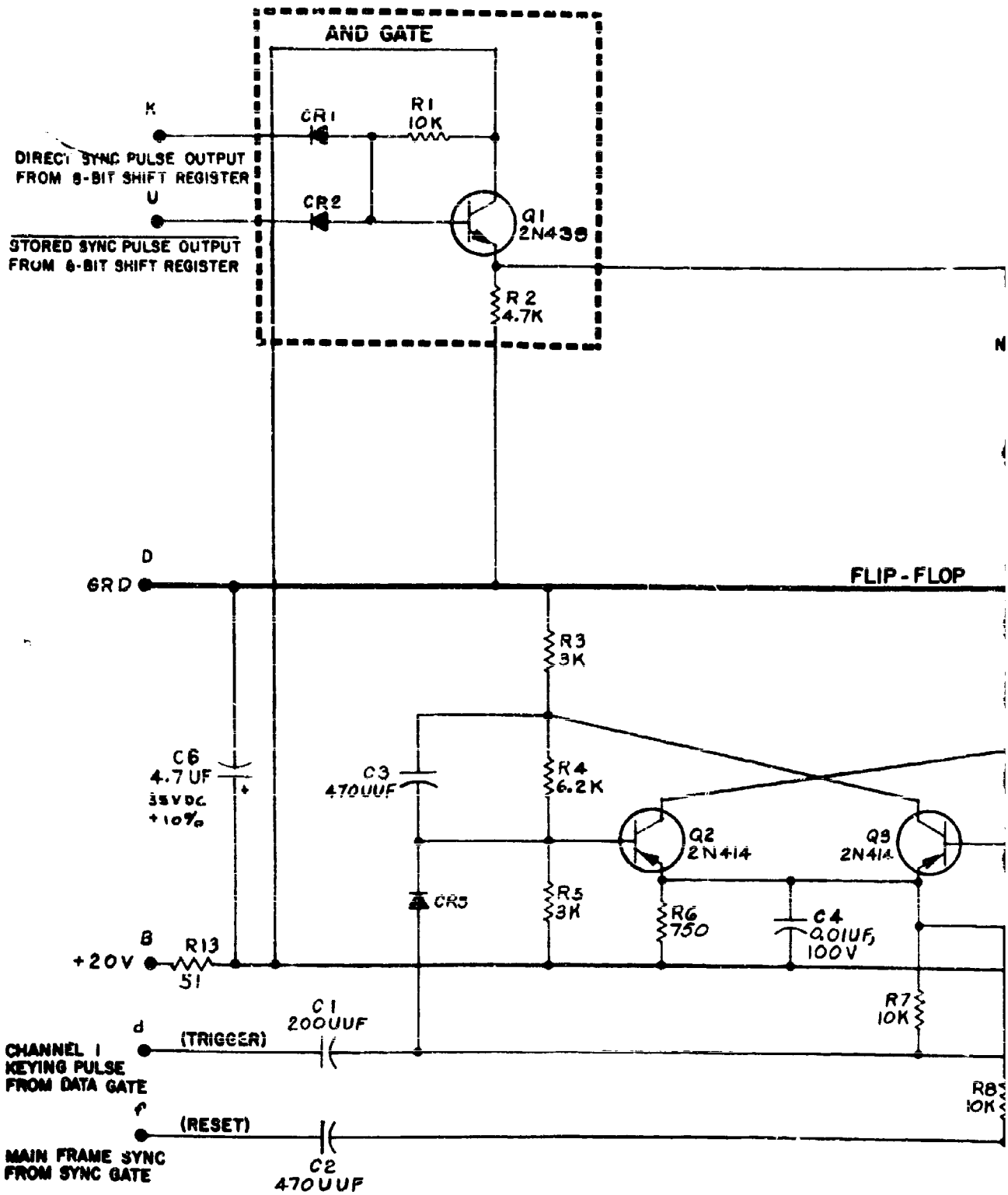
LMSD



PARTS LIST

Reference Designation	Part No.	Vendor or Mfg. Spec.
C1	D6R1BP051J	El Menco, Los Angeles, Calif.
C2, 3, 5	D6R1BP471J	El Menco, Los Angeles, Calif.
C4	56P10S5S1S4	Sprague Electric Co., North Adams, Mass.
C6	1S6D475X9035B2	Sprague Electric Co., North Adams, Mass.
CR1 thru 5	1N888	Texas Inst., Dallas, Texas
Q1	2N488	CBM-Hytron, Danvers, Mass.
Q2 thru 4	2N414	Raytheon Mfg.Co., Newton, Mass.
R1, 7, 8	RC07GF106J	MIL-R-11
R2, 12	RC07GF474J	MIL-R-11
R3, 4, 9, 11	RC07GF306J	MIL-R-11
R5, 10	RC07GF825J	MIL-R-11
R6	RC07GF751J	MIL-R-11
R13	RC07GF510J	MIL-R-11

A


AND GATE
K
CR1
R1
10K
DIRECT SYNC PULSE OUTPUT
FROM 8-BIT SHIFT REGISTER
U
CR2
Q1
2N438
STORED SYNC PULSE OUTPUT
FROM 8-BIT SHIFT REGISTER
R2
4.7K
N
D
GRD
FLIP-FLOP
R3
3K
C6
4.7 UF
35 V DC
+10%
C3
470UUF
R4
6.2K
Q2
2N414
Q3
2N414
CR3
R5
3K
R6
750
C4
.01UF,
100V
B
+20V
R13
51
R7
10K
C1
200UUF
d
(TRIGGER)
CHANNEL 1
KEYING PULSE
FROM DATA GATE
R8
10K
f
(RESET)
MAIN FRAME SYNC
FROM SYNC GATE
C2
470UUF

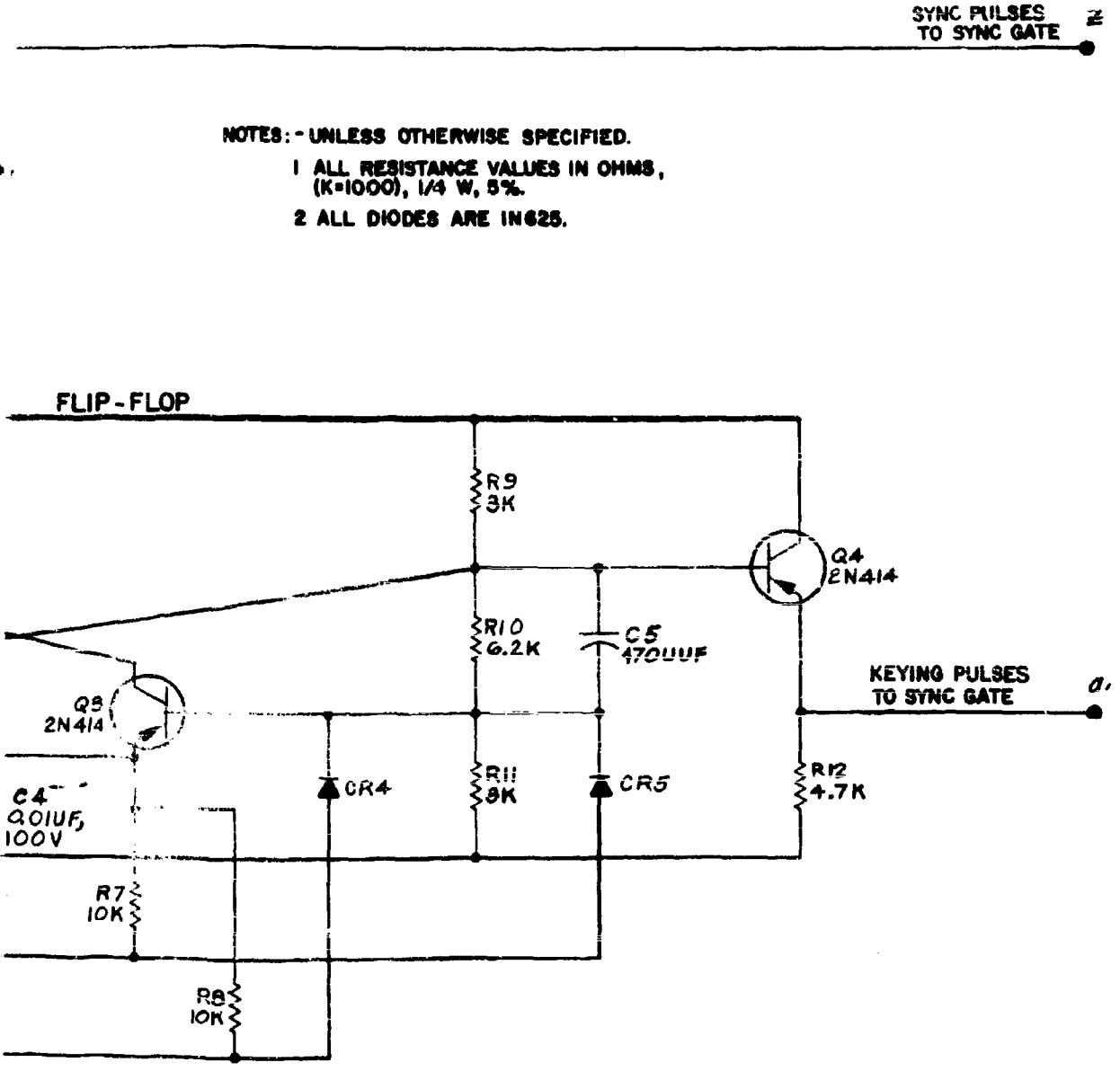
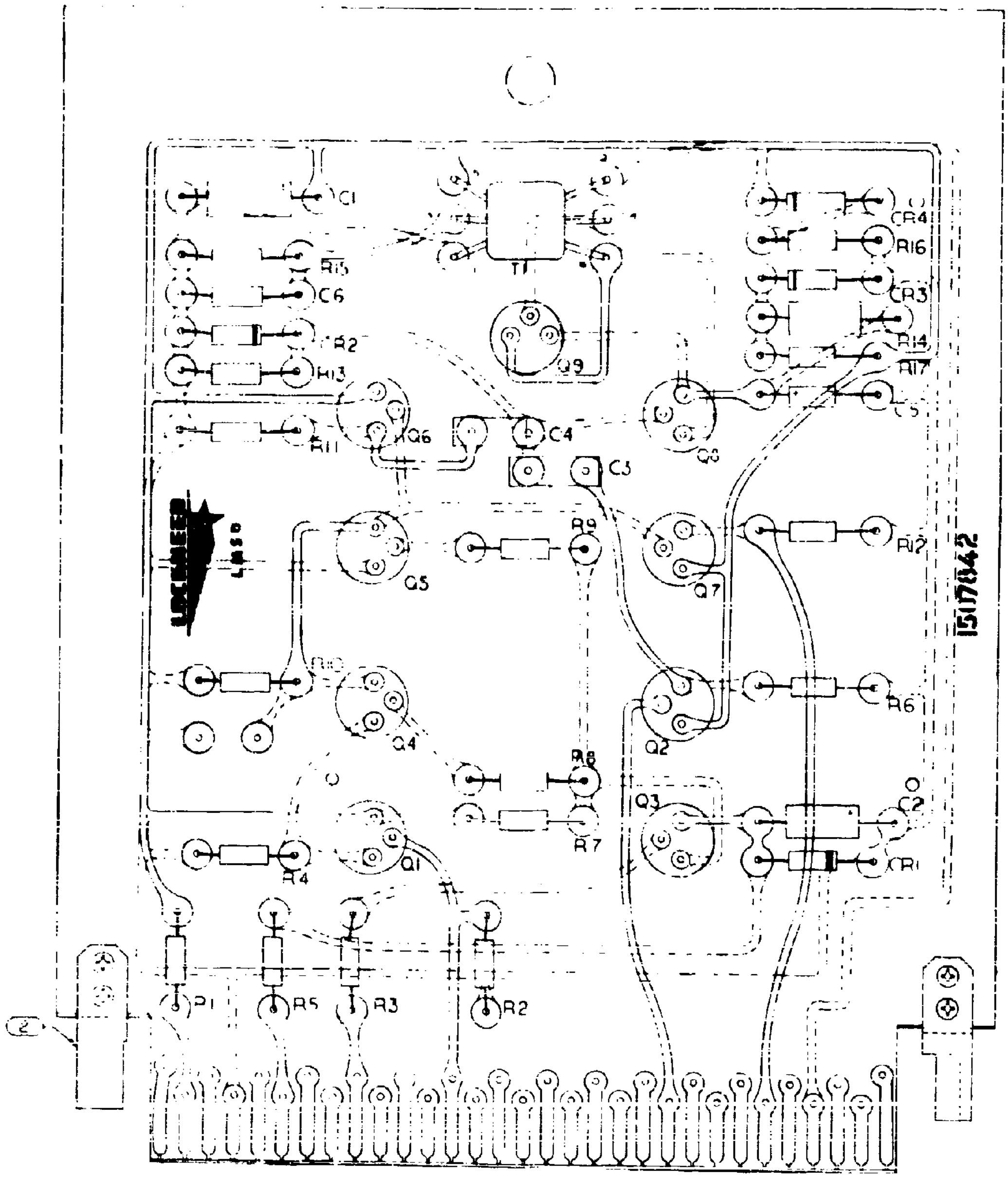


Fig. A-11 Programmer



GROUND

SYNC PULSE FROM EIGHT-BIT SHIFT REGISTER AND GATE

+ 20V

SYNC PULSES FROM FRAME SYNC SEPARATOR

SUBCOM SYNC PULSES TO SYNC GATE

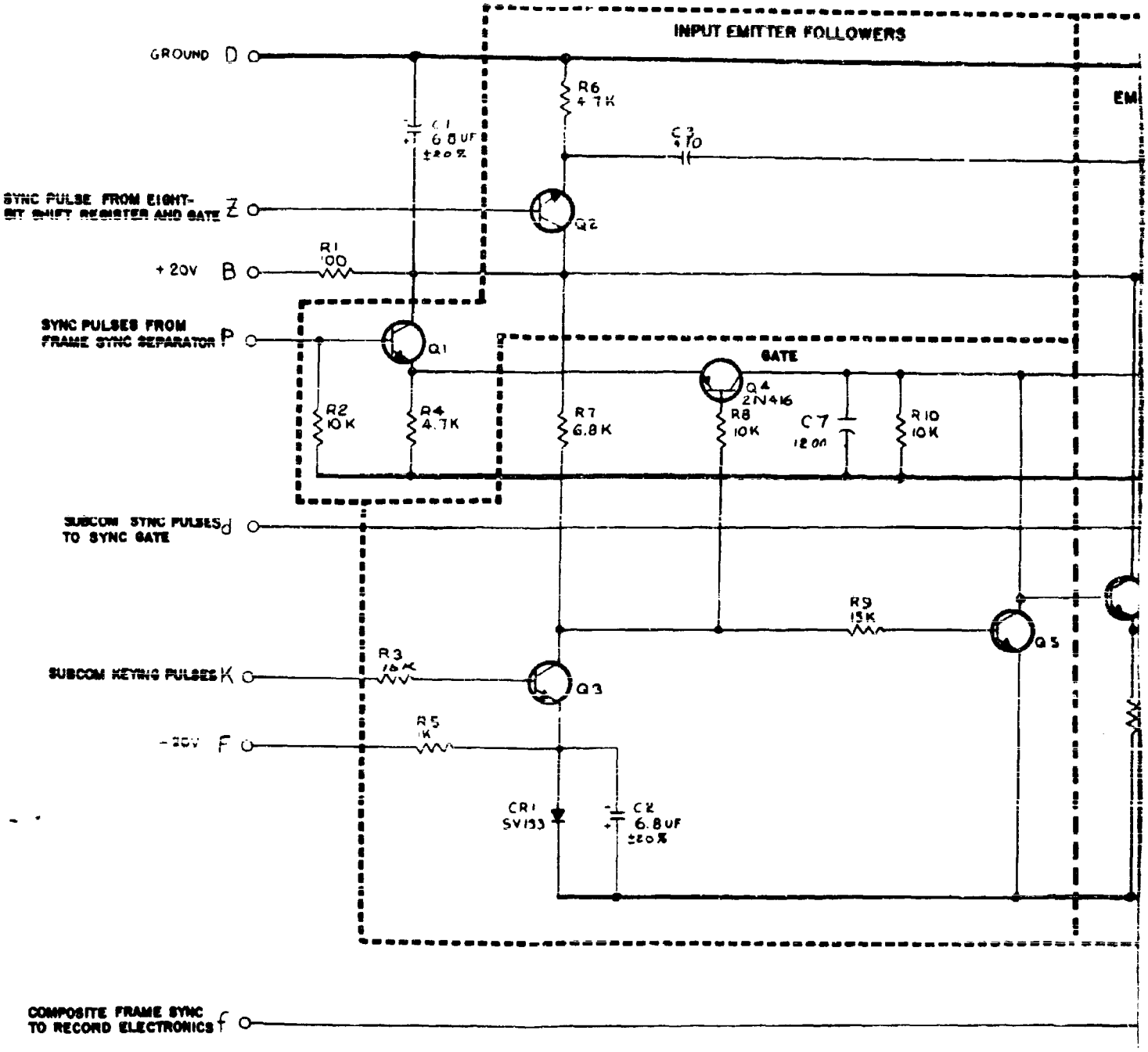
SUBCOM KEYING PULSES

- 20V

PARTS LIST

Reference Designation	Part No.	Vendor or Mil Spec
[illegible]	[illegible]	Sprague Electric Co., North Adams, Mass
[illegible]	DM15F471J	Electro Motive Mfg. Co., Inc., Willimantic, Conn
[illegible]	[illegible]	Sprague Electric Co., North Adams, Mass
[illegible]	[illegible]	[illegible] Conn
CR1	[illegible]	[illegible] Wakefield, Mass
CR2	[illegible]	Pacific Semiconductors, Inc., Culver City, Calif
CR3	[illegible]	Hoffman Electronics Co., Evanston, Ill
CR4	[illegible]	[illegible] Lowell, Mass
[illegible]	[illegible]	[illegible] Lowell, Mass
Q4	[illegible]	Raytheon Mfg. Co., Newton, Mass
R1	[illegible]	MIL-R-11
[illegible]	[illegible]	MIL-R-11
R3	[illegible]	MIL-R-11
R4	[illegible]	MIL-R-11
[illegible]	[illegible]	MIL-R-11
[illegible]	[illegible]	MIL-R-11
[illegible]	[illegible]	MIL-R-11
[illegible]	[illegible]	MIL-R-11
[illegible]	[illegible]	MIL-R-11
T	[illegible]	[illegible] Santa Monica, Calif

COMPOSITE FRAME SYNC TO RECORD ELECTRONICS


INPUT EMITTER FOLLOWERS
GROUND D
R6 4.7K
C1 6.8UF ±20%
C3 .10
SYNC PULSE FROM EIGHT-BIT SHIFT REGISTER AND GATE Z
Q2
+20V B
R1 100
SYNC PULSES FROM FRAME SYNC SEPARATOR P
Q1
GATE
Q4 2N416
R2 10K
R4 4.7K
R7 6.8K
R8 10K
C7 1200
R10 10K
SUBCOM SYNC PULSES TO SYNC GATE d
R9 15K
Q5
SUBCOM KEYING PULSES K
R3 10K
Q3
-20V F
R5 1K
CR1 SV133
C2 6.8UF ±20%
COMPOSITE FRAME SYNC TO RECORD ELECTRONICS f

B

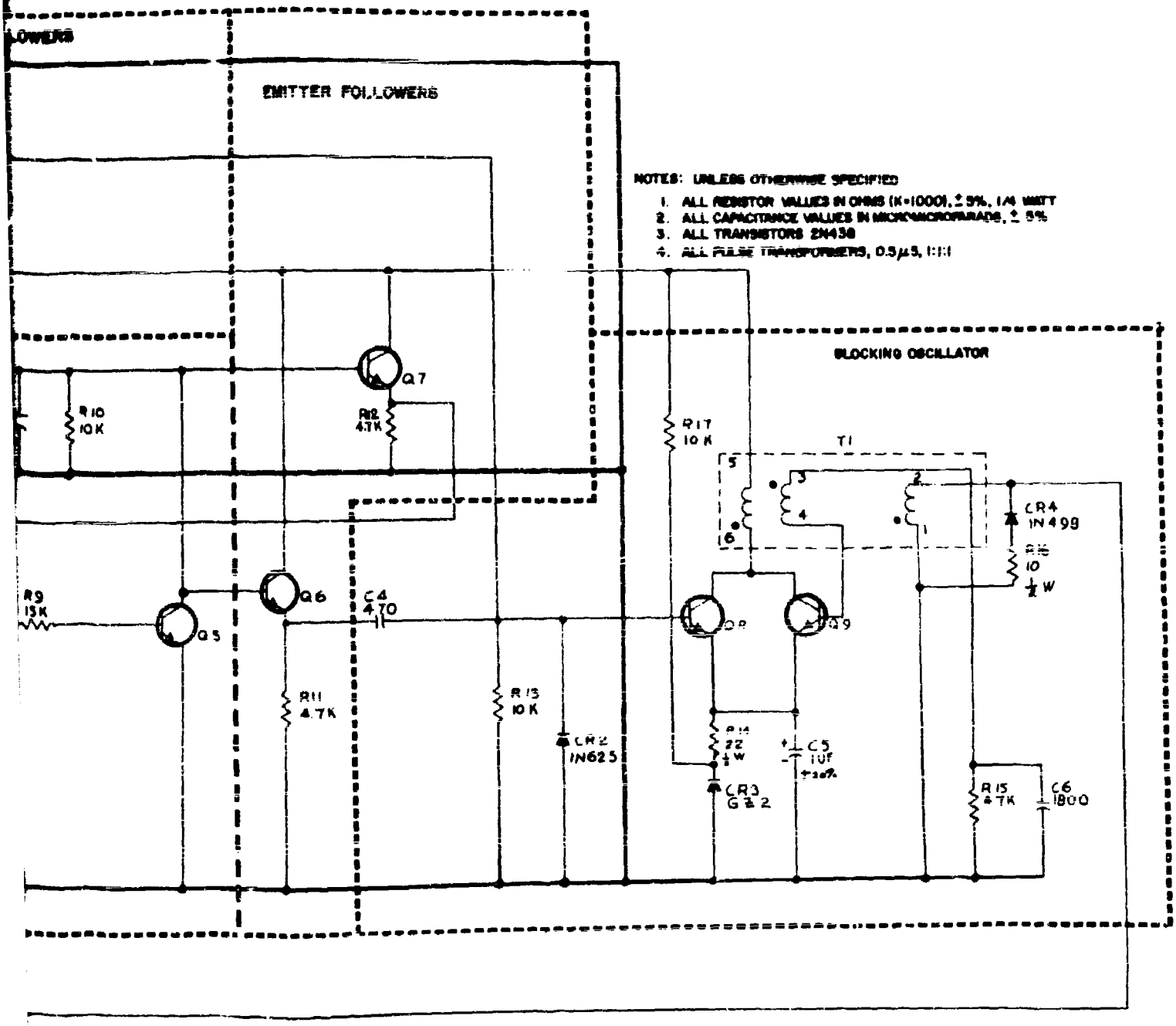
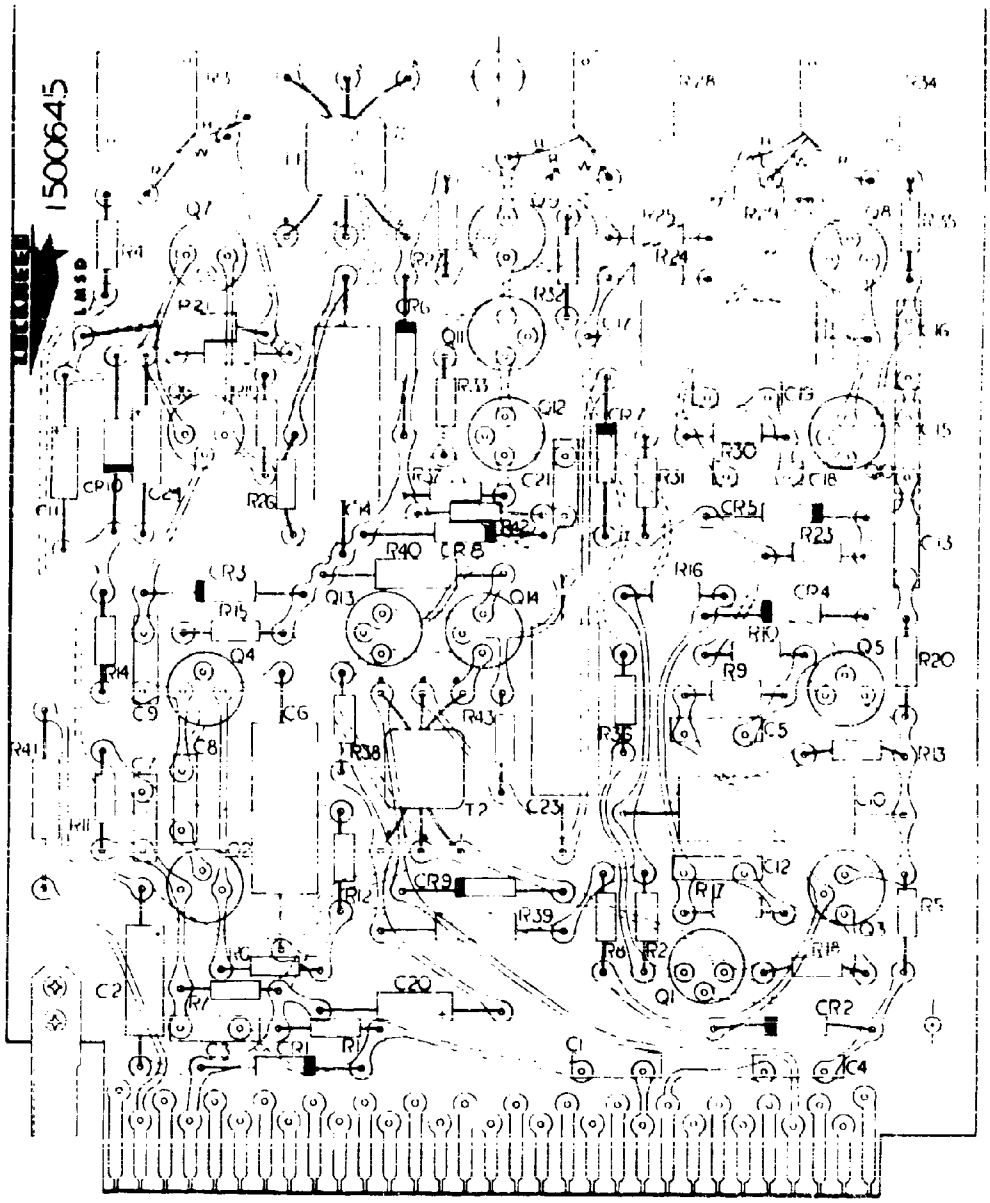
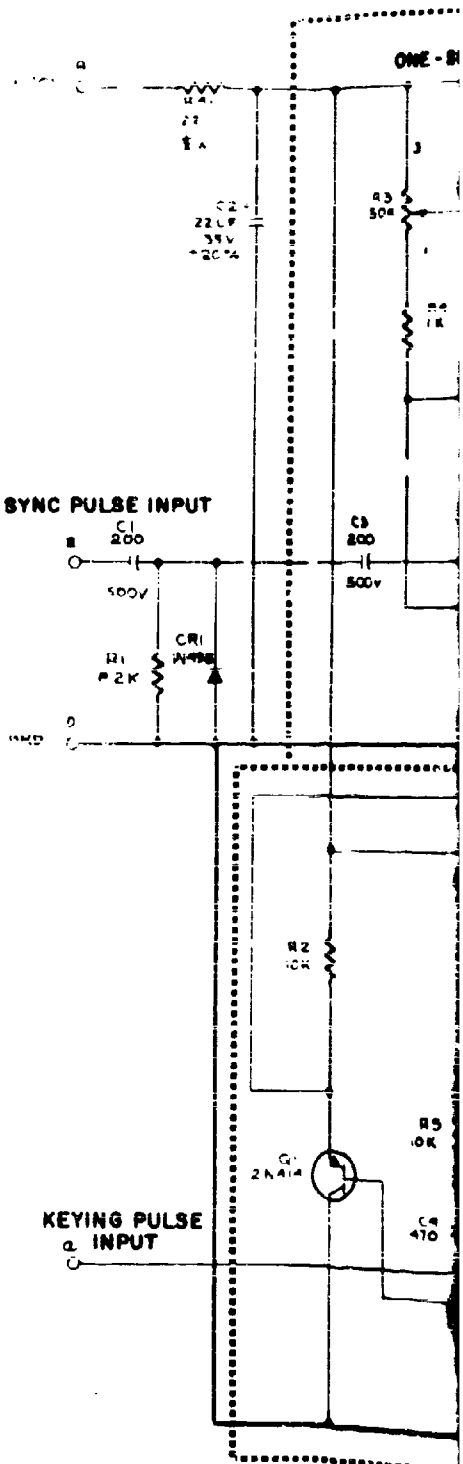


Fig. A-12 Sync Selector, Vibration

1500645

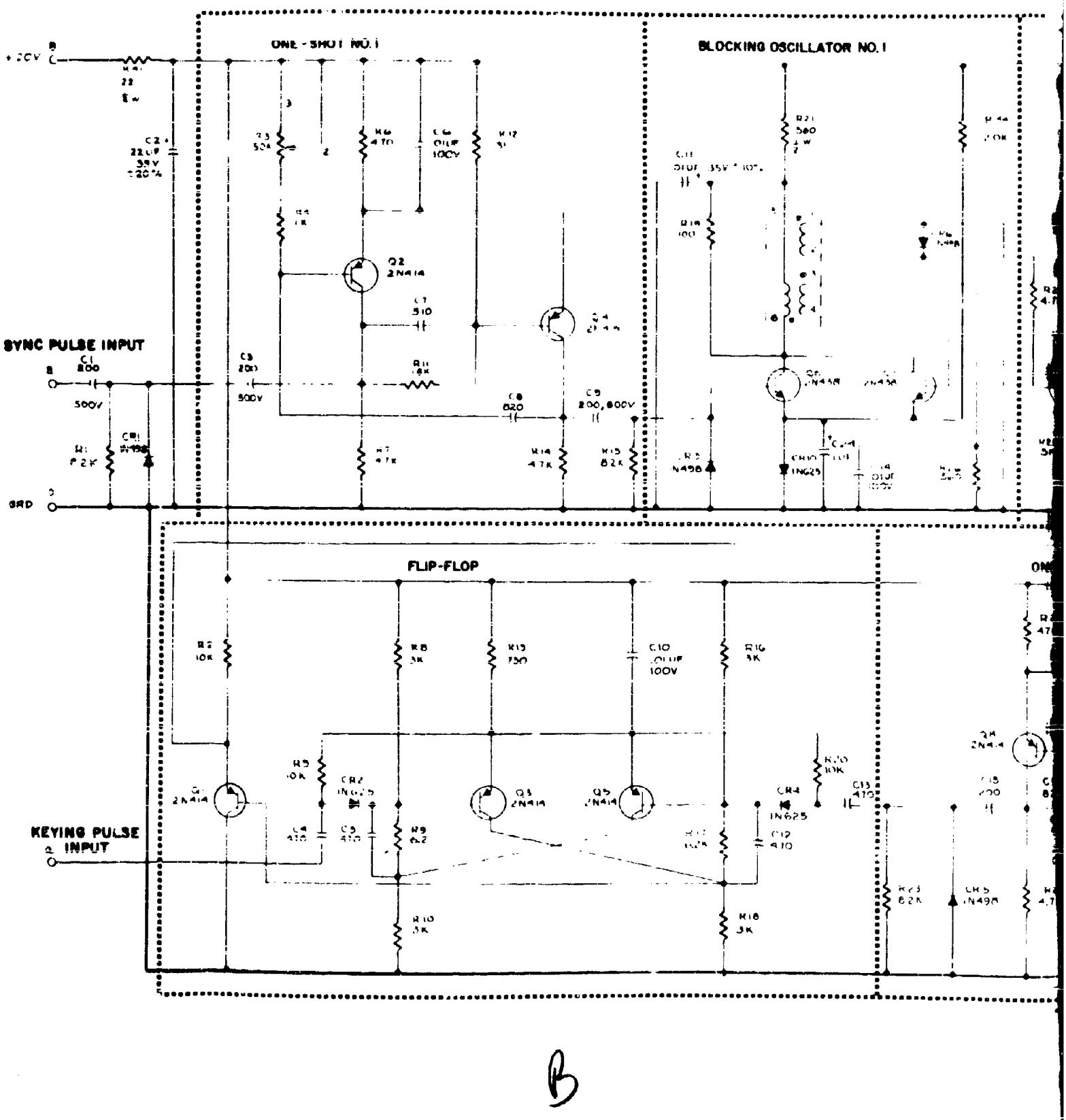




PARTS LIST

Reference Designation	Part No.	Name or Description
C1, 3, 9, 15, 16, 21	[illegible]	[illegible]
C4	[illegible]	[illegible]
C5, 12, 13, C6, 14, 17, 23	[illegible]	[illegible]
C7, 10	[illegible]	[illegible]
C8, 18	[illegible]	[illegible]
C11, 22	[illegible]	[illegible]
C24	[illegible]	[illegible]
CR1, 3, 5 thru 9	[illegible]	[illegible]
CR2, 4, 10	[illegible]	[illegible]
Q1 thru 8, 11	[illegible]	[illegible]
Q9, 7, 9, 11, 13, 14	[illegible]	[illegible]
Q12	[illegible]	[illegible]
R1, 15, 20, 43	[illegible]	[illegible]
R2 thru 5, 9, 13	[illegible]	[illegible]
R6, 16, 17, 18, 23, 24, 26, 30, 31, 34, 38, 39, 40, 41, 42	[illegible]	[illegible]
T2	[illegible]	[illegible]

A


ONE - SHOT NO. 1
BLOCKING OSCILLATOR NO. 1
SYNC PULSE INPUT
FLIP-FLOP
KEYING PULSE INPUT
Q2 2N414
Q1 2N414
Q3 2N414
Q5 2N414
Q6 2N438
Q4 2N414
CR1 N498
CR2 IN625
CR3 N498
CR4 IN625
CR5 N498
CR6 IN625
C1 800
C2 22 UF 35V ±20%
C3 200
C4 820
C5 820
C6 .01UF 100V
C7 510
C8 820
C9 200, 800V
C10 .01UF 100V
C11 .01UF 35V ±10%
C12 410
C13 410
R1 2.2K
R2 10K
R3 50K
R4 1K
R5 10K
R6 470
R7 47K
R8 3K
R9 6.2
R10 3K
R11 18K
R12 5K
R13 750
R14 47K
R15 82K
R16 3K
R17 3K
R18 100
R21 500 ½ W
R22 10K
R23 82K
+20V
GRD

B

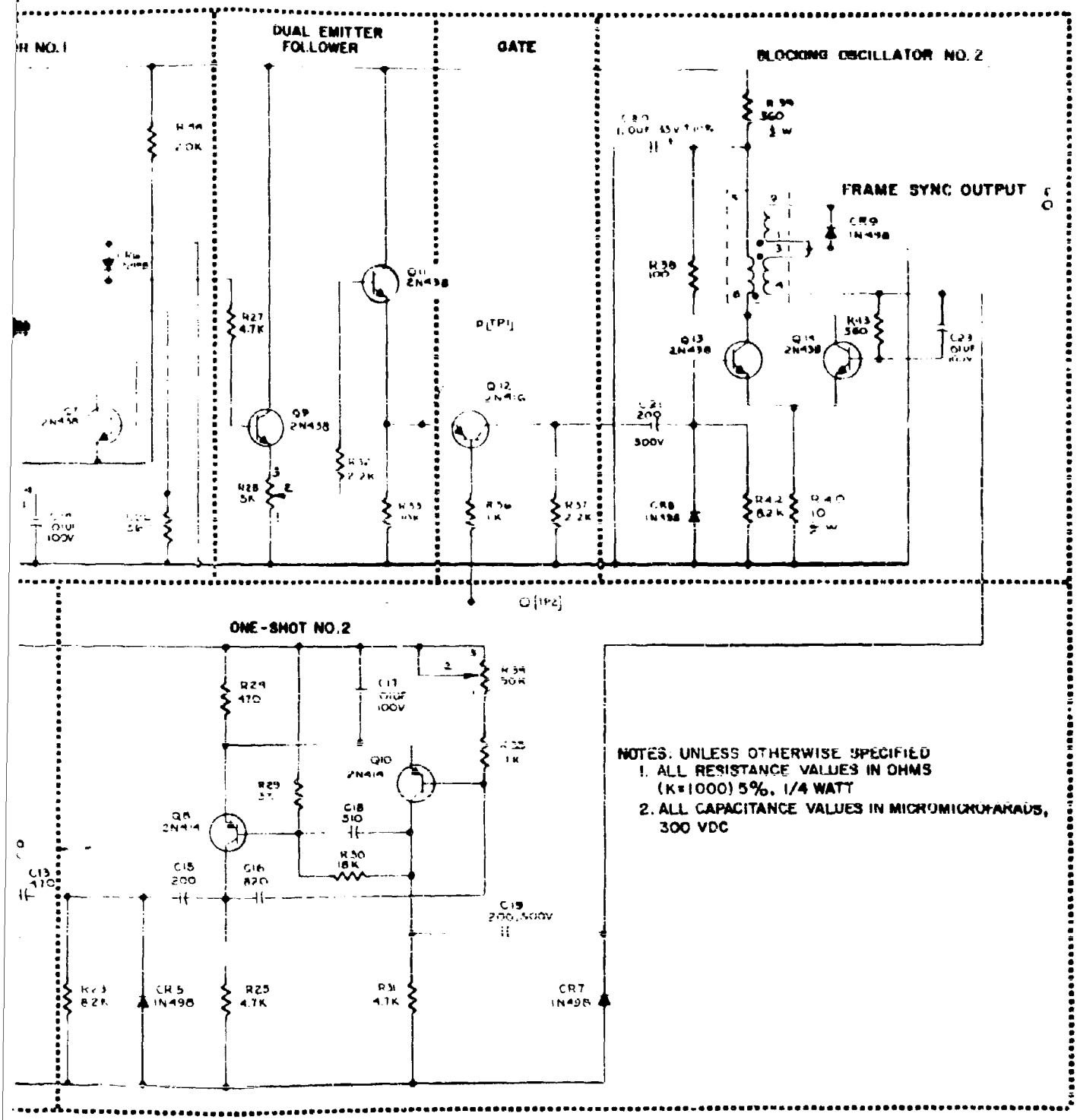
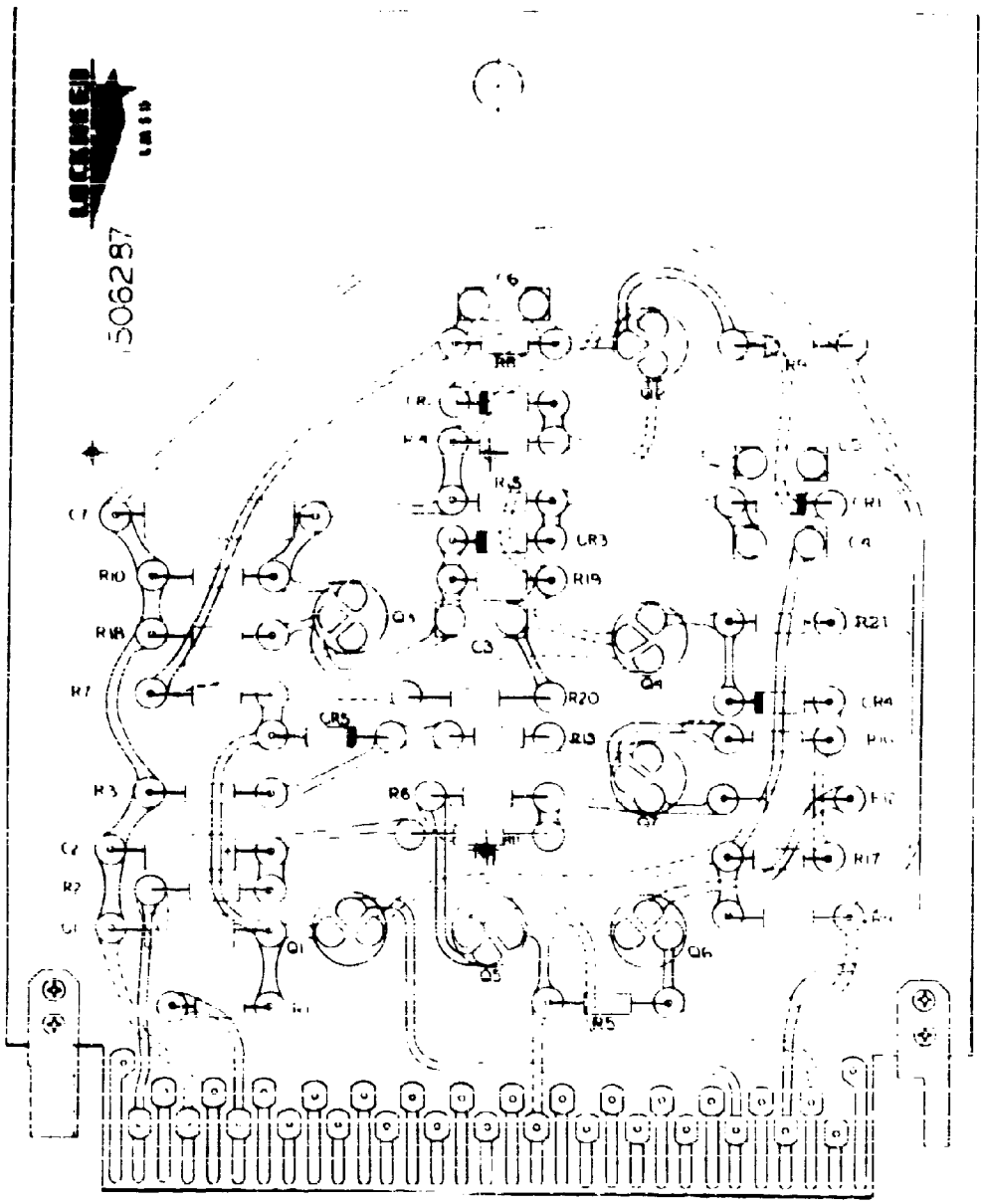


Fig. A-13 Sync Gate, Vibration

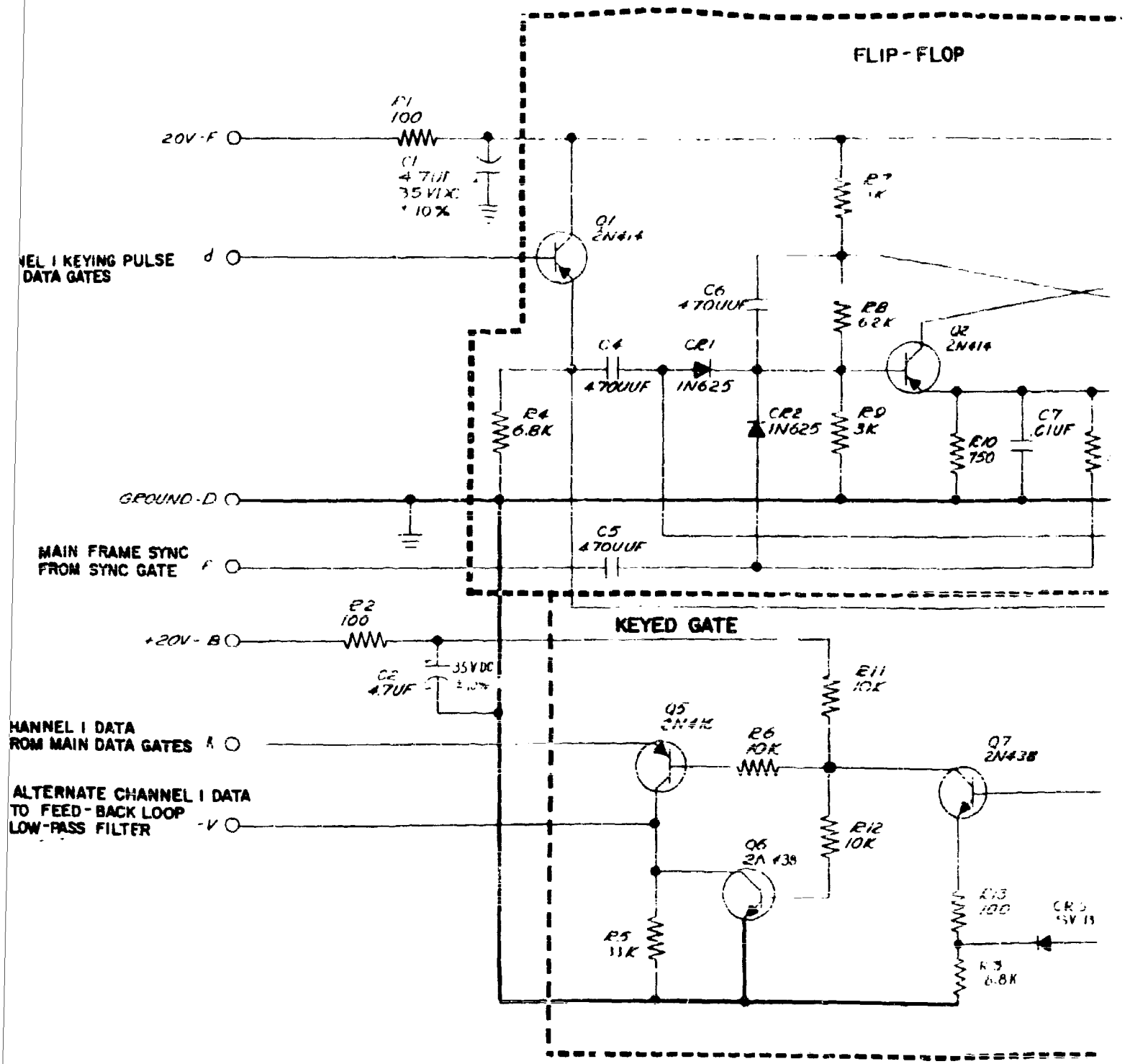


CHANNEL I KE
FROM DATA GA

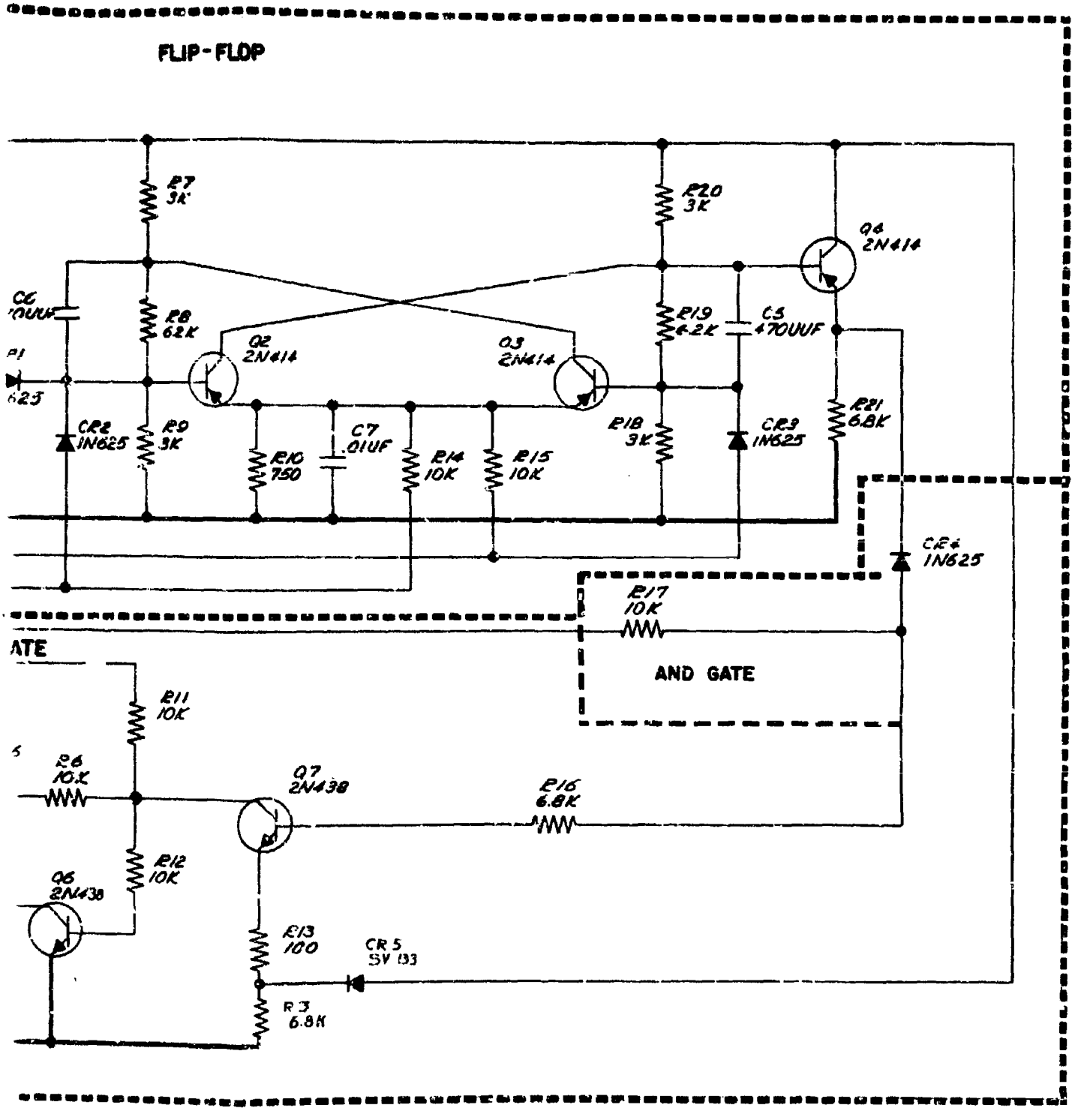
MAIN
FROM

CHANNEL I
FROM MAIN

ALTERNA
TO FEED
LOW-PASS

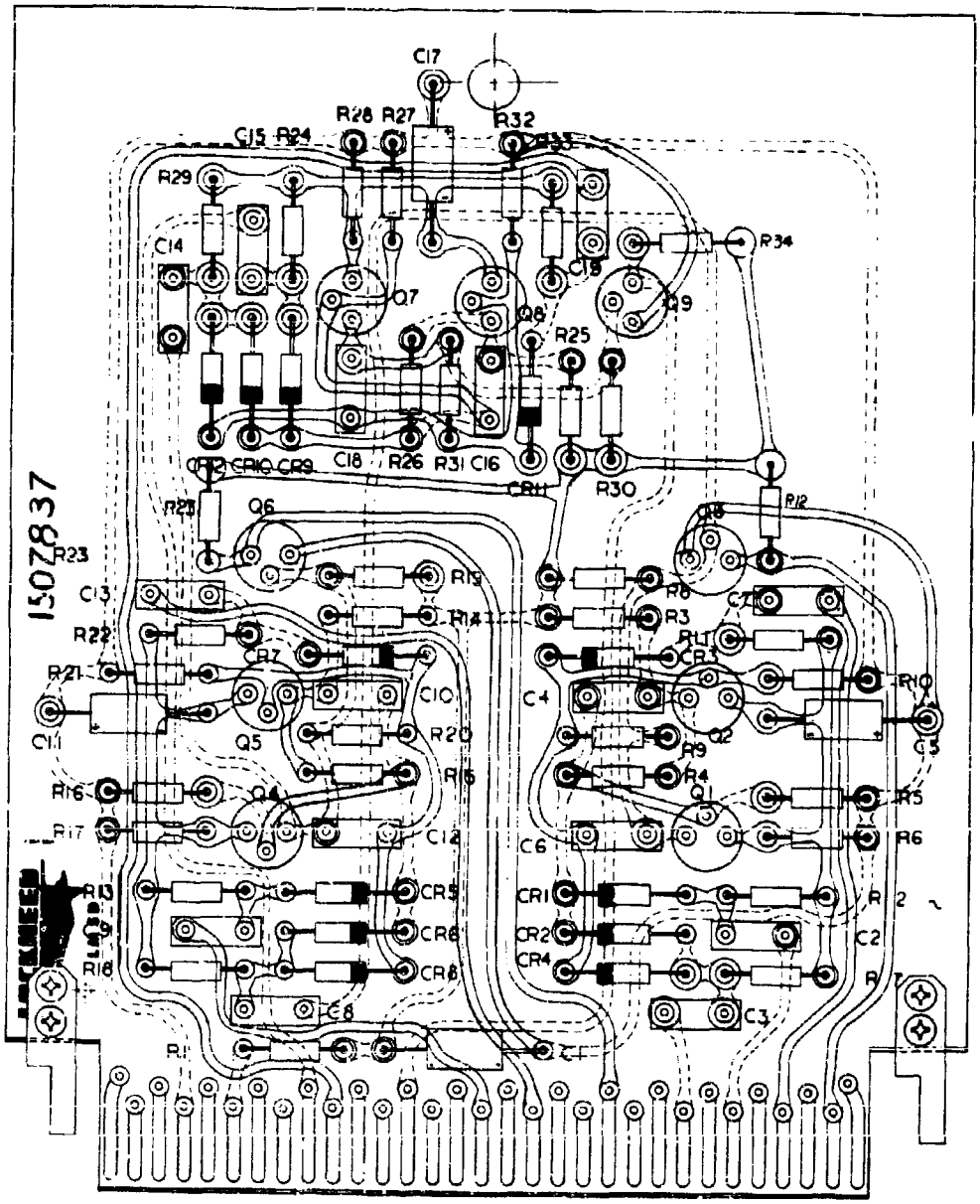

FLIP - FLOP
KEYED GATE
20V - F
R1 100
C1 4.7UF 35 V DC ± 10%
Q1 2N414
NEL I KEYING PULSE
DATA GATES
d
C6 470UUF
R8 62K
Q2 2N414
C4 470UUF
CR1 1N625
R4 6.8K
CR2 1N625
R9 3K
R10 750
C7 .01UF
GROUND - D
C5 470UUF
MAIN FRAME SYNC
FROM SYNC GATE
f
R2 100
+20V - B
C2 4.7UF 35 V DC
R11 10K
Q5 2N414
R6 10K
Q7 2N438
HANNEL I DATA
ROM MAIN DATA GATES
A
ALTERNATE CHANNEL I DATA
TO FEED - BACK LOOP
LOW-PASS FILTER
-V
R12 10K
Q6 2N438
R5 11K
R13 100
R14 6.8K

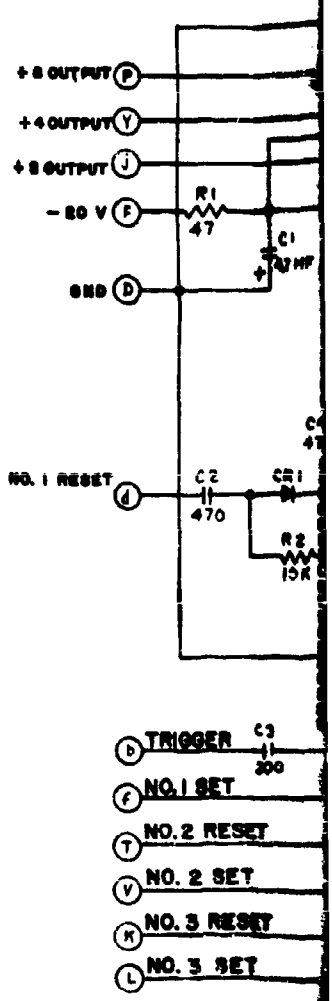
B



NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTANCE VALUES IN OHMS (K=1000)

Fig. A-14 Zero Data Selector

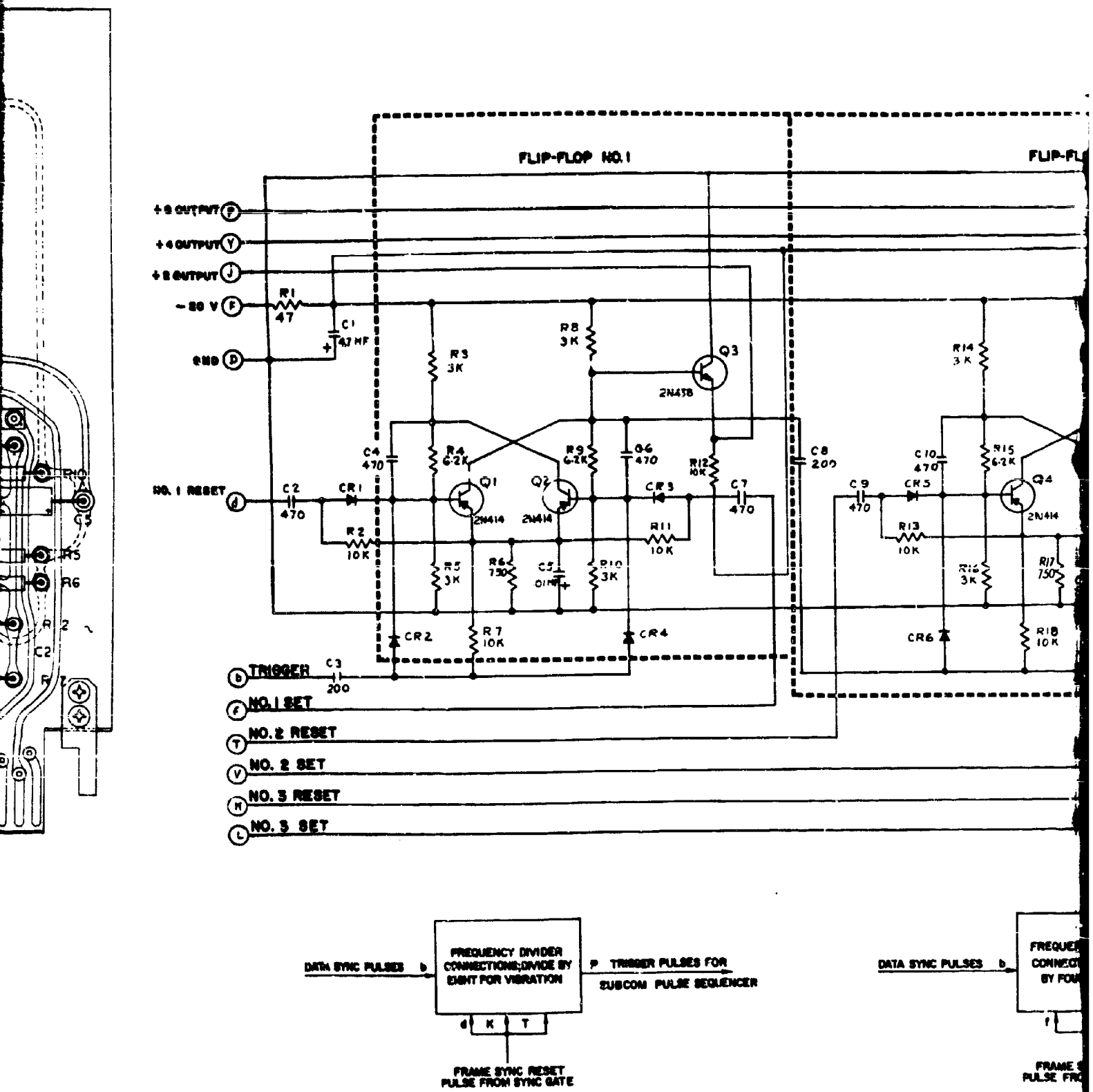




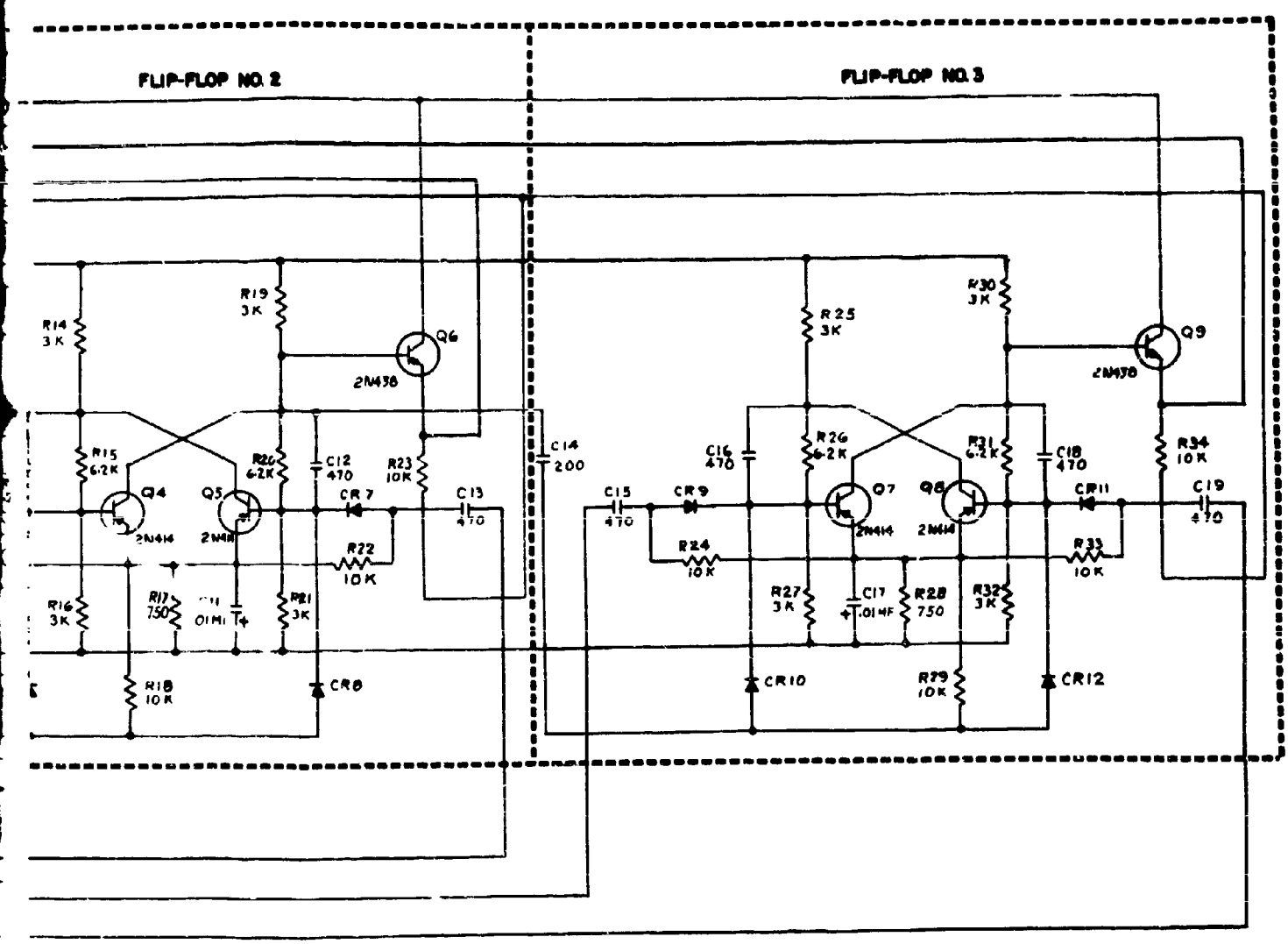
PARTS LIST

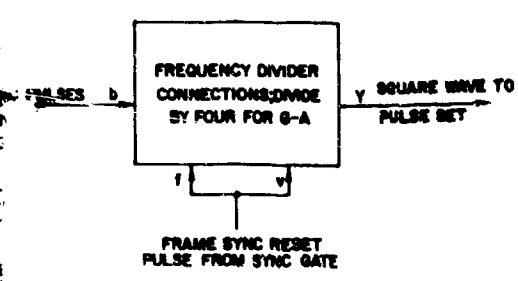
Reference Designation	Part No.	Vendor & Mil. Spec.
C1	150D477X9033A2	Sprague Electric Co. North Adams Mass.
C2 3 4 5 7 9 10 12, 15		
13 16 18 19	DM11F471J	El Menco. Los Angeles Calif.
C6 11 17	150D103X9033A2	Sprague Electric Co. North Adams. Mass.
C8 14	DM11F301J	El Menco. Los Angeles Calif.
CR1 thru 12	1N643	Pacific Semiconductor Culver City Calif.
Q1 thru 9	2N414	Raytheon Mfg. Co. Newton Mass.
R1	RC07GF470J	MIL-R-11
R2 7 11 12 13 17 20 22 24 29 32 34	RC07GF103J	MIL-R-11
R3 5 8 10 14 16 19 21 27 30 33	RC07GF393J	MIL-R-11
R4 9 15 26 28 31	RC07GF153J	MIL-R-11
R6 17 23	RC07GF751J	MIL-R-11

A


FLIP-FLOP NO. 1
FLIP-FL
÷8 OUTPUT P
÷4 OUTPUT Y
÷2 OUTPUT J
-28 V F
GND D
R1 47
C1 4.7 MF
R3 3K
R8 3K
Q3
2N438
R14 3K
C4 470
R4 6.2K
R9 6.2K
C6 470
R12 10K
C8 200
C10 470
R15 6.2K
Q4
2N414
NO. 1 RESET d
C2 470
CR1
Q1
Q2
2N414
CR3
C7 470
C9 470
CR5
R2 10K
R11 10K
R13 10K
R5 3K
R6 750
C5 .01MF
R10 3K
R16 3K
R17 750
CR2
R7 10K
CR4
CR6
R18 10K
TRIGGER b
C3 200
NO. 1 SET e
NO. 2 RESET T
NO. 2 SET V
NO. 3 RESET H
NO. 3 SET L
DATA SYNC PULSES b
FREQUENCY DIVIDER CONNECTIONS; DIVIDE BY EIGHT FOR VIBRATION
P TRIGGER PULSES FOR SUBCOM PULSE SEQUENCER
d K T
FRAME SYNC RESET PULSE FROM SYNC GATE
DATA SYNC PULSES b
FREQUE
CONNEC
BY FOU
FRAME S
PULSE FRO

b



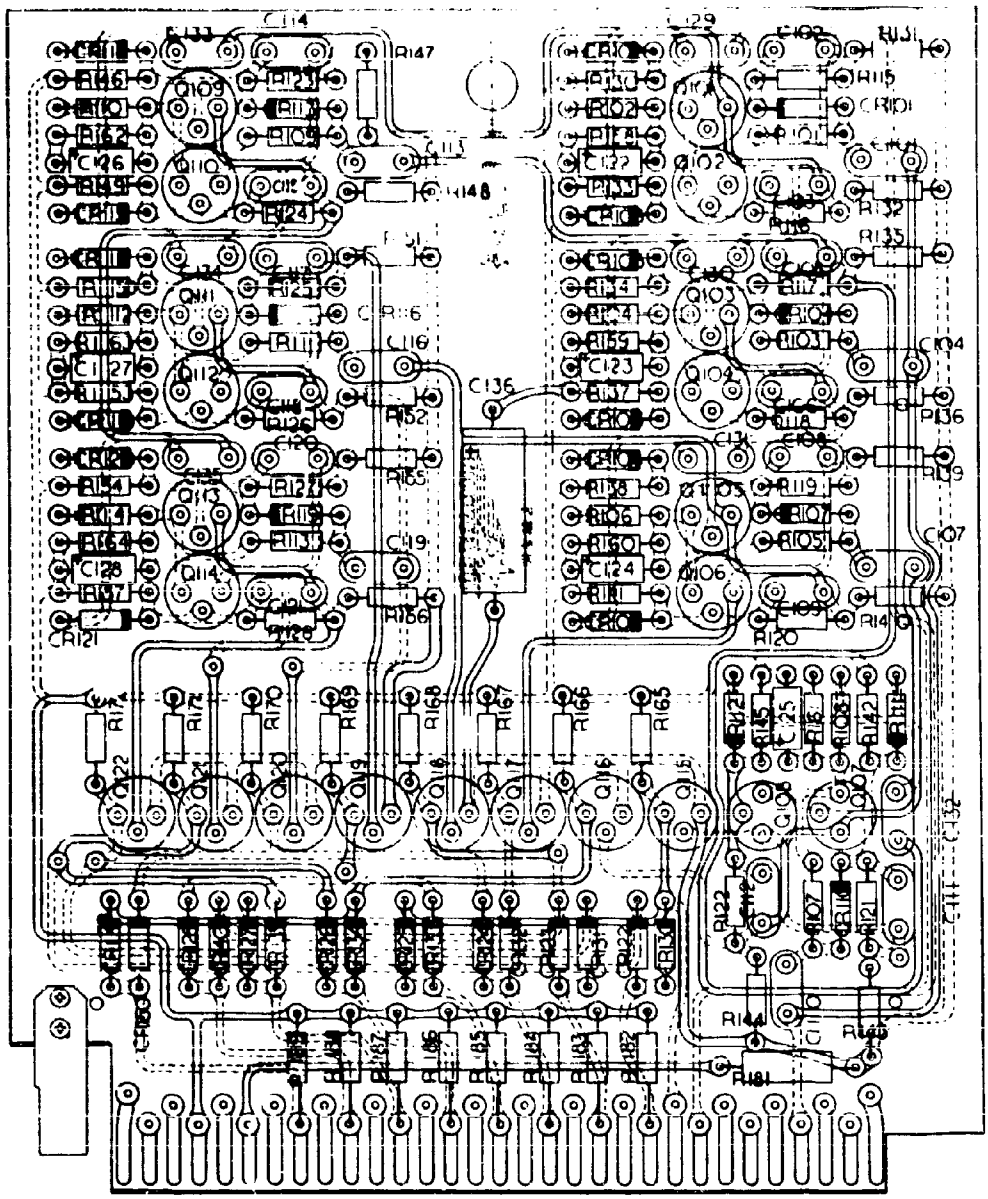


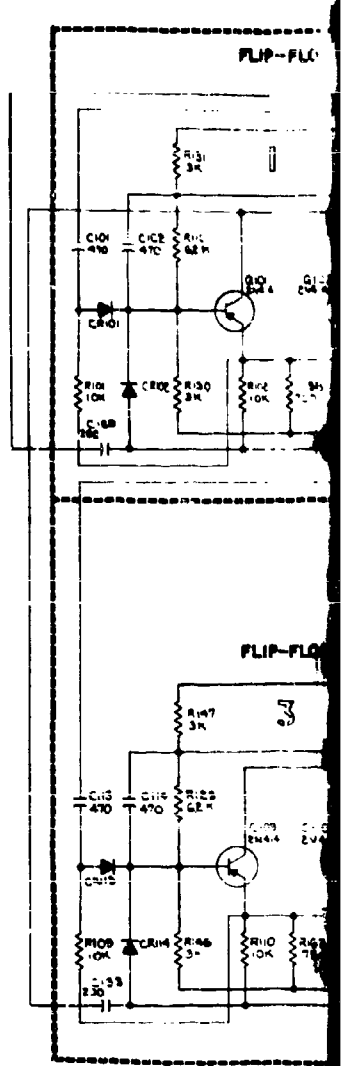
1. ALL RESISTANCE VALUES IN OHMS (K=1000) ±5% 1/4 WATT
2. ALL CAPACITANCE VALUES IN MICROMICROFARADS
3. ALL DIODES IN626

NOTE: UNLESS OTHERWISE SPECIFIED

C

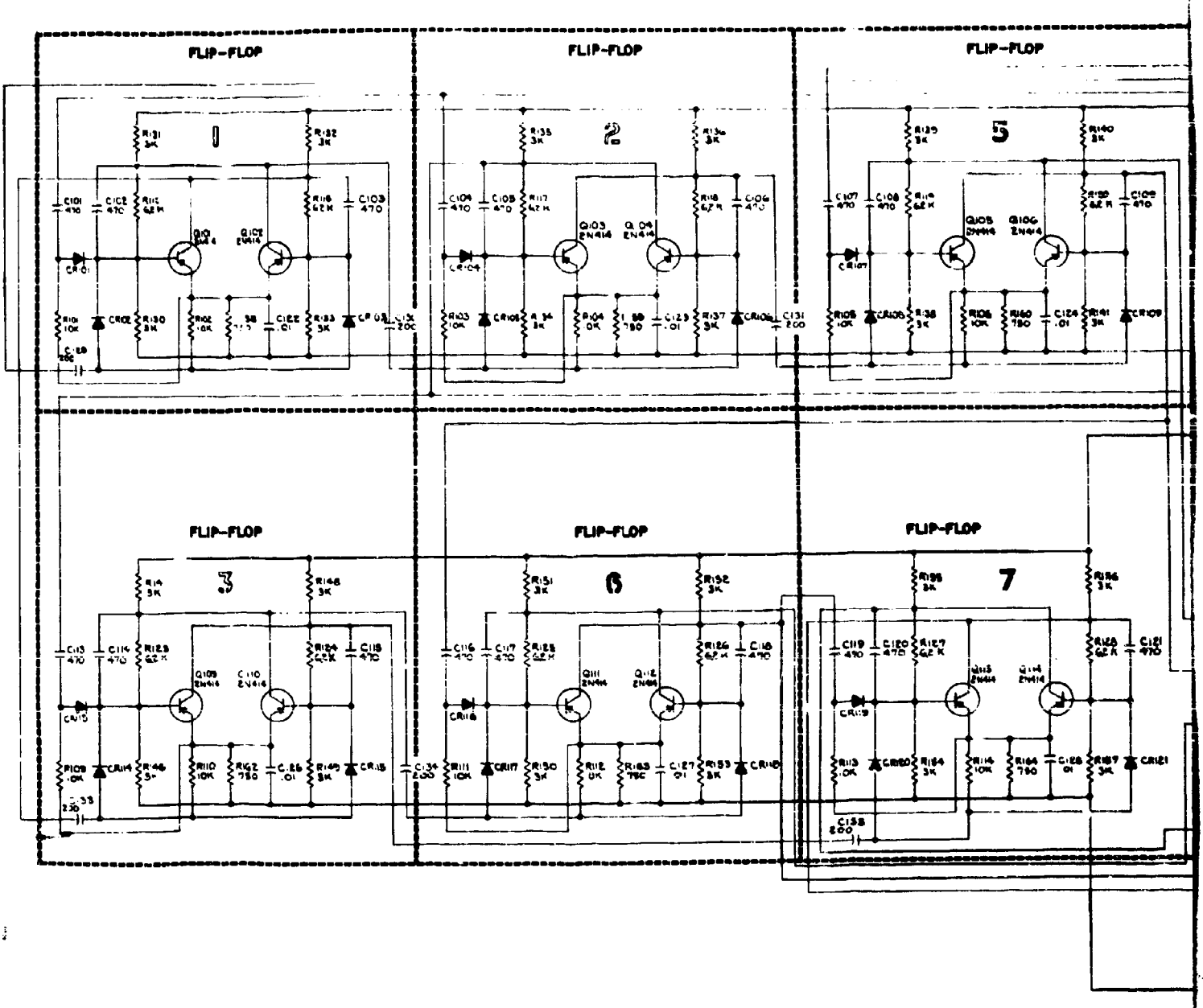
Fig. A-15 Frequency Divider, Vibration



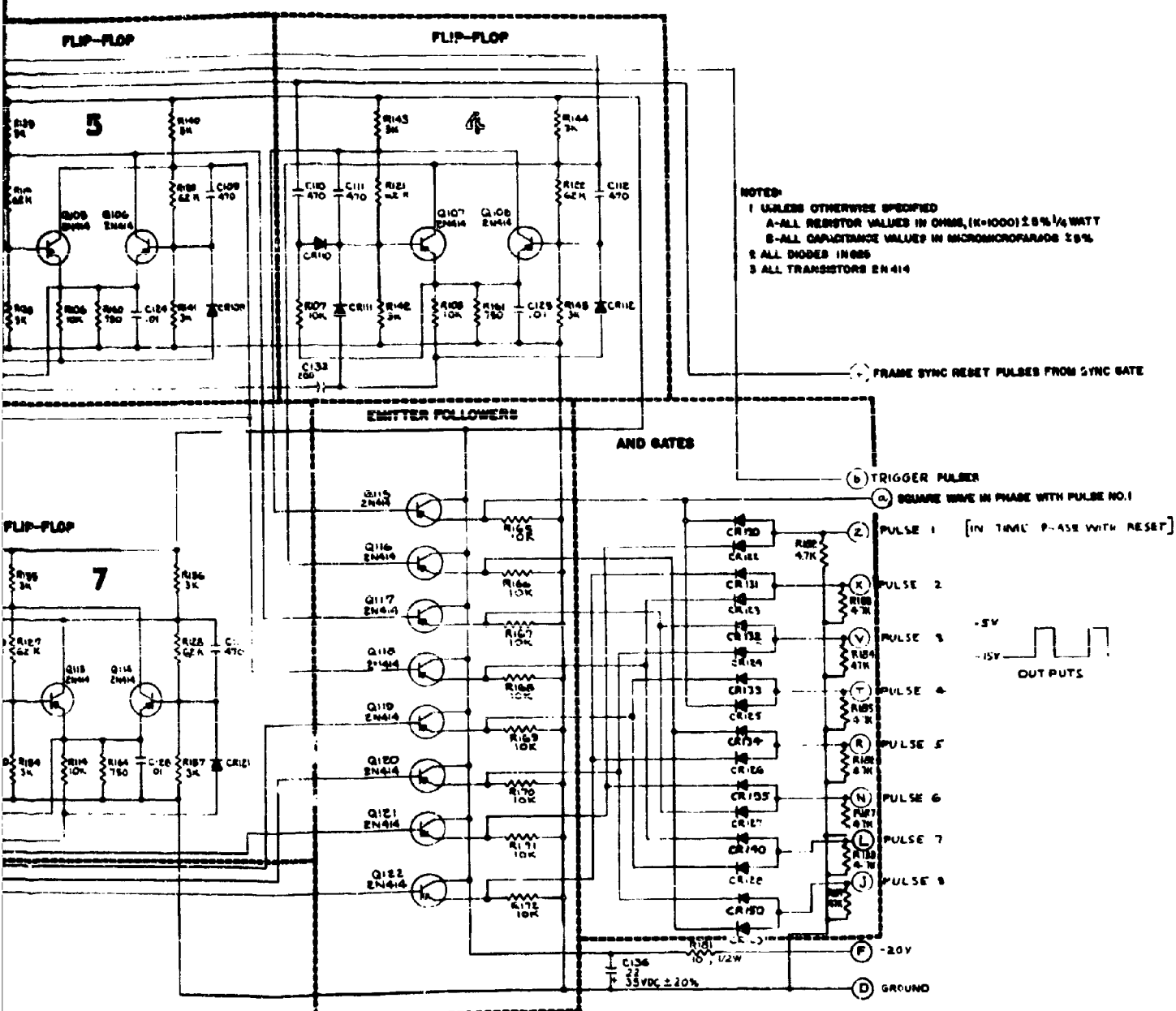


PARTS LIST

Reference Designation	Part No.	Vendor or MIL Spec.
C101 thru 113		
C114 thru 125		
C126 thru 136		
C137		
C138,139 thru 151, 160, 166		
Q101 thru 170		
R101 thru 114, 122 thru 170		
R115 thru 121		
R123 thru 157		
R158 thru 164		
R165		
R166 thru 180		

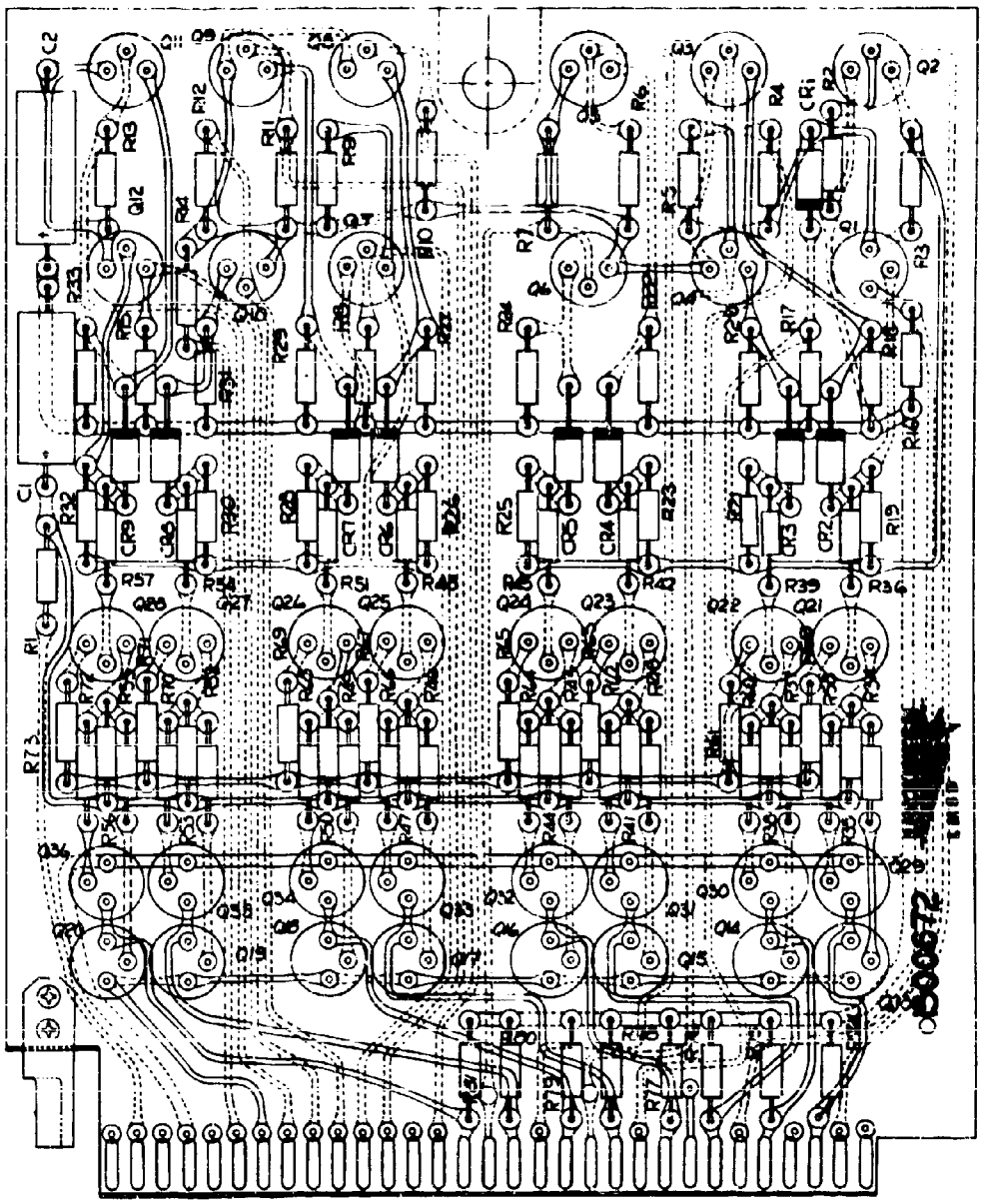


B



C

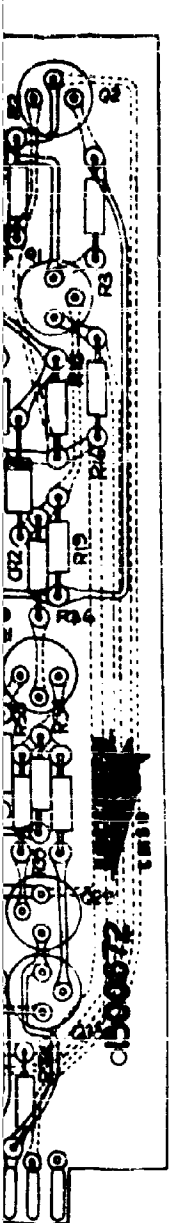
Fig. A-16 Eight-Channel Pulse Sequencer, Vibration

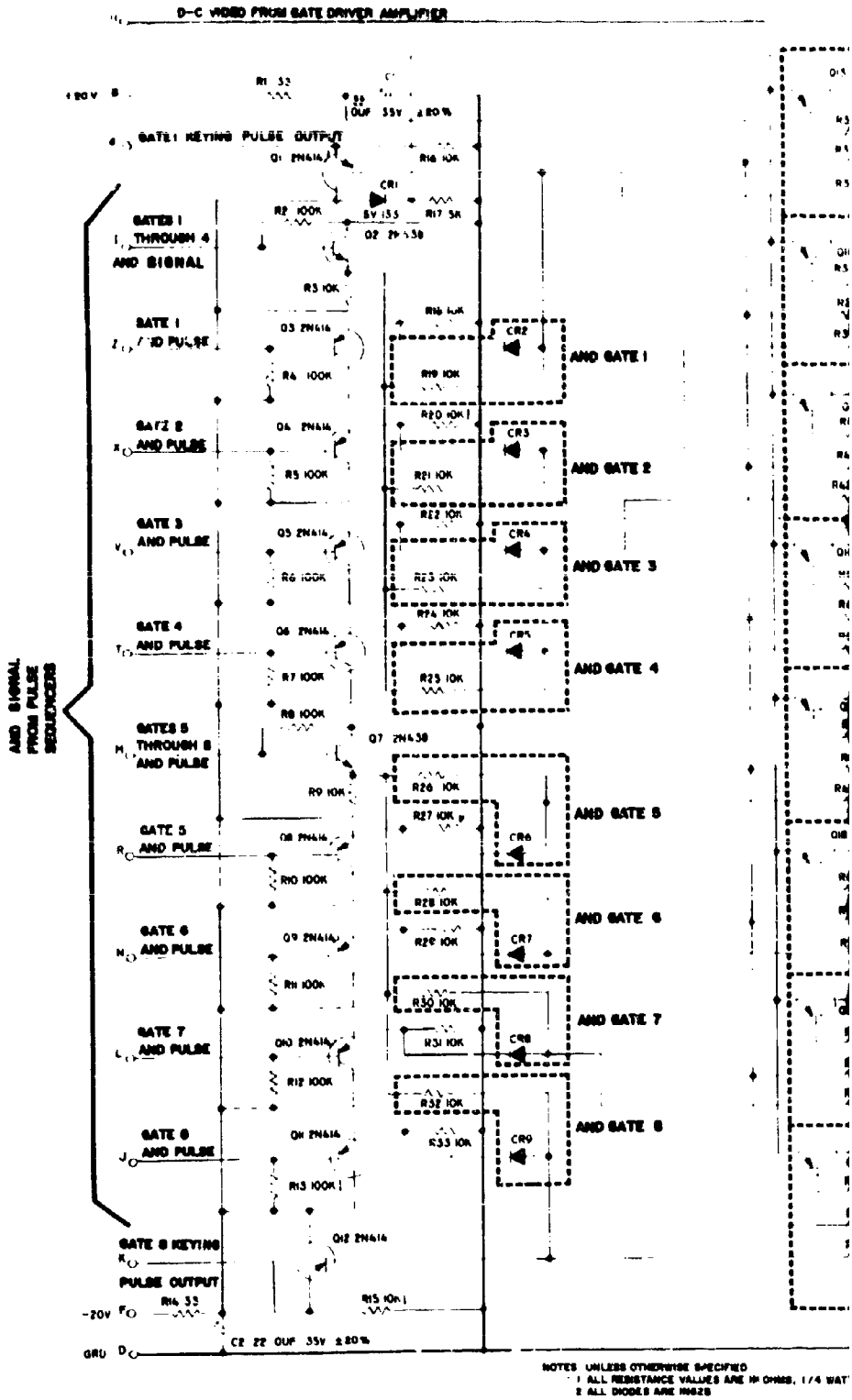


PARTS LIST

Reference Designation	Part No.	Vendor or MIL Spec.
C1, 2	116D226X9063B2	Sprague Electric Co., North Adams, Mass.
CR1	1N758	Transitron, Wakefield, Mass.
CR2 thru 9	1N625	Pacific Semiconductor, Culver City, Calif.
Q1, 3 thru 6, 8 thru 12	2N414	Raytheon, Newton, Mass.
Q2, 7, 21 thru 36	2N430	CBS-Hytron, Danvers, Mass.
Q13 thru 20	2N416	Raytheon, Newton, Mass.
R1, 14	RC07GF334J	MIL-R-11
R2, 4, 5, 6 thru 8, 10 thru 13	RC07GF104J	MIL-R-11
R3, 9, 15, 16, 18 thru 33, 37, 38, 40, 41, 43, 44, 46, 47, 48, 50, 51, 52, 53, 54, 56, 58, 59, 62, 64, 66, 68, 70, 72, 74 thru 81	RC07GF103J	MIL-R-11
R17	RC07GF472J	MIL-R-11
R34, 35, 45, 49, 60, 61, 64, 67	RC07GF332J	MIL-R-11
R36, 61, 63, 65, 67, 69 71, 73	RC07GF101J	MIL-R-11

A




D-C VIDEO FROM GATE DRIVER AMPLIFIER
GATE 1 KEYING PULSE OUTPUT
GATES 1 THROUGH 4 AND SIGNAL
GATE 1 AND PULSE
GATE 2 AND PULSE
GATE 3 AND PULSE
GATE 4 AND PULSE
GATES 5 THROUGH 8 AND PULSE
GATE 5 AND PULSE
GATE 6 AND PULSE
GATE 7 AND PULSE
GATE 8 AND PULSE
GATE 8 KEYING PULSE OUTPUT
AND SIGNAL FROM PULSE SEQUENCERS
AND GATE 1
AND GATE 2
AND GATE 3
AND GATE 4
AND GATE 5
AND GATE 6
AND GATE 7
AND GATE 8
-20V
GRD
NOTES UNLESS OTHERWISE SPECIFIED
1 ALL RESISTANCE VALUES ARE IN OHMS, 1/4 WAT
2 ALL DIODES ARE IN628

B

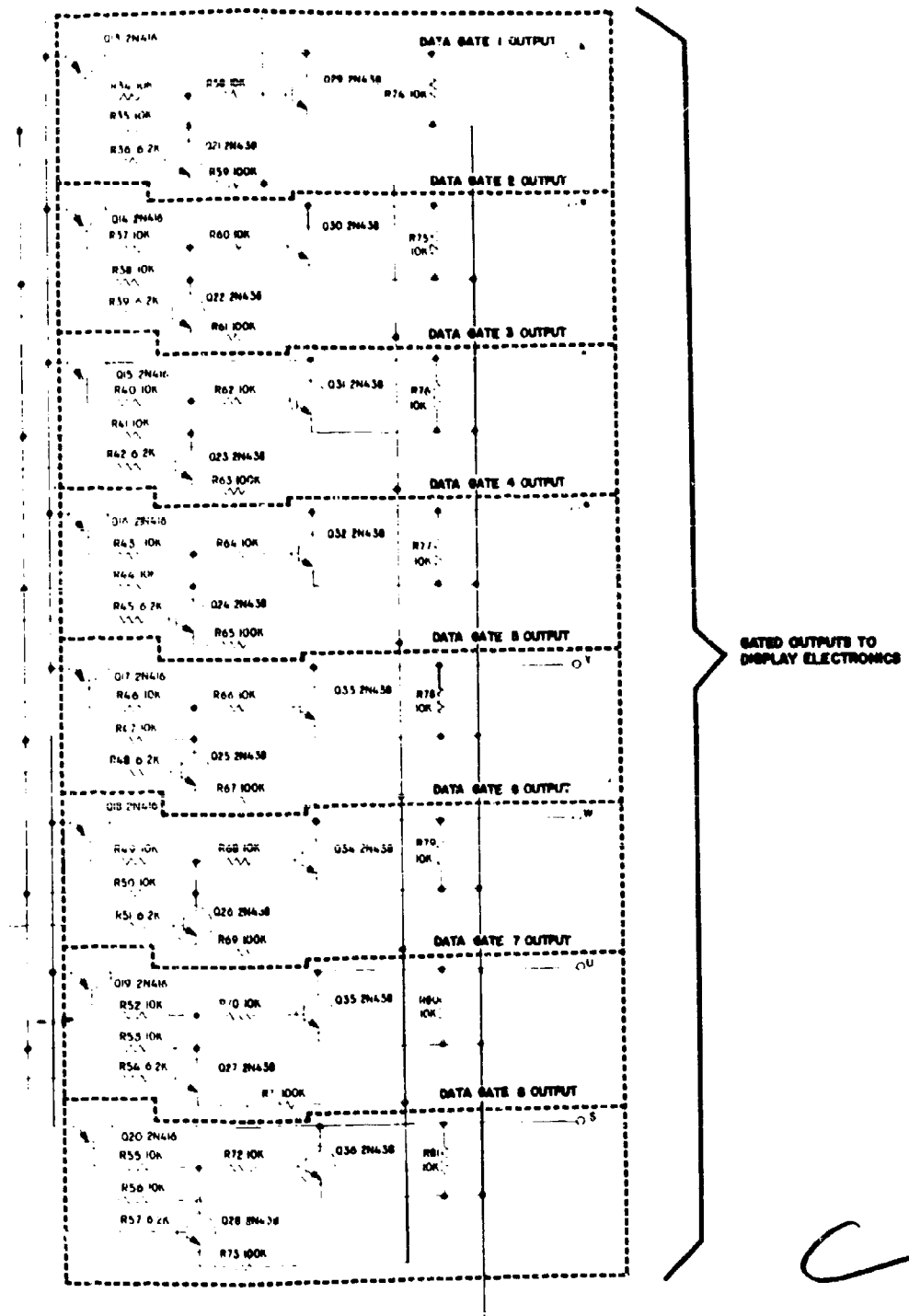
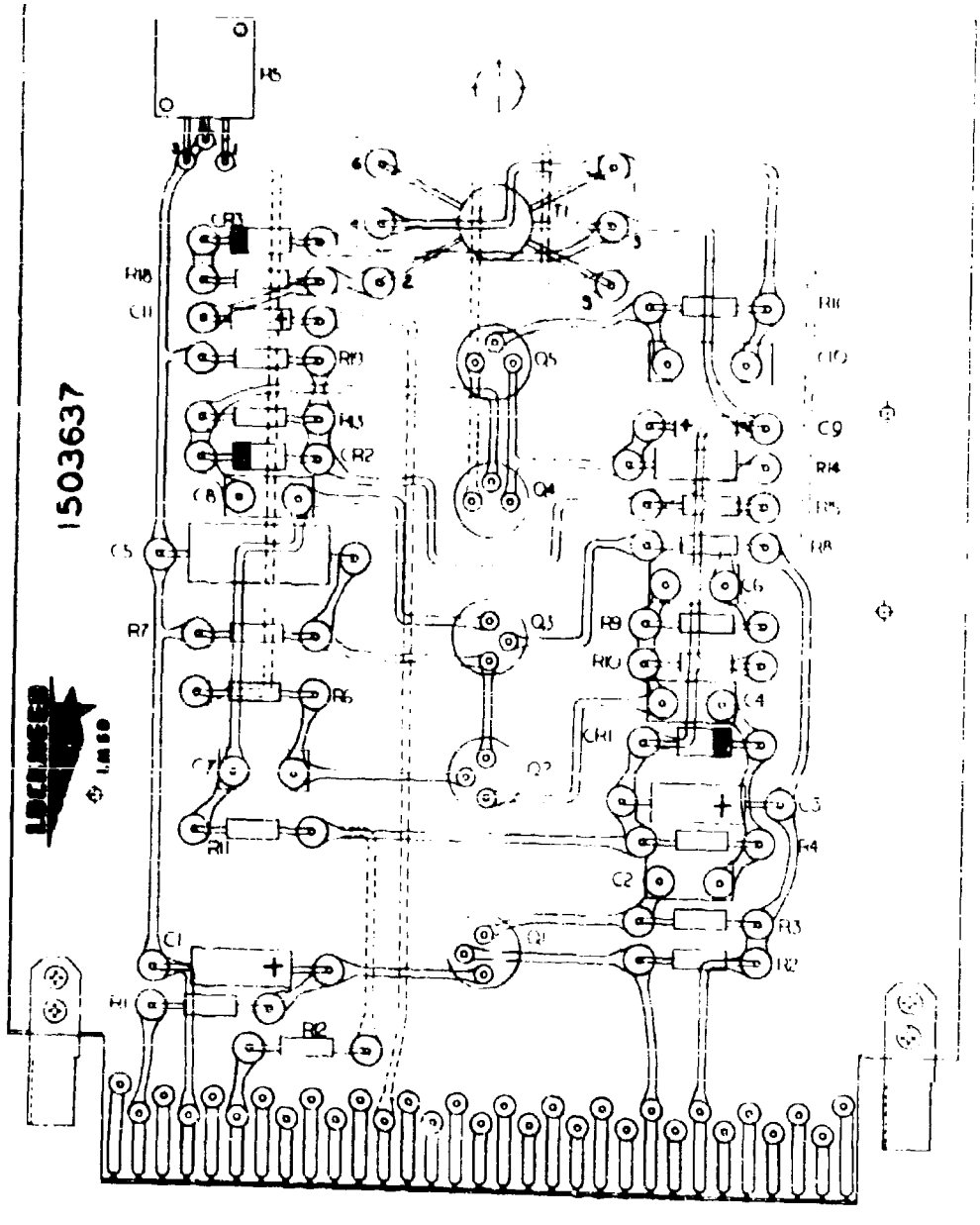


Fig. A-17 Data Gates, Vibration



B
+20V

CLOCK P
DATA SY
A
INPUT

D
GROUND

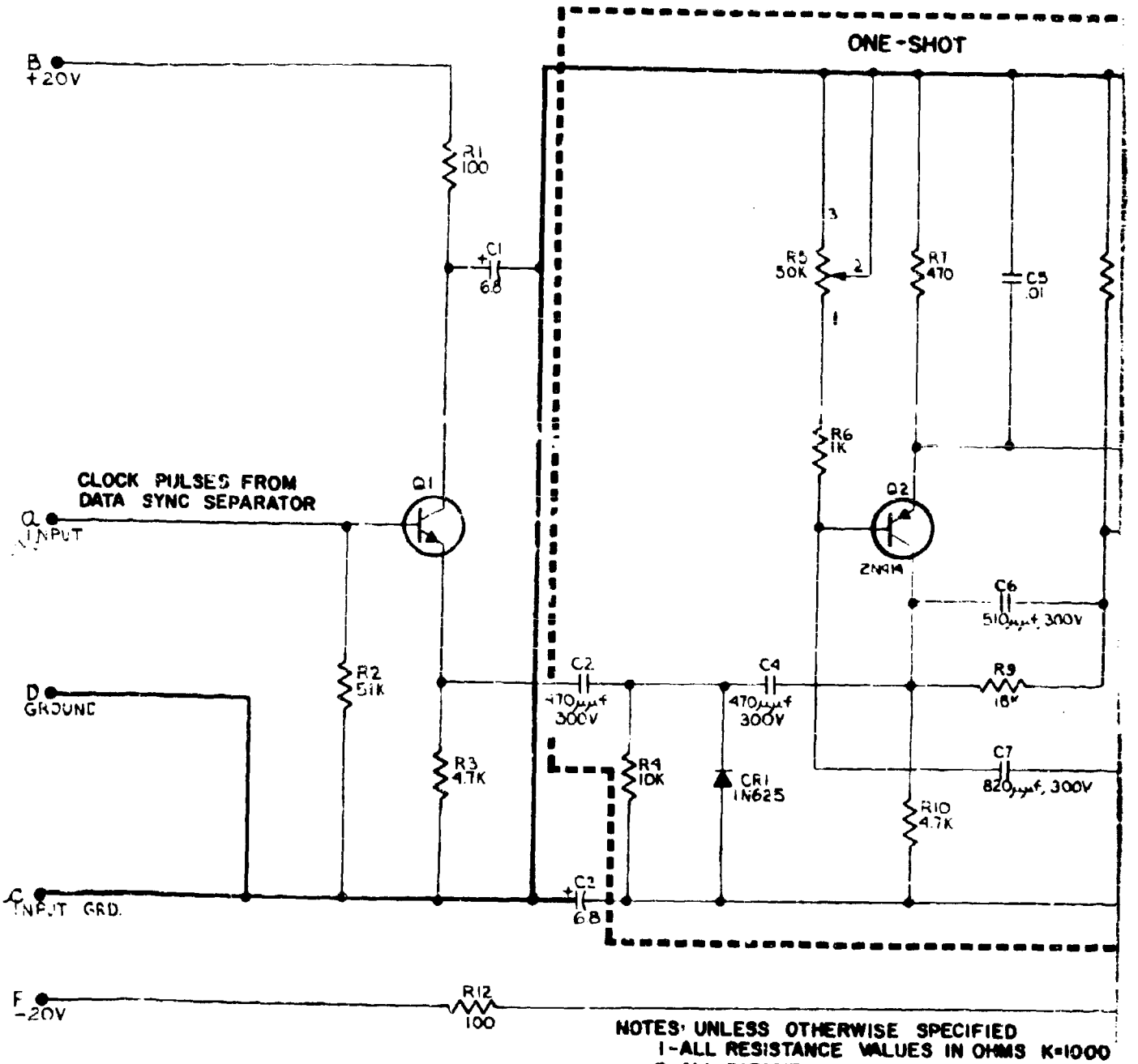
C
INPUT GRD.

F
-20V

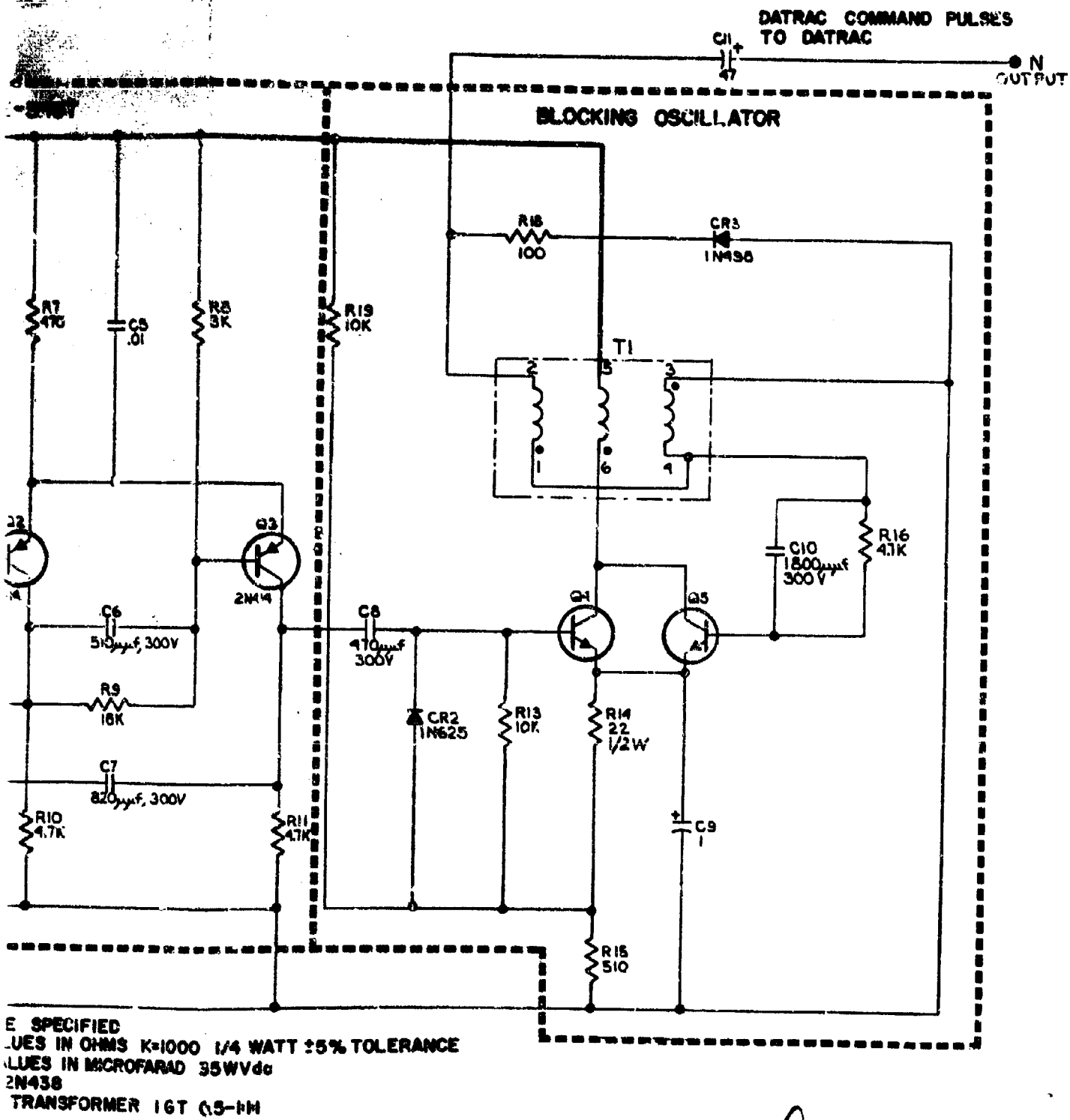
PARTS List

Reference Designation	Part No.	Vendor or MIL Spec.
C1, 3	[illegible]	Sprague Electric Co., North Adams, Mass.
C2, 4, 5	[illegible]	[illegible]
C6	[illegible]	[illegible]
C7	[illegible]	[illegible]
C9	[illegible]	[illegible]
C10	[illegible]	[illegible]
C11	[illegible]	[illegible]
CR1, 2	[illegible]	[illegible]
CR3	[illegible]	[illegible]
Q1, 4, 5	[illegible]	[illegible]
Q2, 3	[illegible]	[illegible]
R1, 13, 14	[illegible]	[illegible]
R2	[illegible]	[illegible]
R3, 9, 11	[illegible]	[illegible]
R4, 15, 16	[illegible]	[illegible]
R5	[illegible]	[illegible]
R6	[illegible]	[illegible]
R7	[illegible]	[illegible]
R8	[illegible]	[illegible]
R9	[illegible]	[illegible]
R10	[illegible]	[illegible]
R12	[illegible]	[illegible]
R17	[illegible]	[illegible]
R18	[illegible]	[illegible]
T1	[illegible]	[illegible]

Dashmm, Santa Monica, Calif.


ONE-SHOT
B
+20V
R1
100
C1
68
R5
50K
3
2
1
R7
470
C5
.01
R6
1K
Q2
2N918
CLOCK PULSES FROM
DATA SYNC SEPARATOR
A
INPUT
Q1
C6
510μμf, 300V
R2
51K
C2
470μμf
300V
C4
470μμf
300V
R9
18K
D
GROUND
R3
4.7K
R4
10K
CR1
1N625
C7
820μμf, 300V
R10
4.7K
C
INPUT GRD.
C3
68
F
-20V
R12
100
NOTES: UNLESS OTHERWISE SPECIFIED
1-ALL RESISTANCE VALUES IN OHMS K=1000
2-ALL CAPACITANCE VALUES IN MICROFARAD
3-ALL TRANSISTORS 2N438
4-TI GUDEMAN PULSE TRANSFORMER 1GT

B

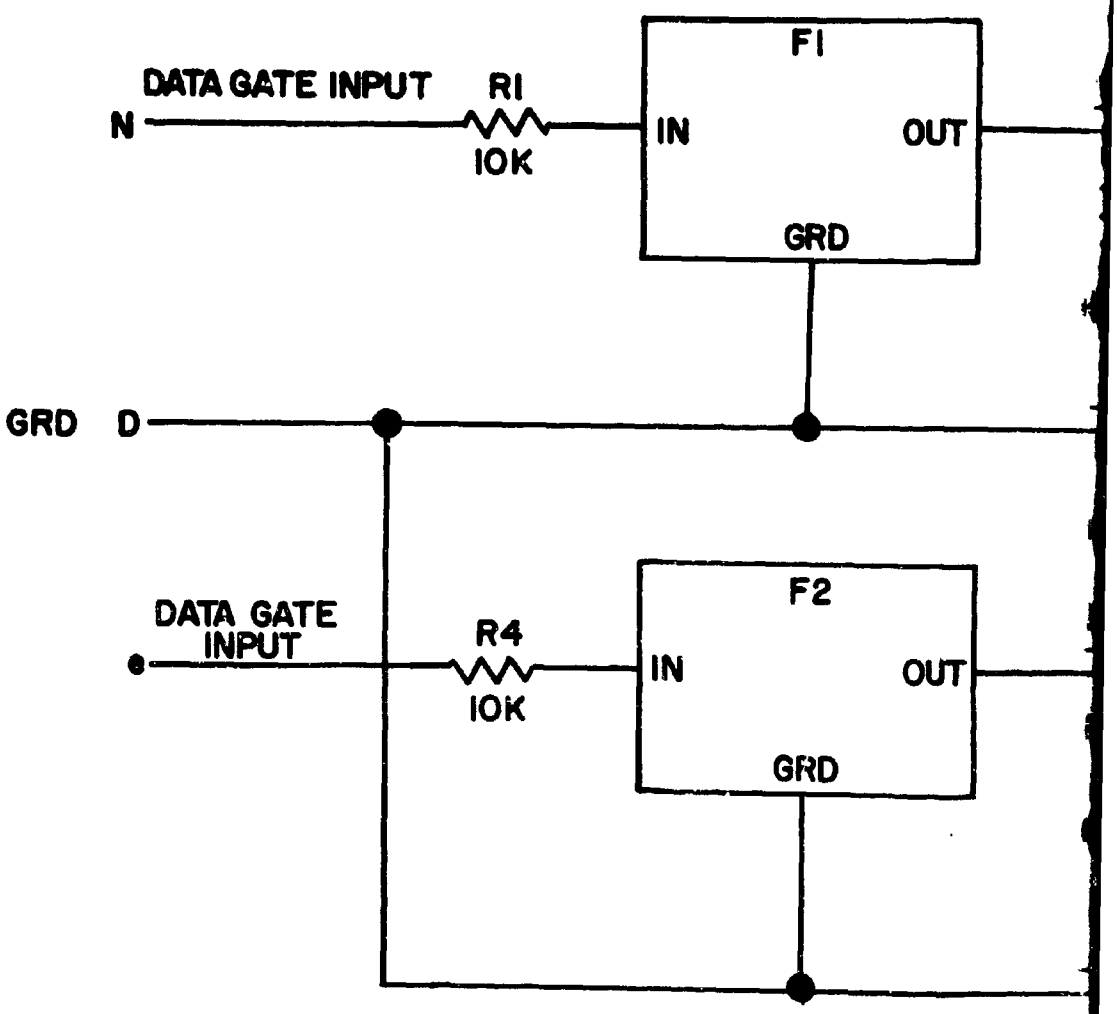


C

Fig. A-18 Data Sync Delay Record, Vibration

PARTS LIST

Reference Designation	Part No.	Vendor or MIL Spec
R1, 4	RC07GF103J (1/4 W, 5%)	MIL-R-11
R2, 5	RC07GF822J (1/4 W, 5%)	MIL-R-11
R3, 6	RC07GF122J (1/4 W, 5%)	MIL-R-11
F1, 2:		
0.250 kc board	FM04-1024	Ferro-Magnetics Co., Palo Alto, Calif.
1 kc board	FM04-1028	Ferro-Magnetics Co., Palo Alto, Calif.
2 kc board	FM04-1029	Ferro-Magnetics Co., Palo Alto, Calif.


F1
DATA GATE INPUT
R1
N
IOK
IN
OUT
GRD
GRD
D
F2
DATA GATE
INPUT
R4
IOK
IN
OUT
GRD

B

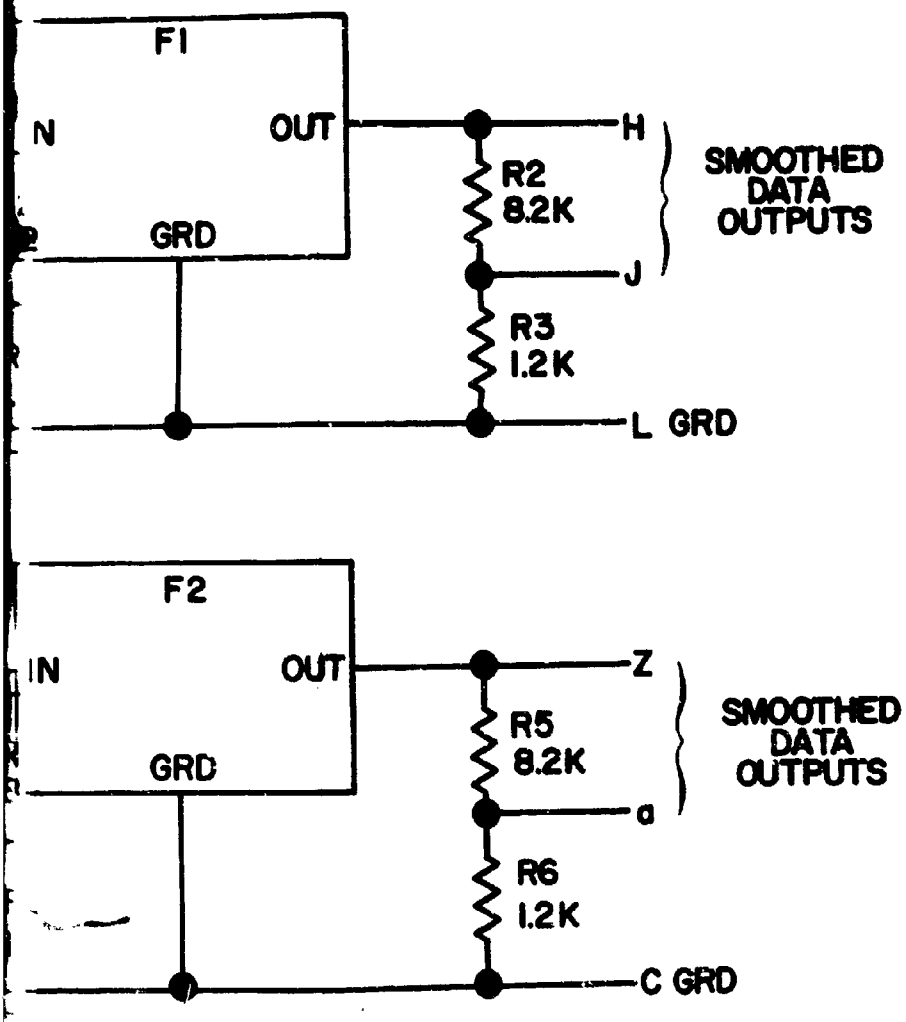


Fig. A-19 Filter Board

PARTS LIST

Reference Designation	Part No.	Vendor
C1, 2, 4, 6, 9 thru 15	DM15	El Menco, Los Angeles, Calif.
C3, 5, 7, 8	P123ZP	Aerovox Corp., New Bedford, Mass.
V1, 10	6414 5 Star	G. E. Owensboro, Ky.
V2, 7, 8, 11, 12	5965 5 Star	G. E. Owensboro, Ky.
V3	6350 5 Star	G. E. Owensboro, Ky.
V4, 5, 9	5726 5 Star	G. E. Owensboro, Ky.
V6	5687 5 Star	G. E. Owensboro, Ky.
R1, 2	R100POKAE	Epsco, Boston, Mass.
R3	6336-15	Epsco, Boston, Mass.
R4	R500POKAE	Epsco, Boston, Mass.
R5, 11, 12, 13, 18, 22, 25, 27 thru 31, 40, 42, 44, 46, 55, 64 thru 67	RC20GF	Allen-Bradley, Milwaukee, Wisc.
R6	R7P50KCFL	Epsco, Boston, Mass.
R7, 60	RV2NAXSD252A	Chicago Telephone Supply, Elkhart, Ind.
R8, 9, 41, 45	CP-1	Aerovox Corp., New Bedford, Mass.
R10, 15, 43, 56	NA30	Continental-Wirt, Phila., Penna.
R14, 20, 21, 49, 52	NA25	Continental-Wirt, Phila., Penna.
R16, 17	NA20	Continental-Wirt, Phila., Penna.
R19, 32, 33, 38, 39	RS10	Dale Products, Inc., Columbus, Nebr.
R23, 26	RC42GF	Allen-Bradley, Milwaukee, Wisc.
R24	SS10W	Sage Electronics Corp., Rochester, N. Y.
R34 thru 37	DCSH$\frac{1}{2}$	Dale Products, Columbus, Nebr.
R47, 48, 50, 51, 53, 54	NA15	Continental-Wirt, Phila., Penna.
R57	611-T1	Epsco, Boston, Mass.
R58	6336-2	Epsco, Boston, Mass.
R59	611-B3	Epsco, Boston, Mass.
R61	R15P00KCEL	Epsco, Boston, Mass.
R63	R2500L	Mallory & Co., Inc., Indianapolis, Ind.
T1, 2	PE2225	Pulse Engineering, Santa Clara, Calif.

les, Calif.
Bedford,

aukee, Wisc.
upply, Elkhart,

Bedford,

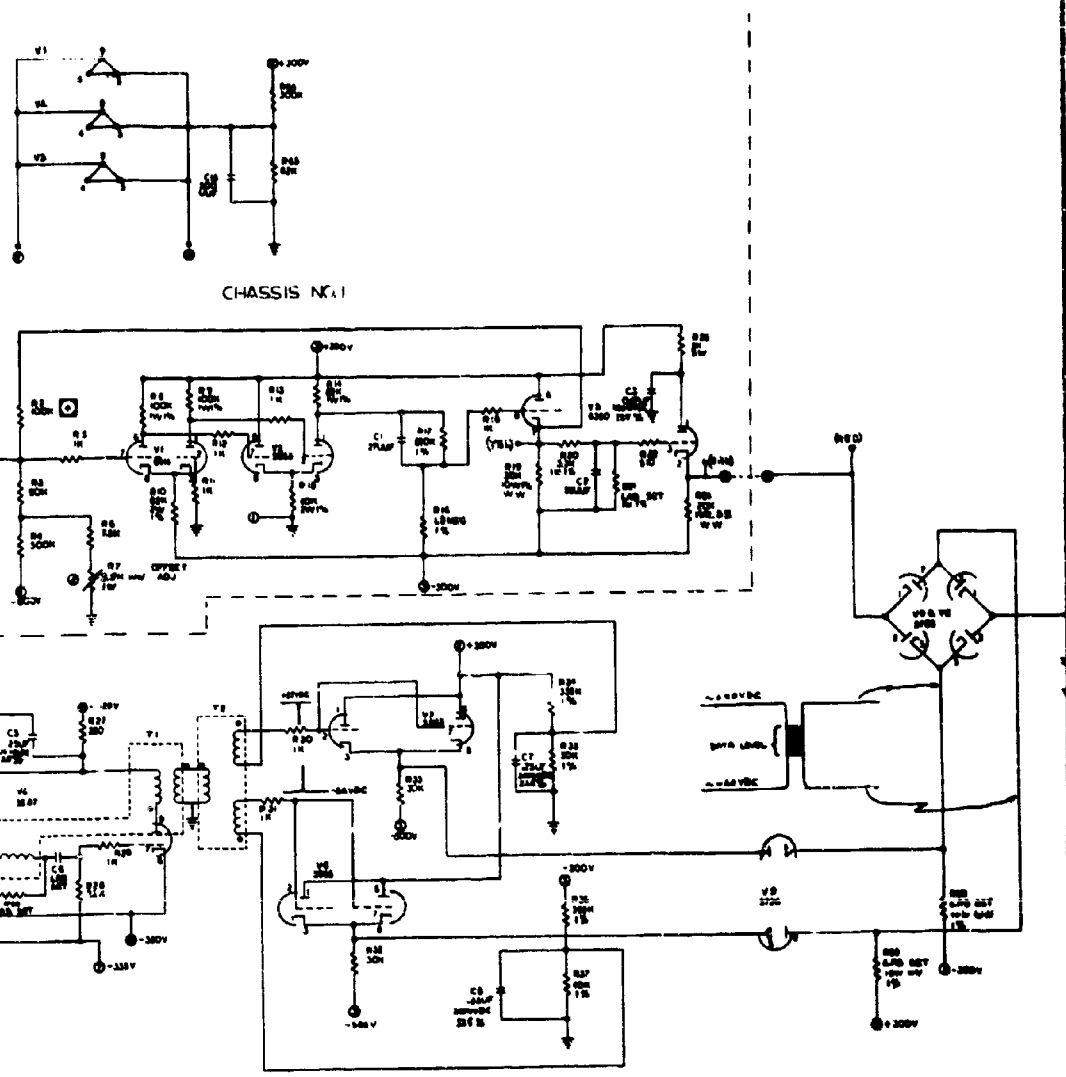
nila., Penna.
nila., Penna.
nila., Penna.
Columbus,

aukee, Wisc.
p., Rochester,

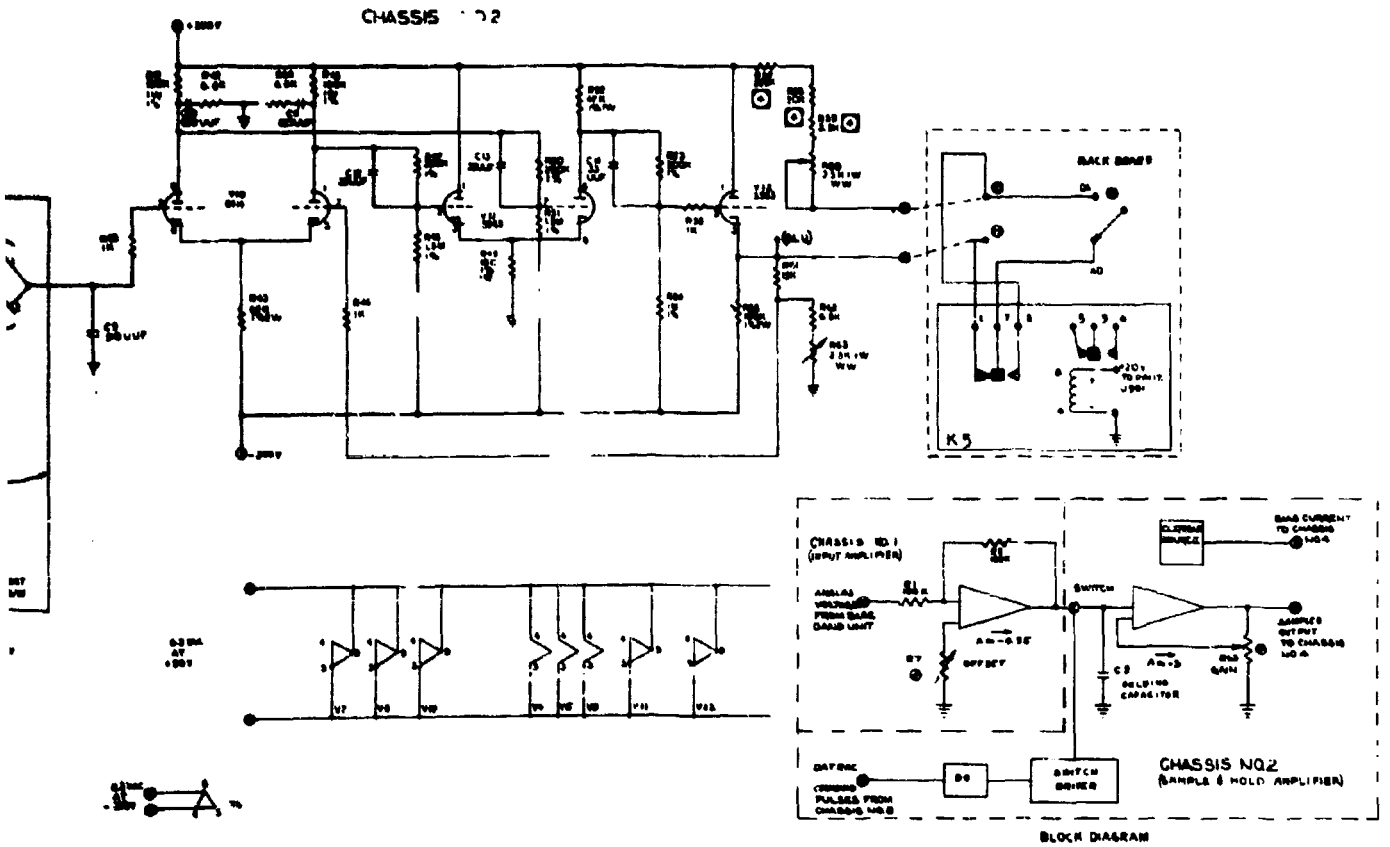
mbus, Nebr.
nila., Penna.

Indianapolis,

nta Clara,

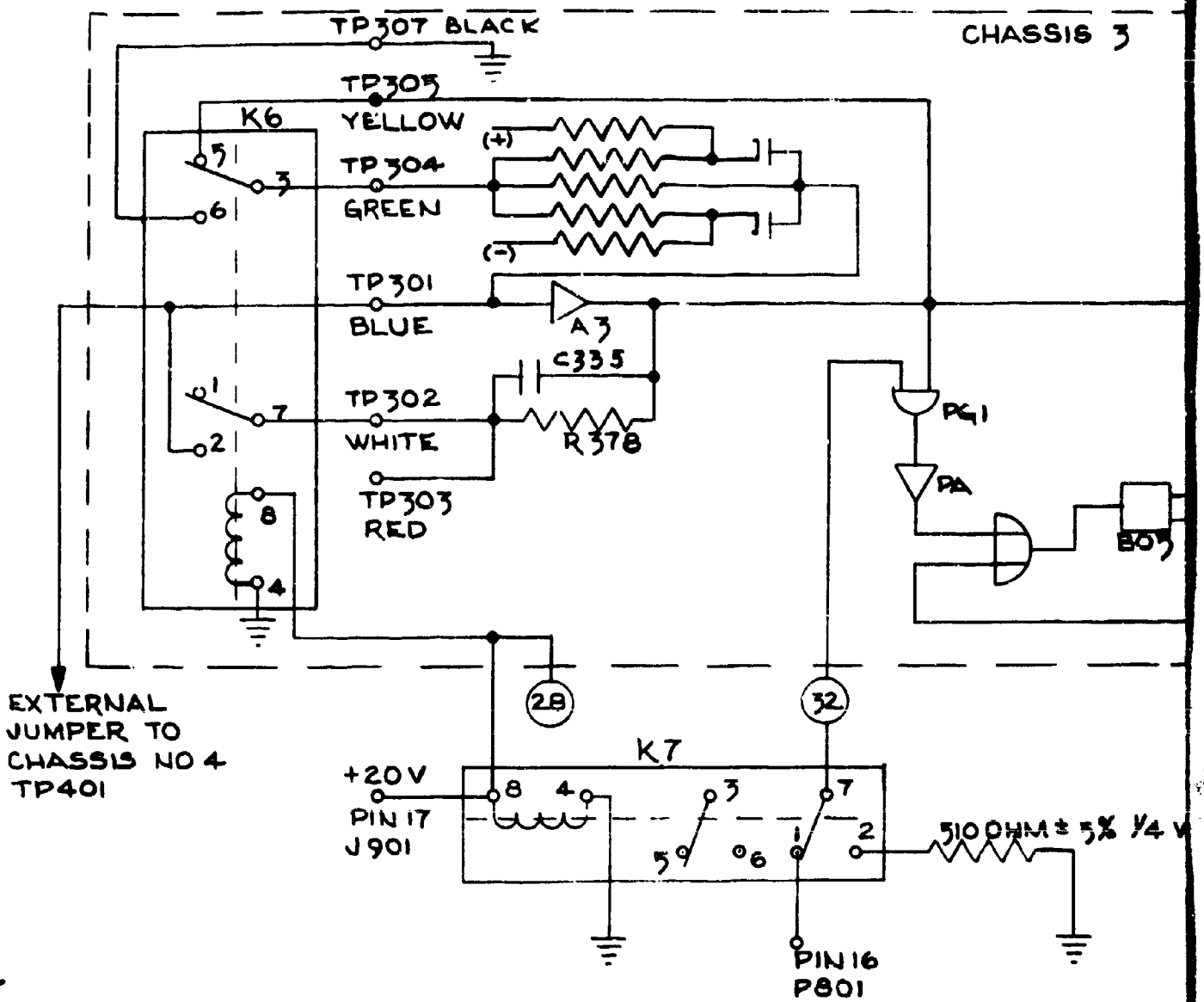


B



NOTES UNLESS OTHERWISE SPECIFIED

Fig. A-20 Datrac Modifications - Chassis One and Two



3- REFER TO DWG R-34815 FOR ASSY- DAT
MODIFICATIONS - CHASSIS NO 3

2- R378 TO CONSIST OF A PAIR OF DALOHM D
±1% RESISTORS IN PARALLEL

1- REFER TO FIG 5.5 COMPARATOR SCHEMA
OF DATRAC MANUAL FOR EXPLANATION
NUMBER & COLOR CODING

NOTES:

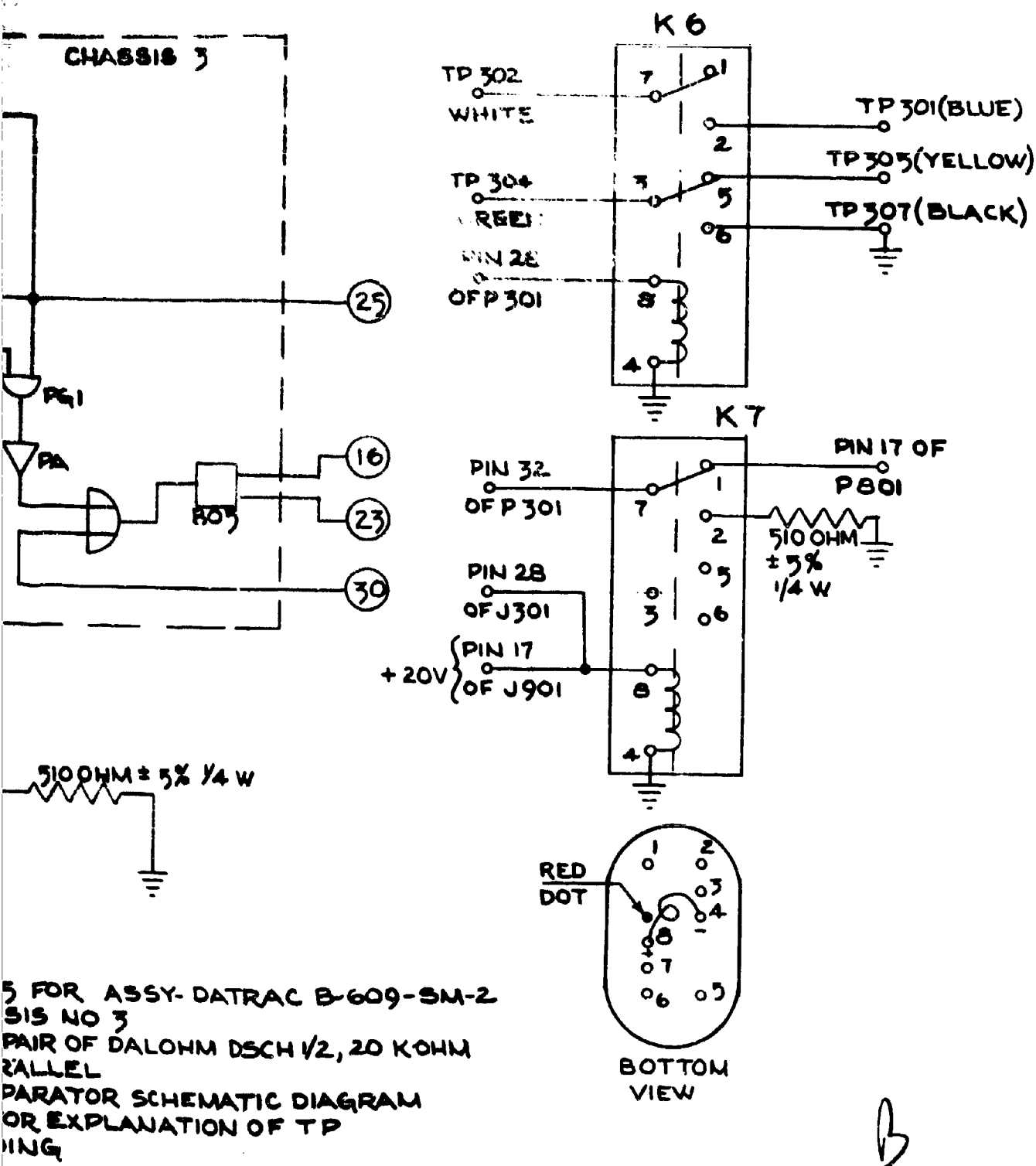
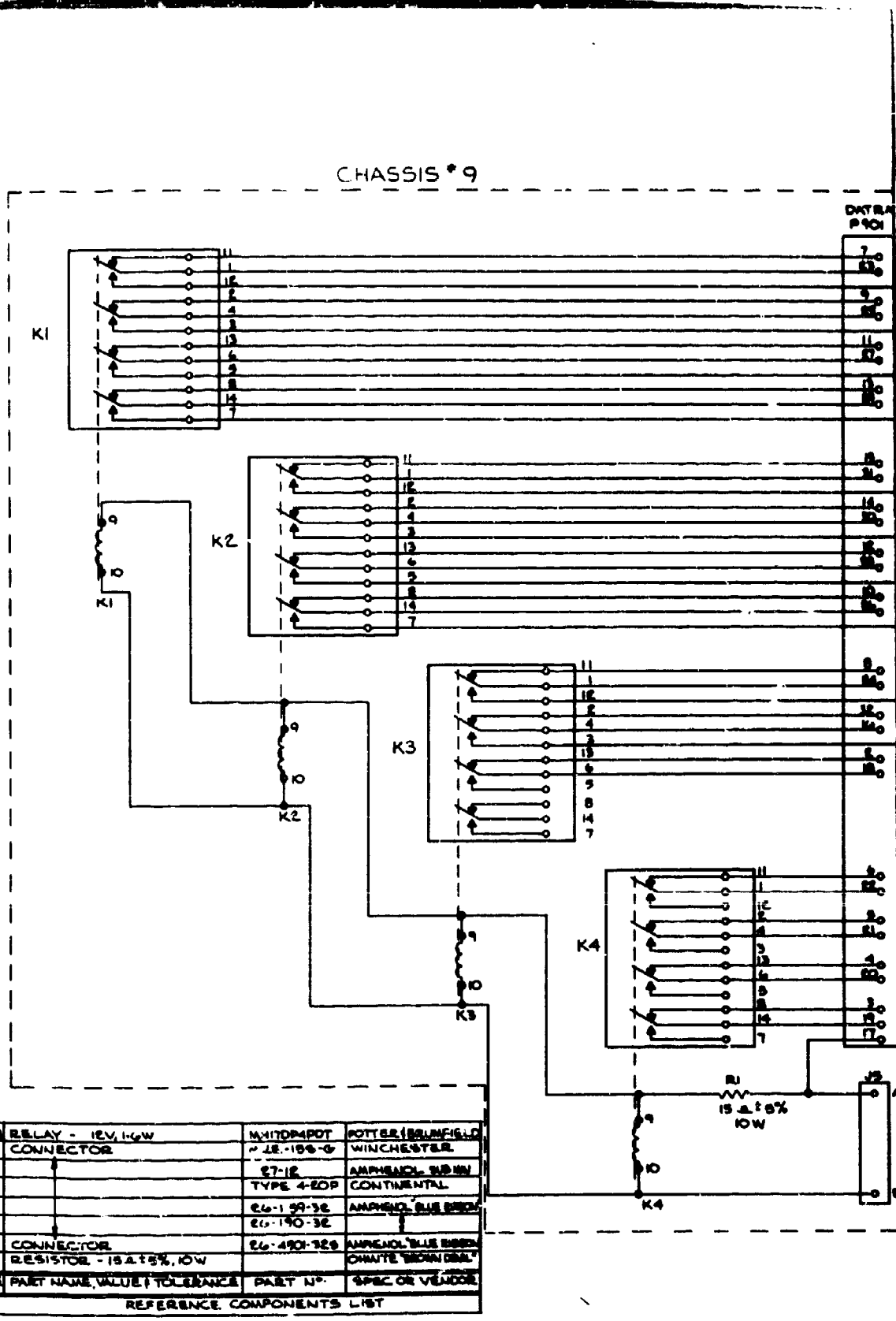


Fig. A-21 Datrac Modifications - Chassis Three



REF DES	PART NAME, VALUE, TOLERANCE	PART Nº	SPEC OR VENDOR
K1	RELAY - 12V, 1.6W	MKIITDP4POT	POTTER & BRUMFIELD
J7	CONNECTOR	~ 2E-156-G	WINCHESTER
J8	↓	87-12	AMPHENOL SUB MIN
J5	↓	TYPE 4-EDP	CONTINENTAL
P501	↓	86-1 98-32	AMPHENOL BLUE RIBBON
J401	↓	86-190-32	↓
J1501	CONNECTOR	86-4901-329	AMPHENOL BLUE RIBBON
R1	RESISTOR - 15Ω ±5%, 10W		OHMITE "BROWN DEAL"

REFERENCE COMPONENTS LIST

A

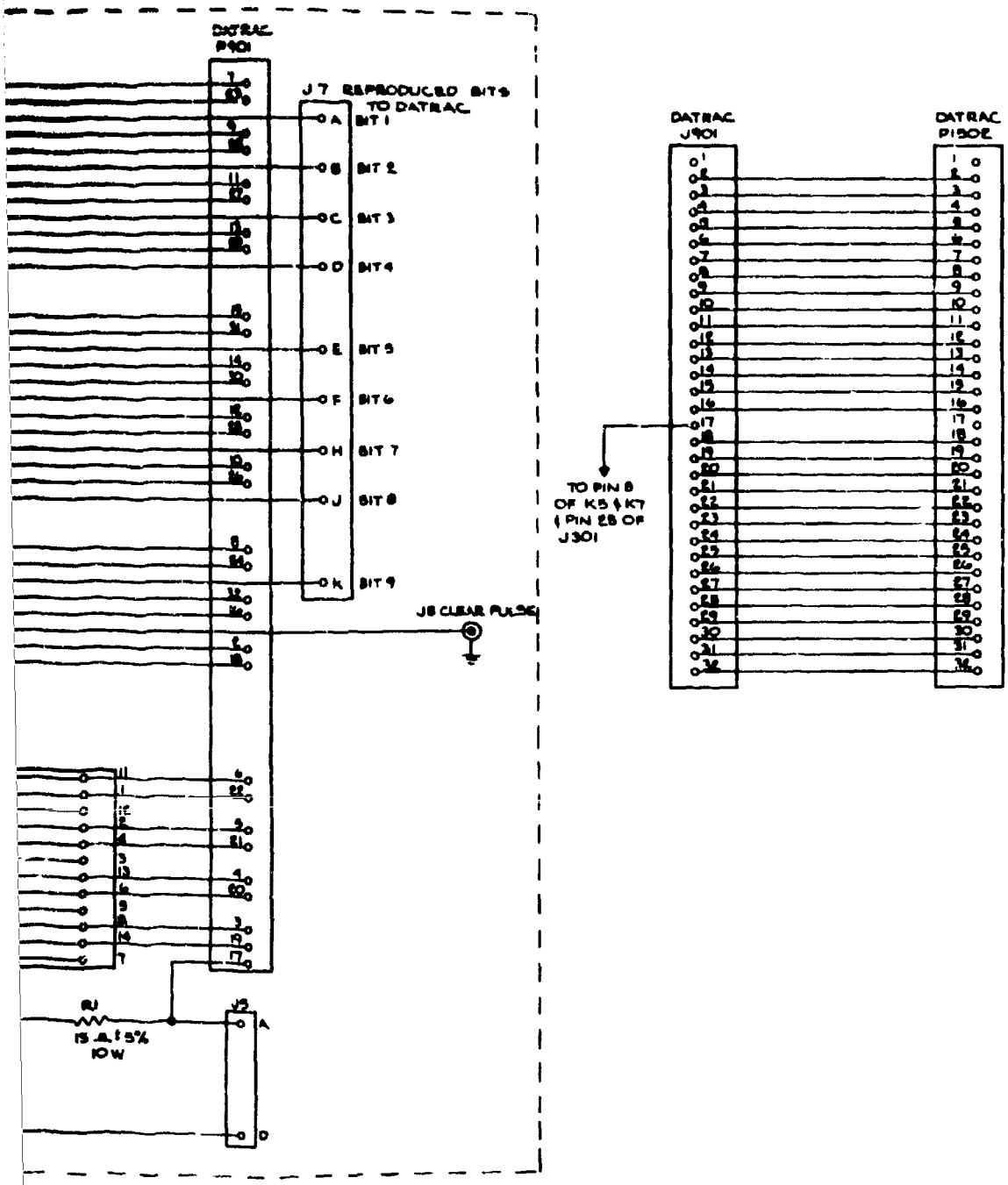
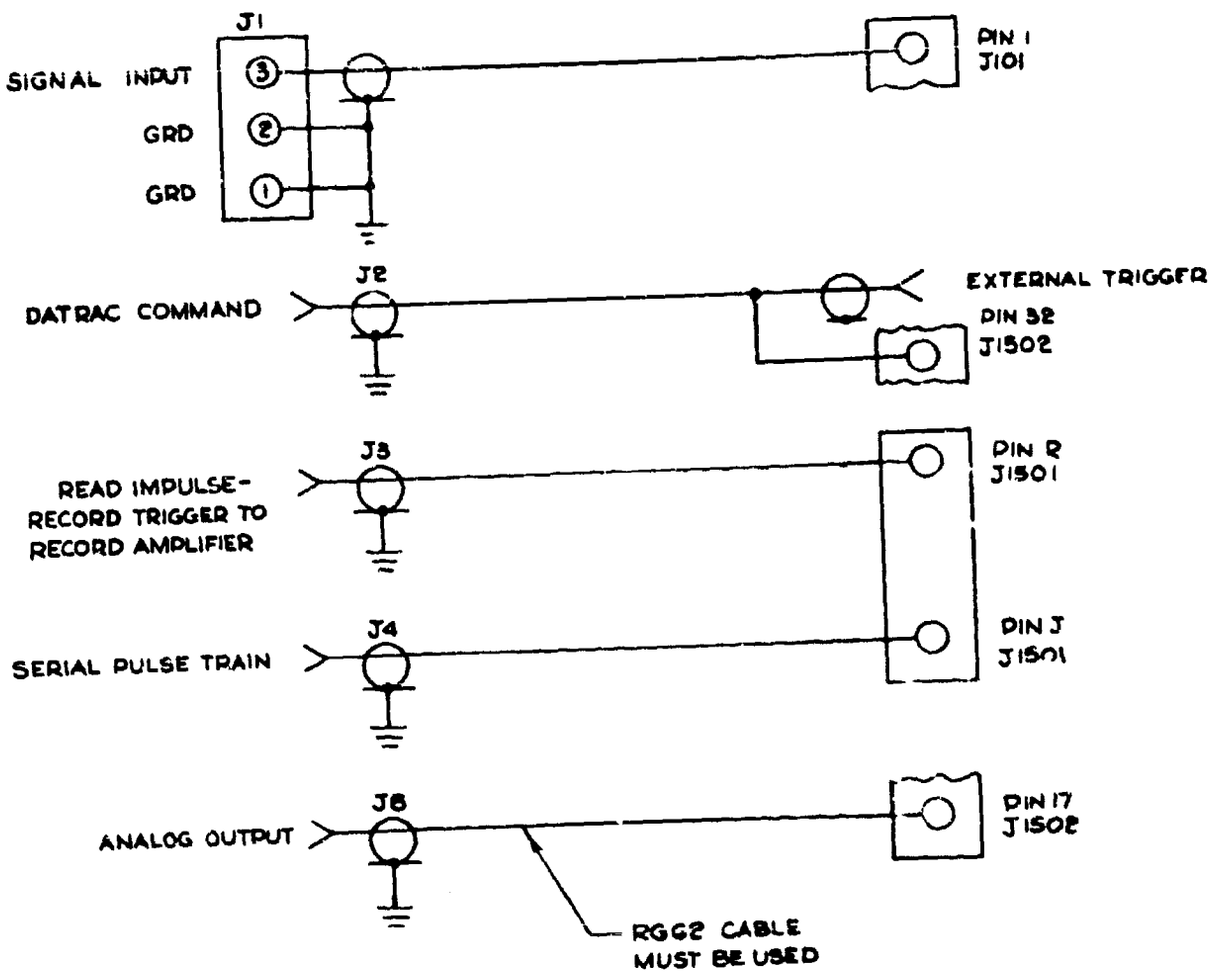
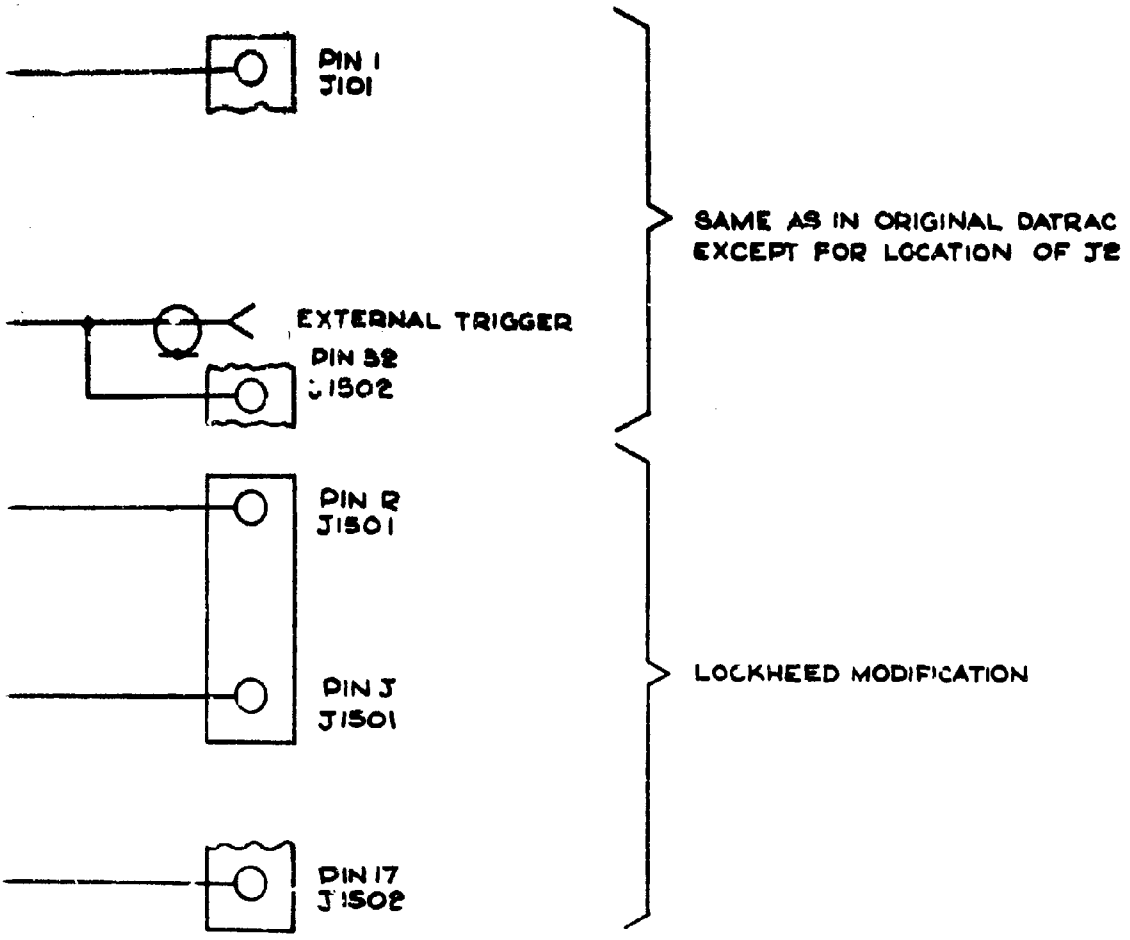


Fig. A-22 Datrac Modifications - Chassis Nine



REFERENCE COMPONENTS LIST			
REF DES	PART NAME VALUE & TOLERANCE	PART NO	SPEC OR VENDOR
J1	RECEPTACLE	91-855	AMPHENOL CHICAGO, ILL.
J2, J3 J4 & J6	RECEPTACLE	UGG57-U	

A

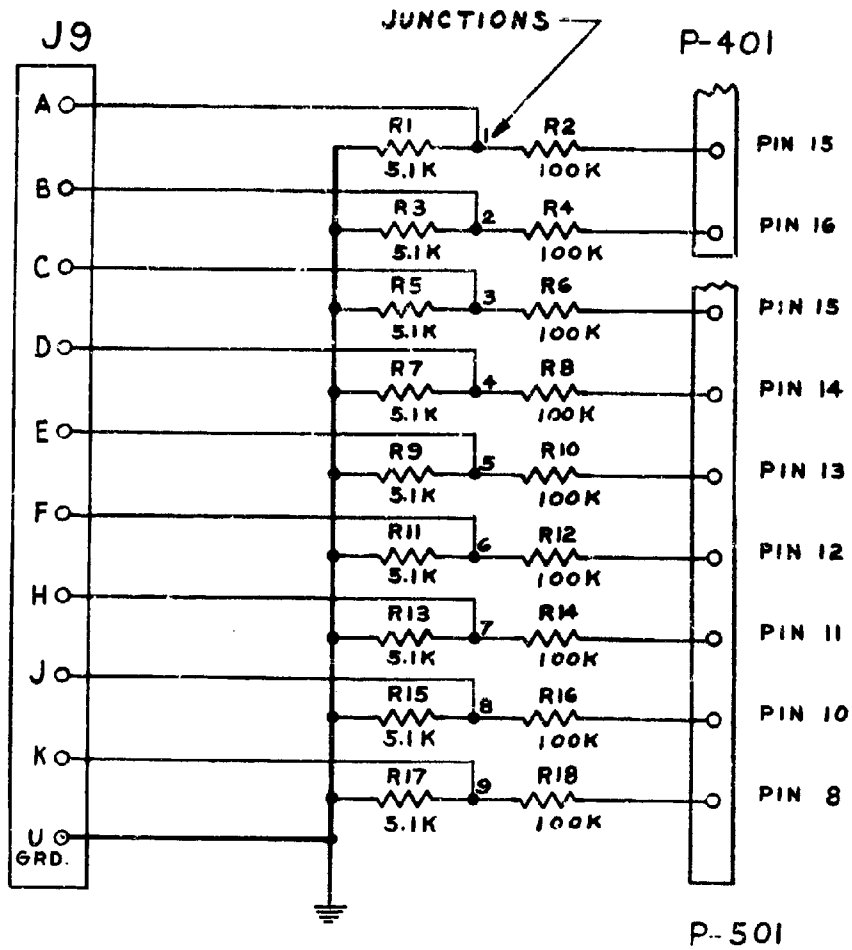


? CABLE
BE USED

SPEC OR VENDOR
AMPHENOL CHICAGO, ILL.

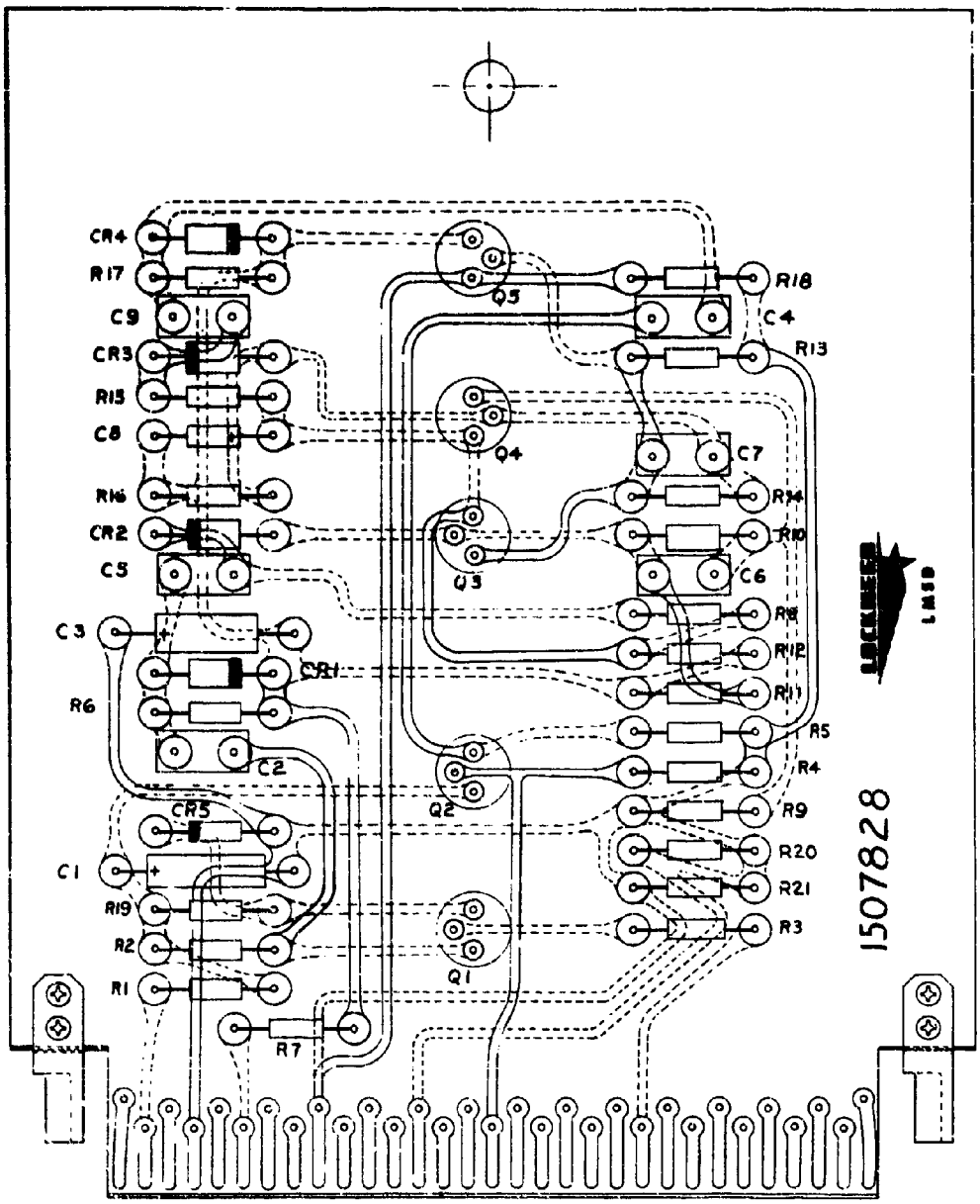
b

Fig. A-23 Dairac External Modifications



REFERENCE COMPONENTS LIST			
REF. DES.	PART NAME, VALUE & TOLERANCE	PART NO.	SPEC. OR VENDOR
R1, 3, 5, 7, 9, 11, 13, 15, & 17	RESISTOR, COMP. ¼ WATT ± 5%	RC07GF512J	MIL-R-11C
R2, 4, 6, 8, 10, 12, 14, 16, & 18	RESISTOR, COMP. ¼ WATT ± 5%	RC07GF104J	MIL-R-11C
J9	RECEPTACLE	MRE-18S-G	WINCHESTER

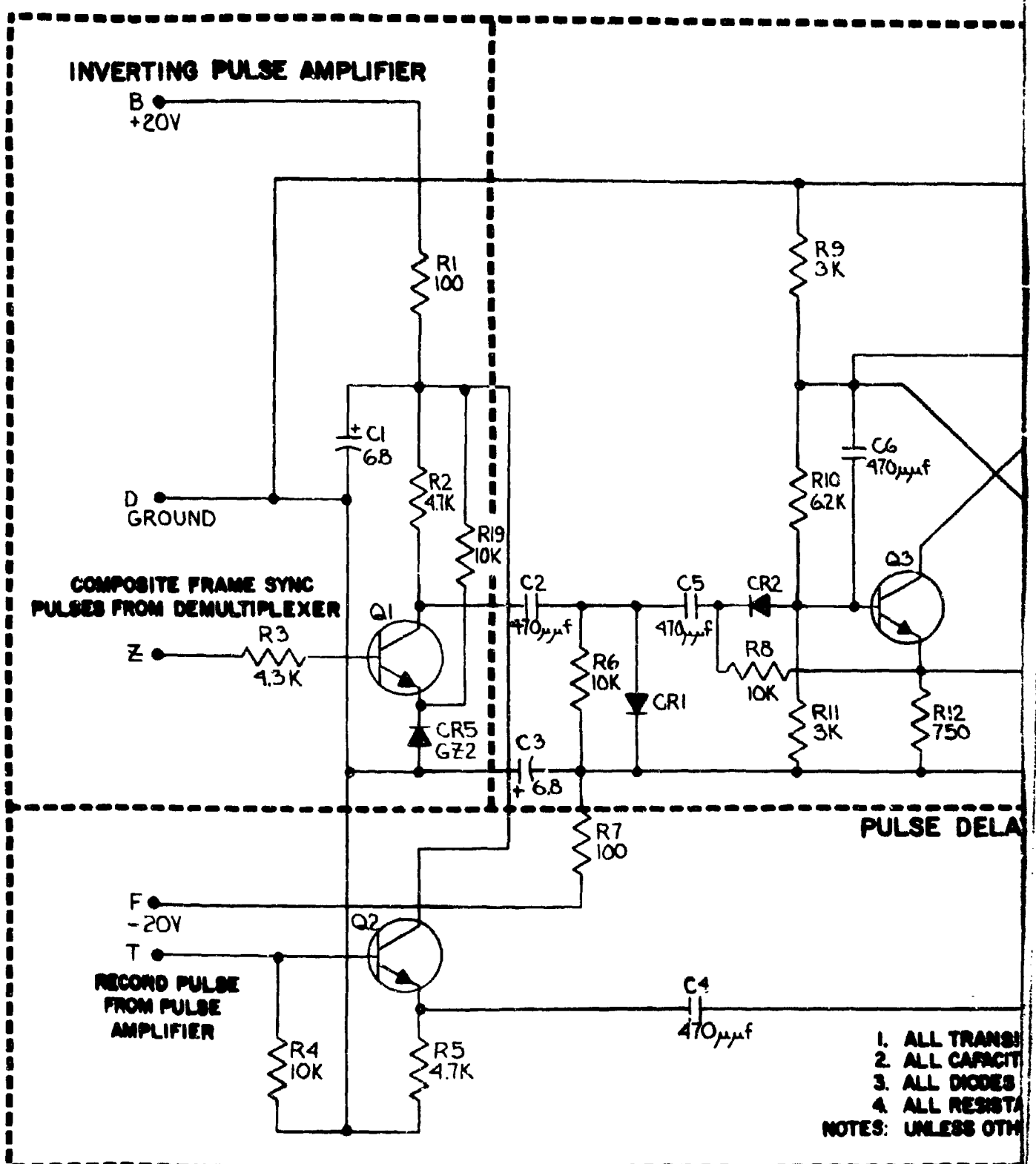
Fig. A-24 Datrac Modifications - Record Outputs and Output Signal Monitor Points



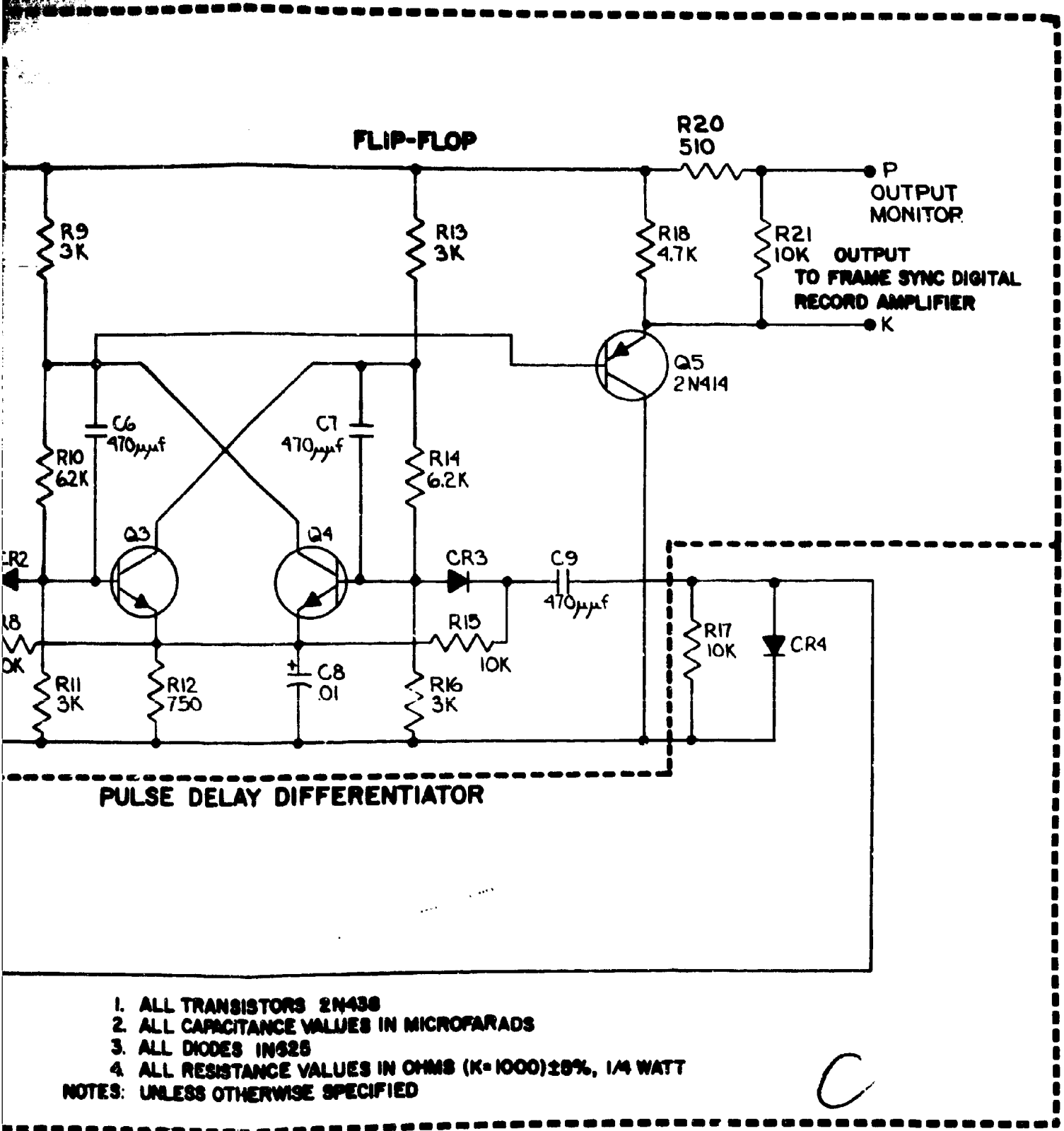
PARTS LIST

Reference Designation	Part No.	Vendor or MIL Spec.
C1, 3	110D681X9033B1	Sprague Electric Co., North Adams, Mass.
C2, 4 thru 7, 9	DM15F471J	El Menco, Los Angeles, Calif.
C8	110D103X9035A2	Sprague Electric Co., North Adams, Mass.
CR1 thru 4	1N645	Pacific Semiconductor, Culver City, Calif.
CR5	GX2	Hoffman Semiconductor, Evanston, Ill
Q1 thru 4	2N430	CBS Semiconductor, Los Angeles, Calif.
Q5	2N414	Raytheon, Newton, Mass.
R1, 7	RC07GF101J	MIL-R-11
R2, 5, 18	RC07GF471J	MIL-R-11
R3	RC07GF432J	MIL-R-11
R4, 6, 8, 13, 17, 19, 21	RC07GF103J	MIL-R-11
R9, 11, 13, 16	RC07GF331J	MIL-R-11
R10, 14	RC07GF822J	MIL-R-11
R12	RC07GF710J	MIL-M-11
R20	RC07GF511J	MIL-R-11

A


INVERTING PULSE AMPLIFIER
B
+20V
R1
100
R9
3K
C1
6.8
C6
470μμf
D
GROUND
R2
4.7K
R10
62K
R19
10K
COMPOSITE FRAME SYNC
PULSES FROM DEMULTIPLEXER
Q1
C2
470μμf
C5
470μμf
CR2
Q3
Z
R3
4.3K
R6
10K
CR1
R8
10K
CR5
GZ2
C3
6.8
R11
3K
R12
750
PULSE DELA
R7
100
F
-20V
T
Q2
RECORD PULSE
FROM PULSE
AMPLIFIER
C4
470μμf
R4
10K
R5
4.7K
1. ALL TRANSI
2. ALL CAPACIT
3. ALL DIODES
4. ALL RESISTA
NOTES: UNLESS OTH

B



NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL TRANSISTORS 2N438
2. ALL CAPACITANCE VALUES IN MICROFARADS
3. ALL DIODES IN625
4. ALL RESISTANCE VALUES IN OHMS (K=1000)±5%, 1/4 WATT

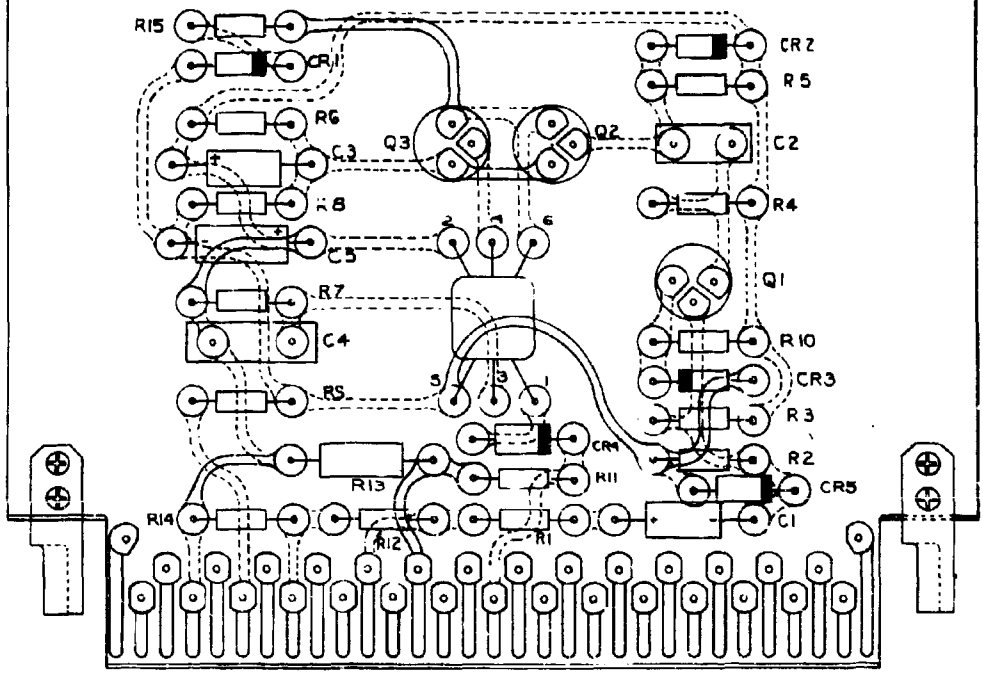
C

Fig. A-25 Frame Sync Storage Record

1501220

LOCKHEED

LMSD



PARTS LIST

Reference Designation	Part No.	Vendor or Mfg. Spec.
C1	[illegible]	Sprague Elec. Co., North Adams, Mass.
C2	[illegible]	El Monte, Los Angeles, Calif.
C3	[illegible]	Sprague Elec. Co., North Adams, Mass.
C4	[illegible]	El Monte, Los Angeles, Calif.
C5	[illegible]	Sprague Elec. Co., North Adams, Mass.
CR1, 6	1N538	CBS-Hytron, Electronic, Mass.
CR2, 5	1N888	Pacific Semiconductor, Culver City, Cal.
CR3	IP3	Transitron, Wakefield, Mass.
CR4	1N538	CBS-Hytron, Danvers, Mass.
CR7, 8	1N914	Raytheon, Newton, Mass.
R1	RCR07G[illegible]JS	RESL-0-11
R2, 3, 4, 10, 13	RCR07G[illegible]GS	RESL-0-11
R5	RCR07G[illegible]GS	RESL-0-11
R6, 14	RCR07G[illegible]GS	RESL-0-11
R7	RCR07G[illegible]GS	RESL-0-11
R8	RCR07G[illegible]FS	RESL-0-11
R9	RCR07G[illegible]FS	RESL-0-11
R11	RCR07G[illegible]FS	RESL-0-11
R12	RCR07G[illegible]FS	RESL-0-11
R15	RCR07G[illegible]JS	RESL-0-11
R16	RCR07G[illegible]JS	RESL-0-11
T1	10T 88-1(1-)	Globetek, Reds Meadow, Calif.

F
-20V

INV

RECORD PU
RECORD A

T
OUT PUT

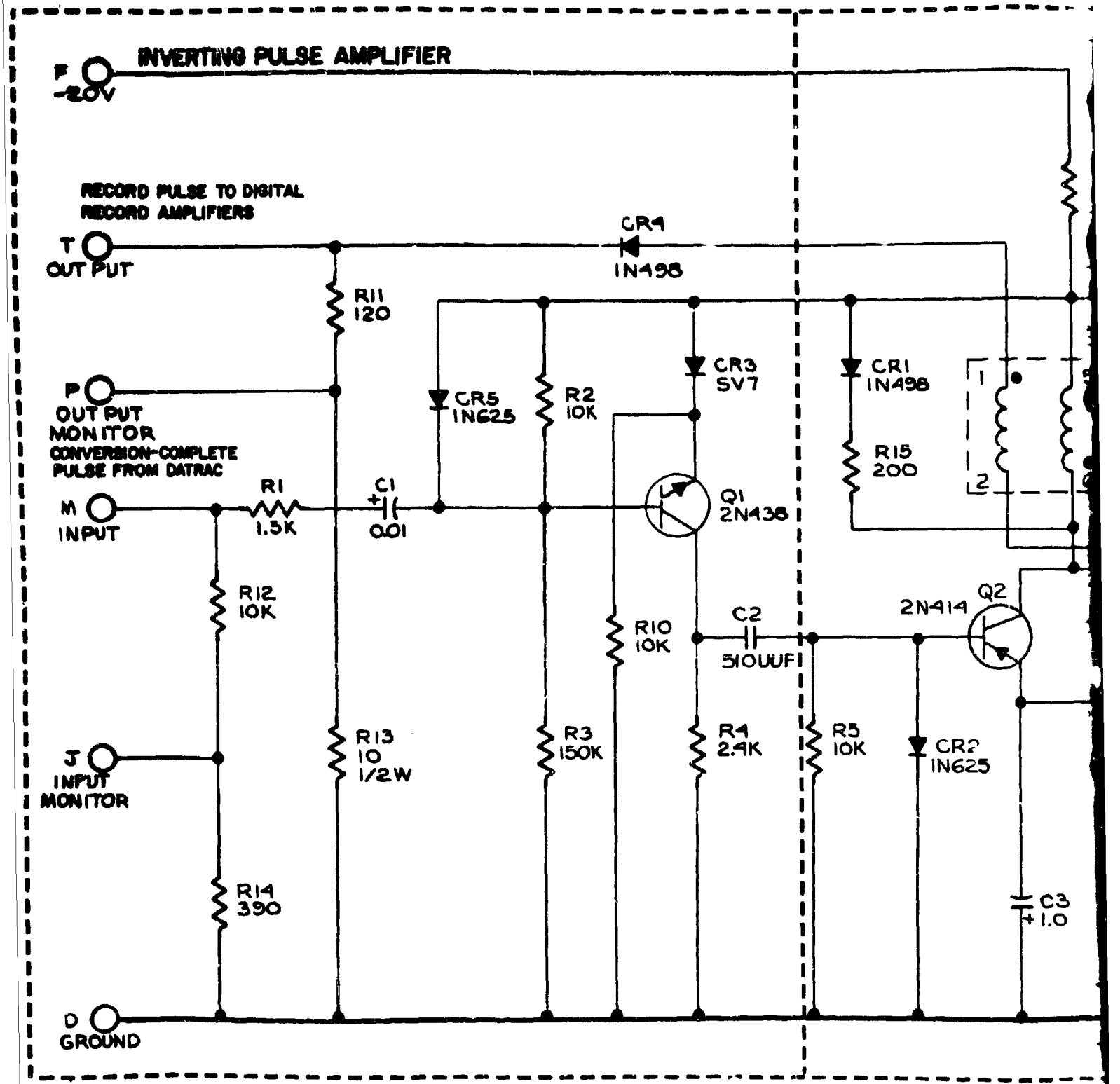
P
OUT PUT
MONITOR
CONVERSION-CO
PULSE FROM D

M
INPUT

J
INPUT
MONITOR

D
GF JUND

A


INVERTING PULSE AMPLIFIER
F
-20V
RECORD PULSE TO DIGITAL
RECORD AMPLIFIERS
T
OUT PUT
CR4
IN498
R11
120
P
OUT PUT
MONITOR
CONVERSION-COMPLETE
PULSE FROM DATRAC
CR5
IN625
R2
10K
CR3
SV7
CR1
IN498
R15
200
1
2
M
INPUT
R1
1.5K
C1
0.01
Q1
2N438
R12
10K
R10
10K
C2
510UUF
2N414
Q2
J
INPUT
MONITOR
R13
10
1/2W
R3
150K
R4
2.4K
R5
10K
CR2
IN625
R14
390
C3
+1.0
D
GROUND

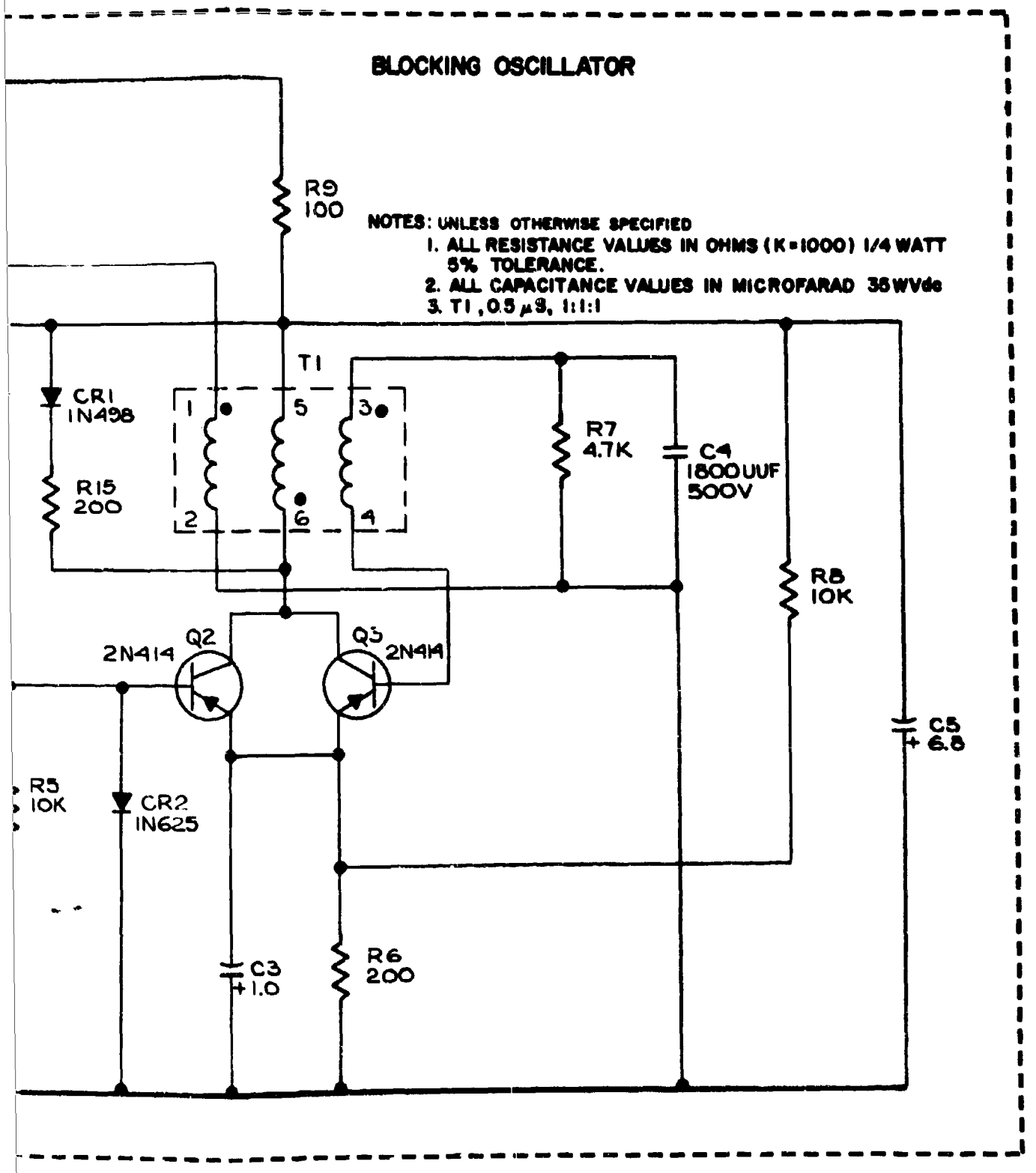
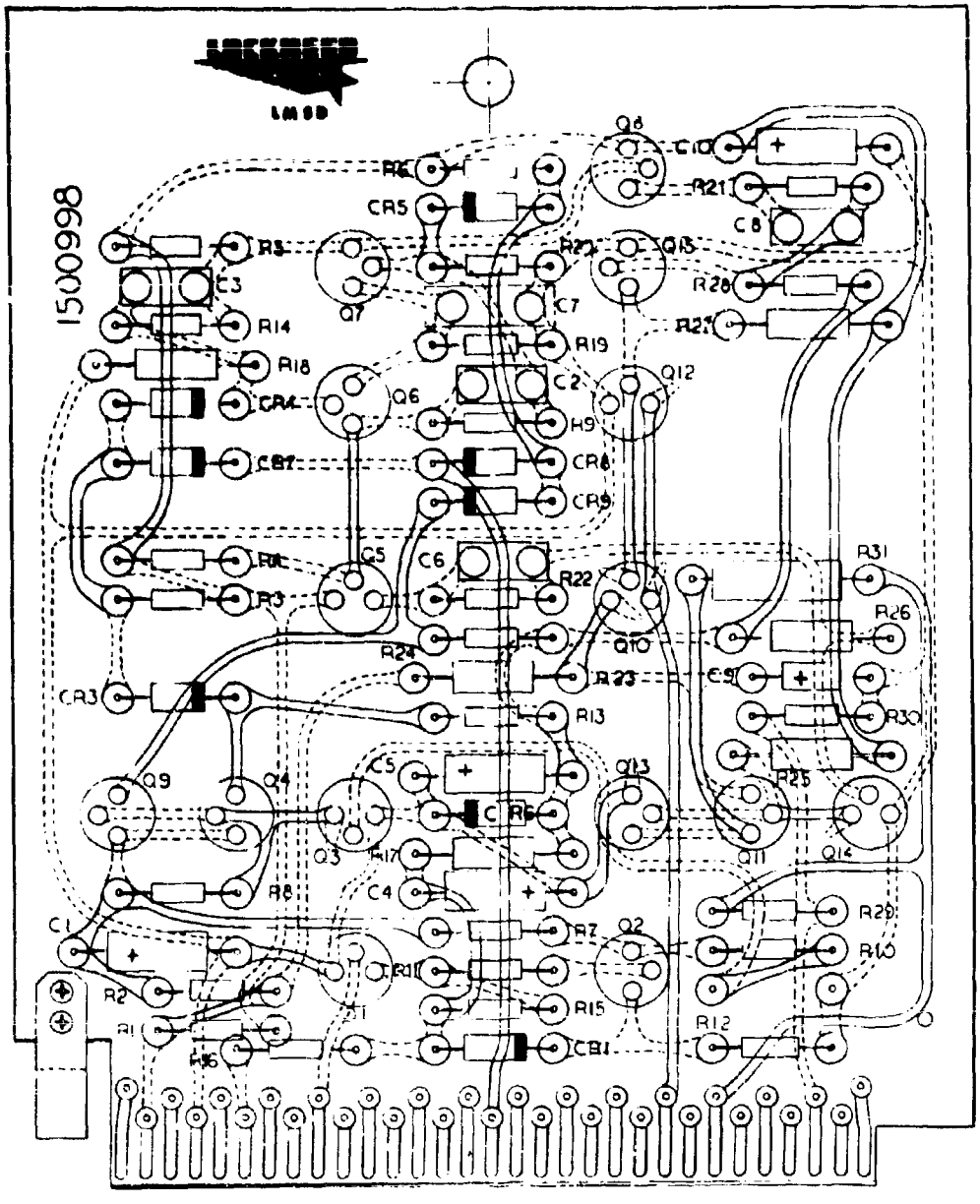
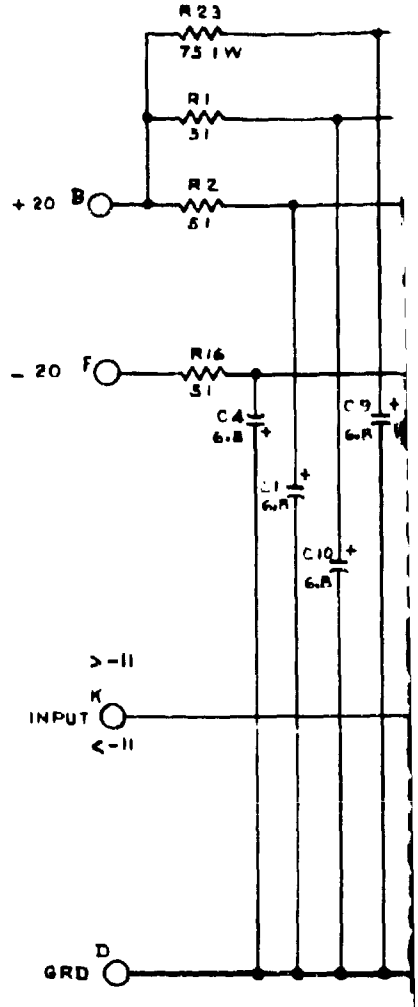
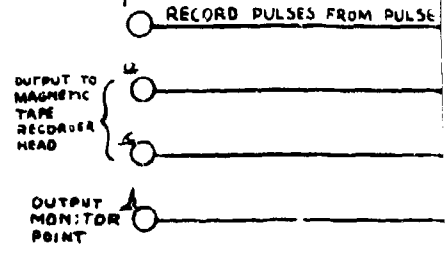


Fig. A-26 Pulse Amplifier







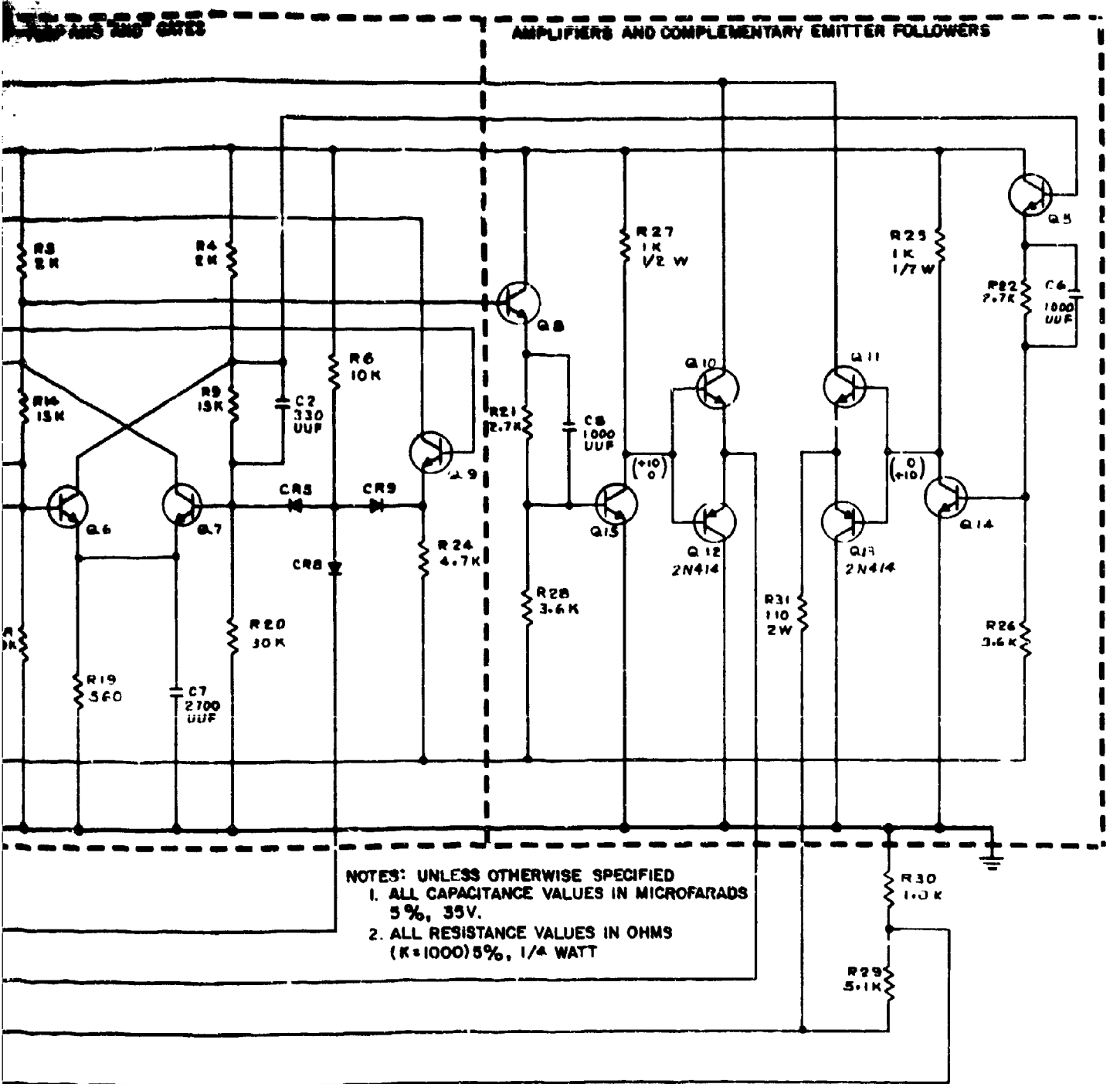
PARTS LIST

Reference Designation	Part No.	Vendor or MIL Spec.
C1, 4, 5, 9, 10	150D686X9035B1	Sprague Electric Co., North Adams, Mass.
C3	DM15F331J	El Menco, Los Angeles, Calif.
C6, 8	DM15F100J	El Menco, Los Angeles, Calif.
C7	DM15F5R1J	El Menco, Los Angeles, Calif.
CR1	SV9	Transitron, Wakefield, Mass.
CR2, 3, 4, 5, 7, 8, 9	1N456	Pacific Semiconductor, Culver City, Calif.
CR6	SV7	Transitron, Wakefield, Mass.
Q1, 2, 4 thru 11, 14, 15	2N638	CBS-Hytron, Danvers, Mass.
Q3, 12, 13	2N614	Raytheon, Newton, Mass.
R1, 2, 16	RC07GF510J	MIL-R-11
R3, 6, 10, 11	RC07GF150J	MIL-R-11
R4, 5	RC07GF750J	MIL-R-11
R7	RC07GF560J	MIL-R-11
R8	RC07GF220J	MIL-R-11
R9, 12, 14	RC07GF153J	MIL-R-11
R13, 24	RC07GF473J	MIL-R-11
R18	RC07GF333J	MIL-R-11
R17, 25, 27	RC20GF103J	MIL-R-11
R18, 20	RC07GF304J	MIL-R-11
R19	RC07GF561J	MIL-R-11
R21, 22	RC07GF271J	MIL-R-11
R23	M8356A4-T4	MIL-R-11
R26, 28	RC07GF364J	MIL-R-11
R29	RC07GF512J	MIL-R-11
R30	RC07GF102J	MIL-R-11
R31	M8356A6-04	MIL-R-11

A

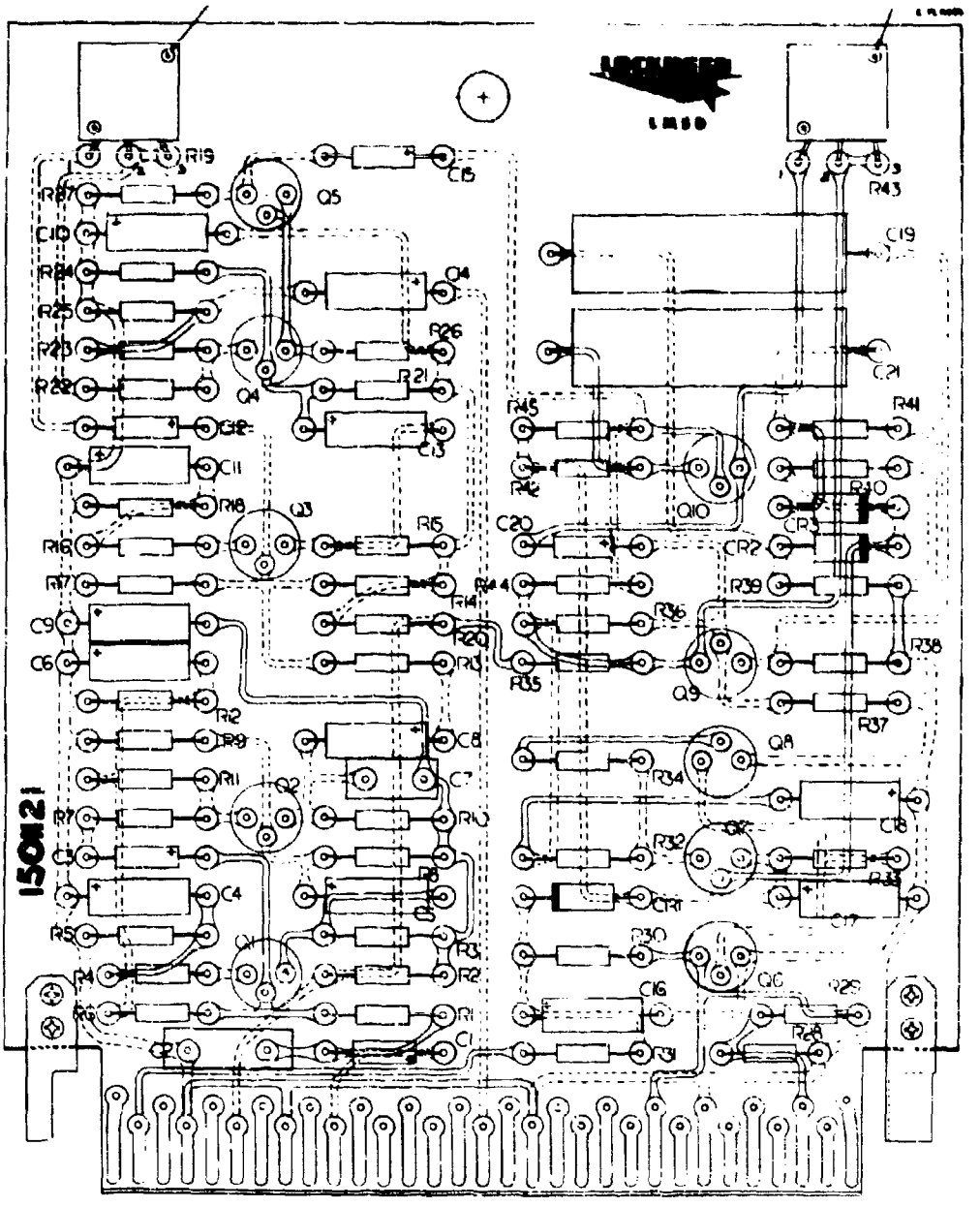
INVERTING PULSE AMPLIFIER
FLIP-FLOP AND "AND" GATES
R23 75 1W
R1 51
R2 51
+20 B
-20 F
R16 51
C4 6.8
C9 6.8
C1 6.8
C10 6.8
R15 3.3K
R7 6.8K
CR1 5V9
R8 2.2K
R17 1K 1/2W
+20
Q4
R3 10K
C3 330 UUF
R14 15K
R5 2K
R10 10K +20
Q3 2N414
ON
OFF
R11 10K
Q2
Q1
>-11
K
INPUT
<-11
-11
R12 15K
CR6 5V7
C5 6.8
R13 4.7K
-7
CR3
CR4
Q6
CR7
R18 30K
R19 560
C7 270 UUF
D
GRD
T
RECORD PULSES FROM PULSE AMPLIFIER
OUTPUT TO MAGNETIC TAPE RECORDER HEAD
OUTPUT MONITOR POINT

B



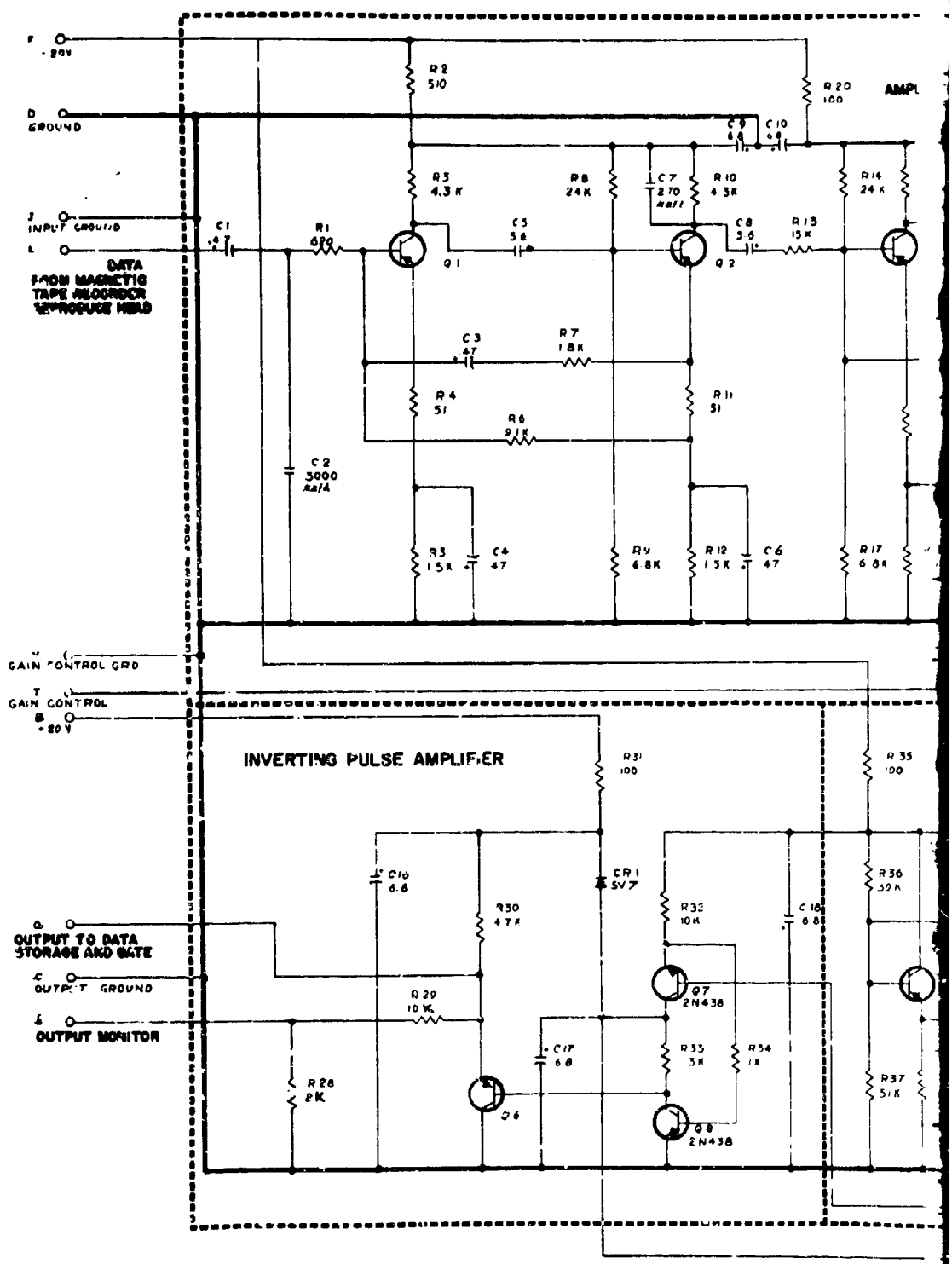
C

Fig. A-27 Digital Record Amplifier



PARTS LIST

Reference Designation	Part No.	Vendor or Mfr. Name
C1, 2, 13, 15, 19		
C3, 5, 11, 14		
C 12		
C6, 16, 17, 18		
C4, 20		
C7, 8		
C9, 10		
CR1, 2		
Q1 thru 6, 8, 10		
Q 9		
R1		
R2		
R3		
R4		
R5		
R6		
R7		
R8		
R9		
R10, 35, 38		
R11, 36, 39		
R12, 37, 40		
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R14, 42		
R15, 43		
R16, 44		
R17, 45		
R18		
R19		
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R 36		
R 37		
R 38		
R 39		
R 40		
R 41		
R 42		
R 43		
R 44		
R 45		
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XC3, 4		
XC5, 6		
XC7, 8		
XC9, 10		
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XC997, 998		
XC999, 1000		


F
- 22V
D
GROUND
J
INPUT GROUND
L
DATA
FROM MAGNETIC
TAPE RECORDER
REPRODUCE HEAD
R2
510
R20
100
AMPL
C9
6.8
C10
.68
R3
4.3 K
R8
24K
C7
270
mmf
R10
4.3K
R14
24 K
C1
.47
R1
620
Q1
C5
56
Q2
C8
3.6
R13
15K
C3
.47
R7
1.8K
R4
51
R11
51
R6
2.1K
C2
3000
mmf
R5
1.5K
C4
47
R9
6.8K
R12
1.5K
C6
47
R17
6.8K
M
GAIN CONTROL GRD
T
GAIN CONTROL
B
+20 V
INVERTING PULSE AMPLIFIER
R31
100
R35
100
C16
6.8
CR1
5V7
R30
4.7K
R32
10K
C18
6.8
R36
39K
Q7
2N438
R29
10K
C17
6.8
R33
3K
R34
1K
R37
51K
R28
2K
Q6
Q8
2N438
A
OUTPUT TO DATA
STORAGE AND GATE
C
OUTPUT GROUND
E
OUTPUT MONITOR

B

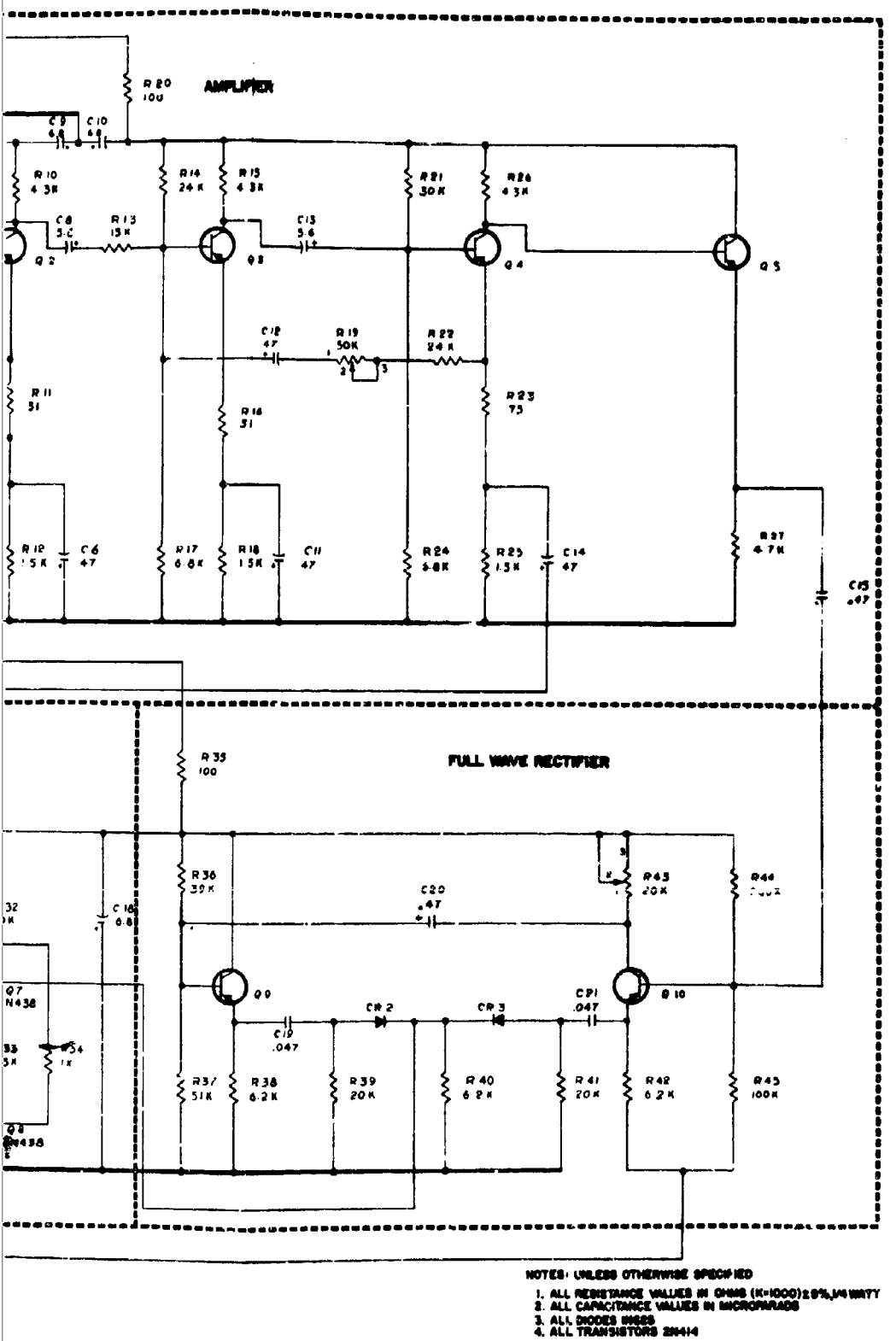
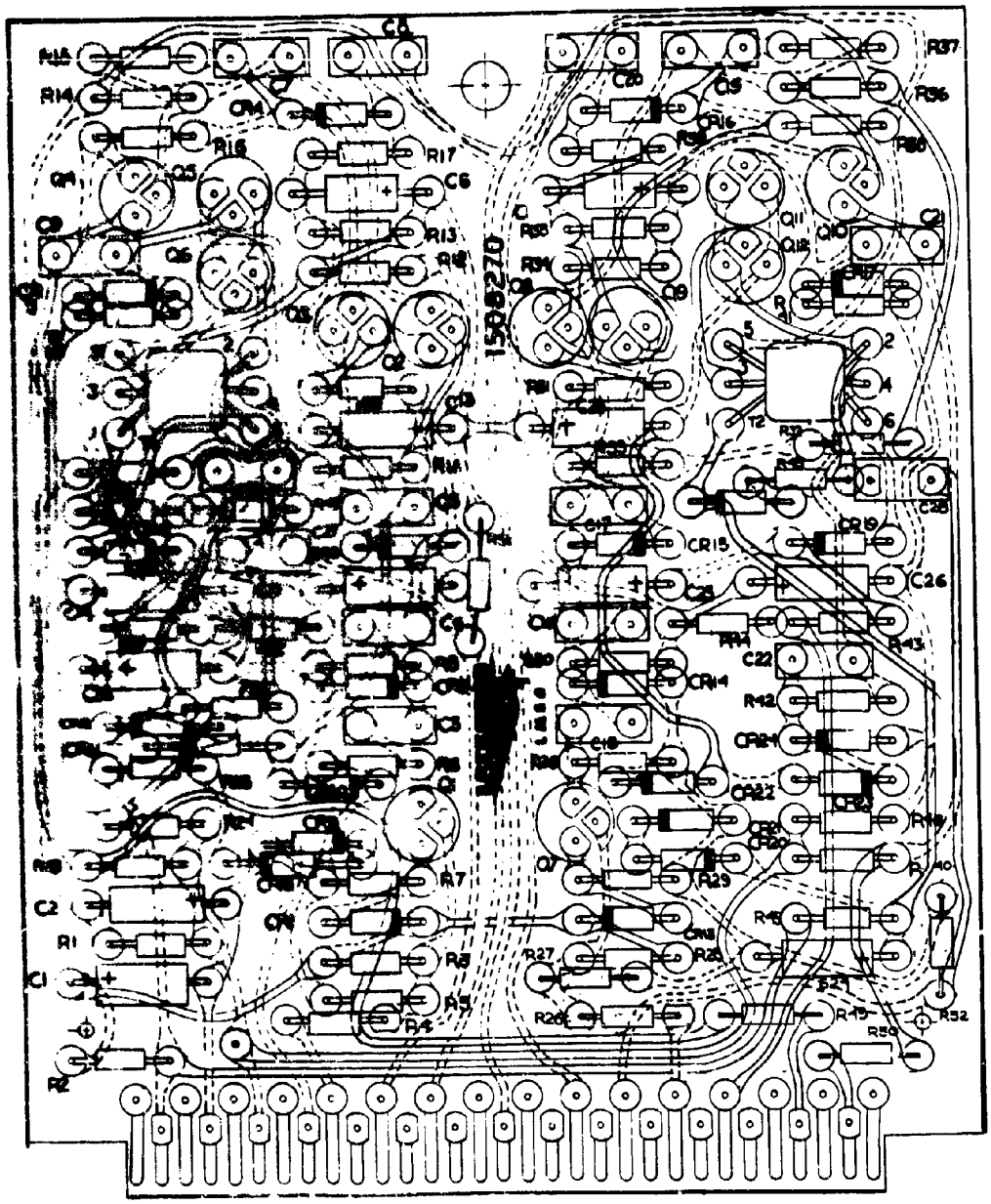
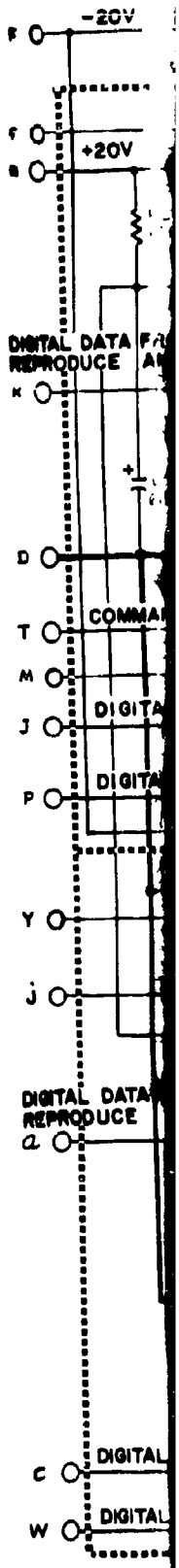


Fig. A-28 Digital Reproduce Amplifier

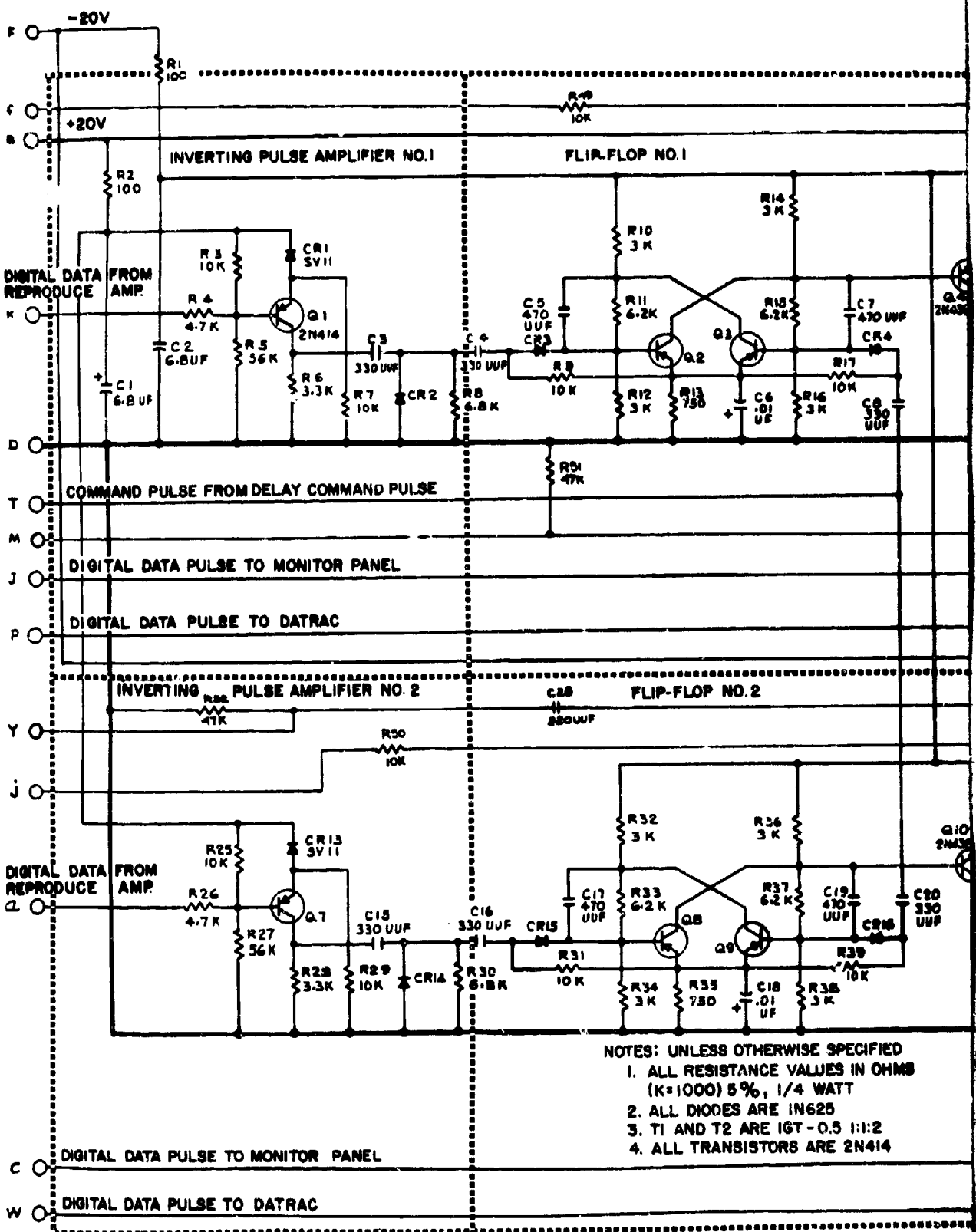




PARTS LIST

Reference Designations	Part No.	Vendor or Mil. Spec.
C1, 2, 12, 13, 14, 24, 28, 30, 34	1SMD681X9K5B1	Sprague Elec. Co., North Adams, Mass.
C3, 4, 6, 9, 15, 16, 29	DM15E330J	Electro Motive Mfg., Willimantic, Conn.
C5, 7, 10, 17, 18, 32	DM15E471J	Electro Motive Mfg., Willimantic, Conn.
C8, 19	1SMD10X5K35A1	Sprague Elec. Co., North Adams, Mass.
C10, 31	DM15E911J	Electro Motive Mfg., Willimantic, Conn.
C11, 20	1SMD684X5K35A1	Sprague Elec. Co., North Adams, Mass.
CR1, 13	6V11	Transitron, Wakefield, Mass.
CR2 thru 4, 11, 14 thru 18, 23	1N128	Fairchild Semiconductor, Carver City, Calif.
CR7, 19	1N645	CBS-Hytron, Lowell, Mass.
CR8, 9, 20, 21	6V7	Transitron, Wakefield, Mass.
CR10, 24	6V9	Transitron, Wakefield, Mass.
CR12, 22	6V8	Transitron, Wakefield, Mass.
Q1, 2, 3, 7, 8, 9	2N834	Raytheon, Needham Heights, Mass.
Q4, 5, 6, 10, 11, 12	2N525	CBS-Hytron, Lowell, Mass.
R1, 3, 49, 50	RCR07G161J	MIL-R-11
R2, 7, 8, 17, 18, 38, 39, 51, 52, 60, 64	RCR07G103J	MIL-R-11
R4, 35	RCR07GF47J	MIL-R-11
R5, 37	RCR07GF68J	MIL-R-11
R6, 19, 36, 46	RCR07GF330J	MIL-R-11
R9, 20	RCR07GF68J	MIL-R-11
R10, 12, 14, 16, 32, 34, 40, 58	RCR07GF39J	MIL-R-11
R11, 15, 33, 57	RCR07GF68J	MIL-R-11
R13, 31, 55, 45	RCR07GF51J	MIL-R-11
R30, 42	RCR07GF61J	MIL-R-11
R22, 54	RCR07GF61J	MIL-R-11
R53, 56, 48, 44	RCR07GF34J	MIL-R-11
R41, 43		

A


-20V
+20V
R1 100
R49 10K
INVERTING PULSE AMPLIFIER NO.1
FLIP-FLOP NO.1
R2 100
DIGITAL DATA FROM REPRODUCE AMP.
R3 10K
CR1 5V11
R4 4.7K
Q1 2N414
C2 6.8UF
R5 56K
C3 330 UUF
C4 330 UUF
C1 6.8 UF
R6 3.3K
R7 10K
CR2
R8 6.8K
C5 470 UUF
CR3
R9 10K
R10 3K
R11 6.2K
R12 3K
R13 750
Q2
Q3
R14 3K
R15 6.2K
C6 .01 UF
R16 3K
C7 470 UUF
CR4
R17 10K
C8 330 UUF
R51 47K
COMMAND PULSE FROM DELAY COMMAND PULSE
DIGITAL DATA PULSE TO MONITOR PANEL
DIGITAL DATA PULSE TO DATRAC
INVERTING PULSE AMPLIFIER NO. 2
R52 47K
C28 330UUF
FLIP-FLOP NO.2
R50 10K
DIGITAL DATA FROM REPRODUCE AMP.
R25 10K
CR13 3V11
R26 4.7K
Q7
R27 56K
C18 330 UUF
C16 330 UUF
CR15
R28 3.3K
R29 10K
CR14
R30 6.8K
R31 10K
C17 470 UUF
R32 3K
R33 6.2K
R34 3K
R35 750
Q8
Q9
R36 3K
C18 .01 UF
R37 6.2K
C19 470 UUF
CR16
R38 10K
C20 330 UUF
Q10 2N43
NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTANCE VALUES IN OHMS (K=1000) 5%, 1/4 WATT
2. ALL DIODES ARE IN625
3. T1 AND T2 ARE IGT-0.5 1:1:2
4. ALL TRANSISTORS ARE 2N414
DIGITAL DATA PULSE TO MONITOR PANEL
DIGITAL DATA PULSE TO DATRAC

B

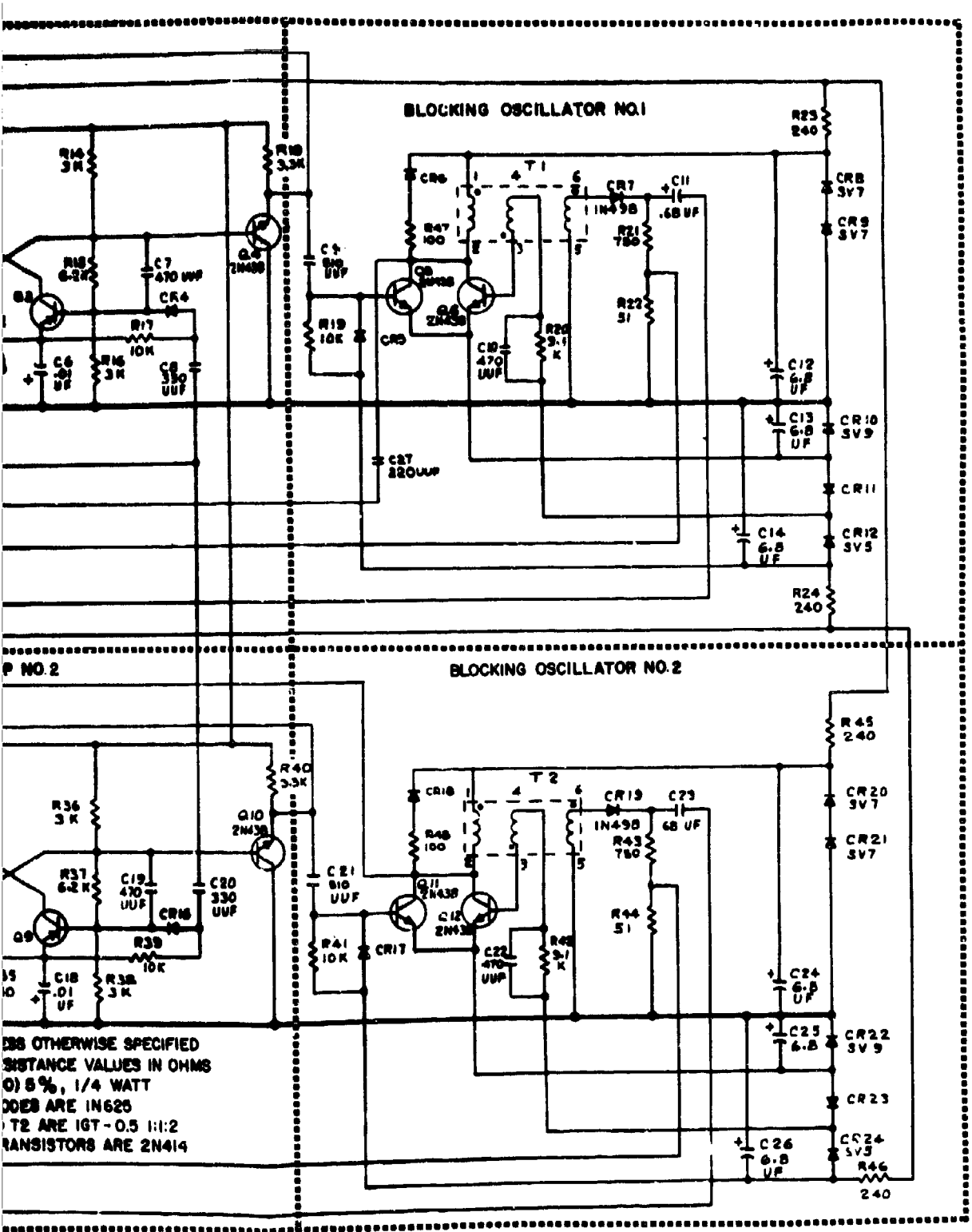
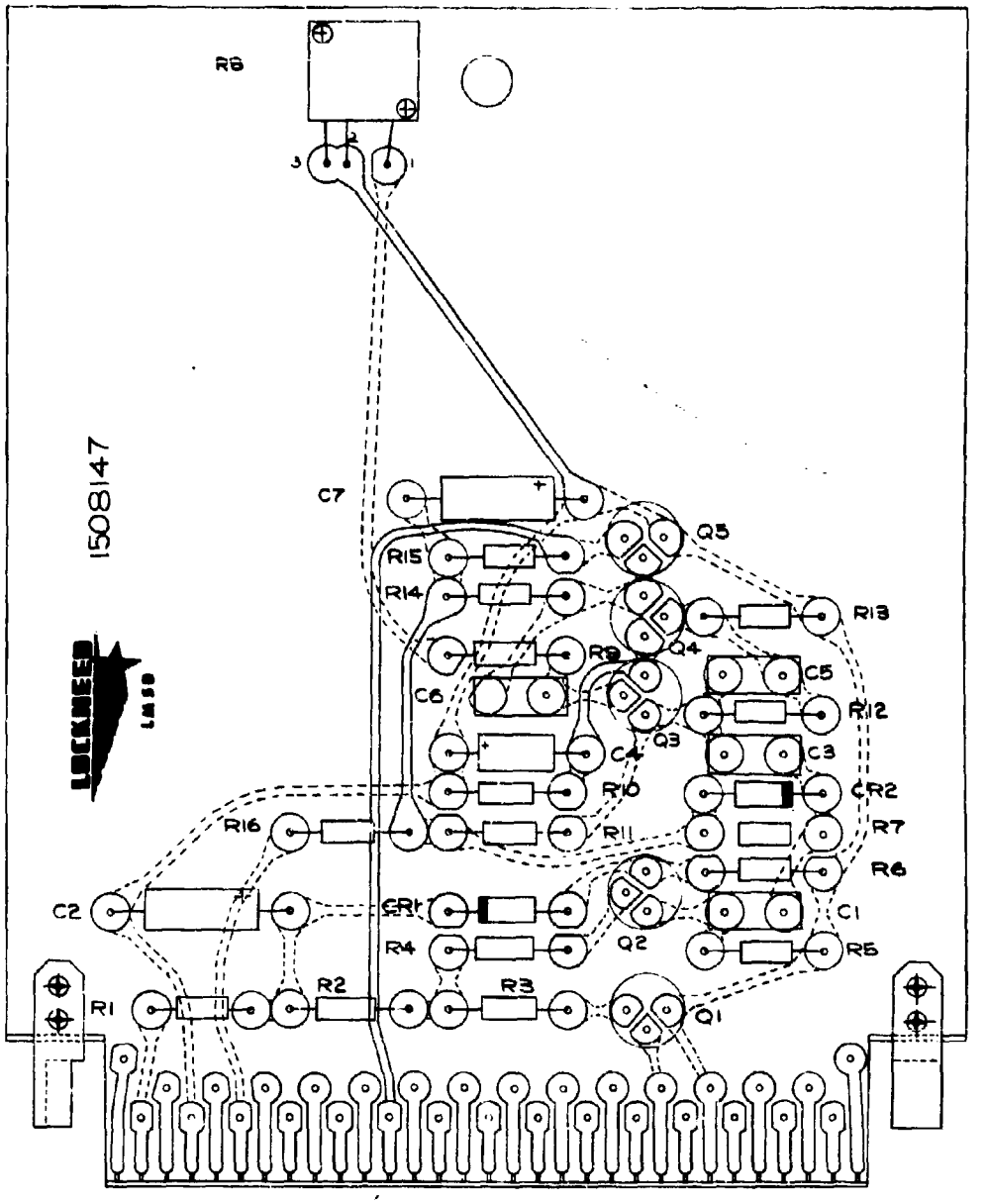


Fig. A-29 Data Storage and Gate



PARTS LIST

Reference Designation	Part No.	Vendor or MIL Desc.
C1, 3	[illegible]	El Monte, Los Angeles, Calif.
C2, 7	[illegible]	Sprague Electric Co., North Adams, Mass
C4	[illegible]	Sprague Electric Co., North Adams, Mass
C5	[illegible]	El Monte, Los Angeles, Calif.
C6	[illegible]	El Monte, Los Angeles, Calif.
CR1	[illegible]	Transitron, Wakefield, Mass.
CR2	[illegible]	Pacific Semiconductor, Culver City, Calif.
Q1 thru 4	[illegible]	Raytheon, Newton, Mass.
R1	[illegible]	CTS Berne, Elkhart, Ind.
R2, 16	RCR07G[illegible]J	MIL-R-11
R3, 9	RCR07G[illegible]J	MIL-R-11
R4	RCR07G[illegible]J	MIL-R-11
R5	RCR07G[illegible]J	MIL-R-11
R6	RCR07G[illegible]J	MIL-R-11
R7	RCR07G[illegible]J	MIL-R-11
R8	RCR07G[illegible]J	MIL-R-11
R10	311-04-100	Dynamics Pacific, Simi Simiens, Calif.
R11	RCR07G[illegible]J	MIL-R-11
R12	RCR07G[illegible]J	MIL-R-11
R13, 14, 15	RCR07G[illegible]J	MIL-R-11
R16	RCR07G[illegible]J	MIL-R-11
R17	RCR07G[illegible]J	MIL-R-11

OUTPUT FROM DATA
DIGITAL REPRODUCE
AMPLIFIER

D
GROU

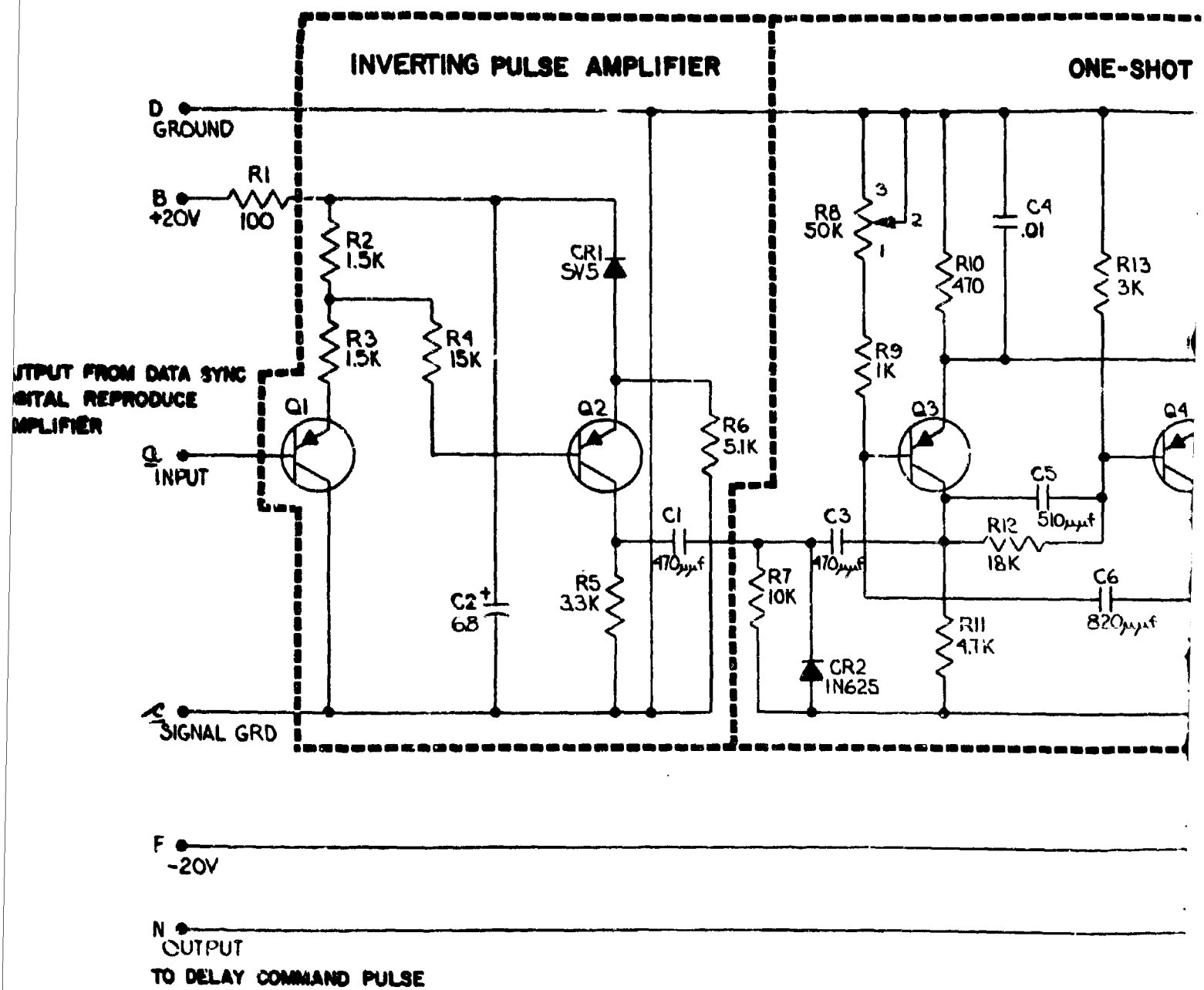
B
+20V

A
INPUT

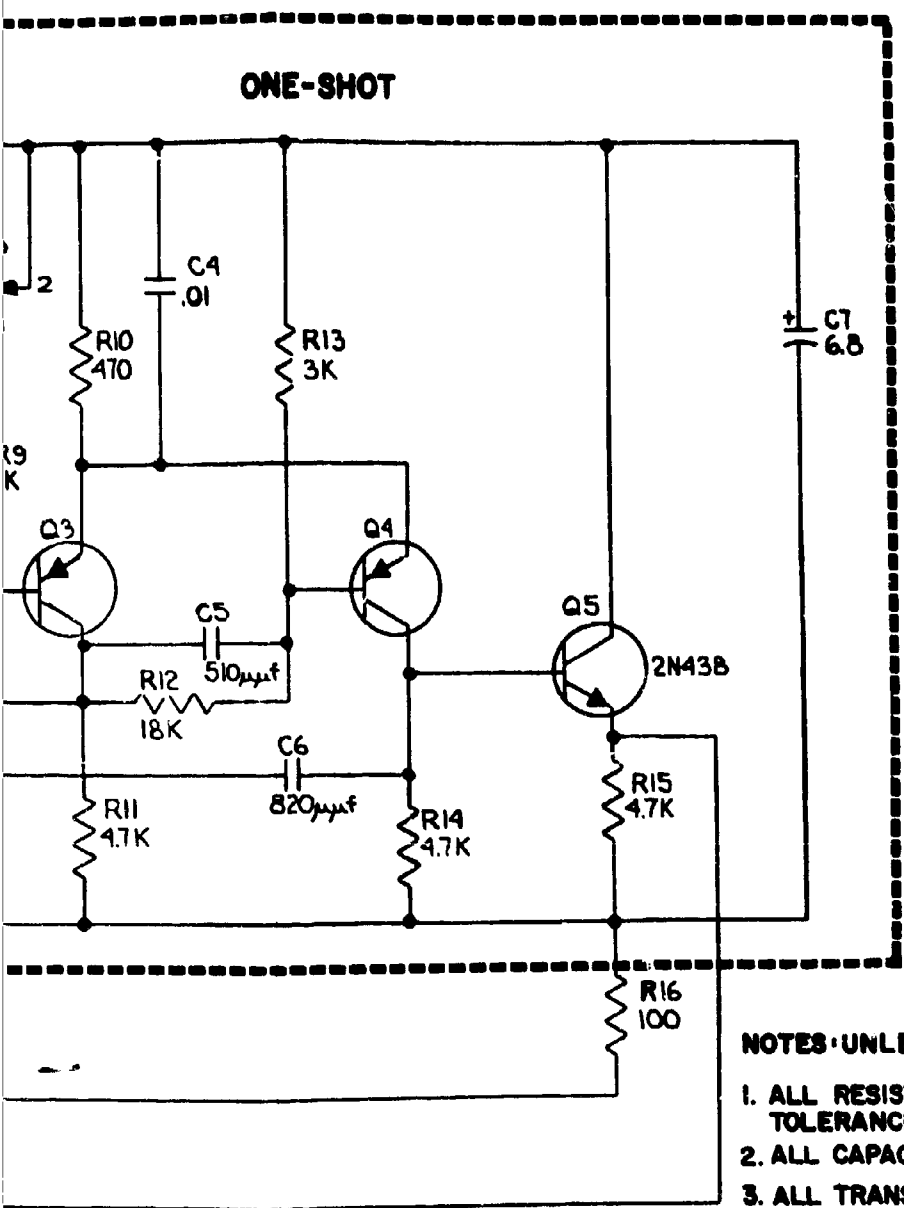
F
SIGNA

F
-20V

N
OUTP
TO DE


INVERTING PULSE AMPLIFIER
ONE-SHOT
D
GROUND
B
+20V
R1
100
R2
1.5K
R3
1.5K
R4
15K
CR1
SV5
R8
50K
3
2
1
C4
.01
R10
470
R13
3K
R9
1K
UTPUT FROM DATA SYNC
RITAL REPRODUCE
MPLIFIER
Q1
Q2
Q3
Q4
R6
5.1K
C5
510μμf
C
INPUT
C1
470μμf
C3
470μμf
R12
18K
C6
820μμf
C2
68
R5
33K
R7
10K
R11
4.7K
CR2
1N625
SIGNAL GRD
F
-20V
N
OUTPUT
TO DELAY COMMAND PULSE

B

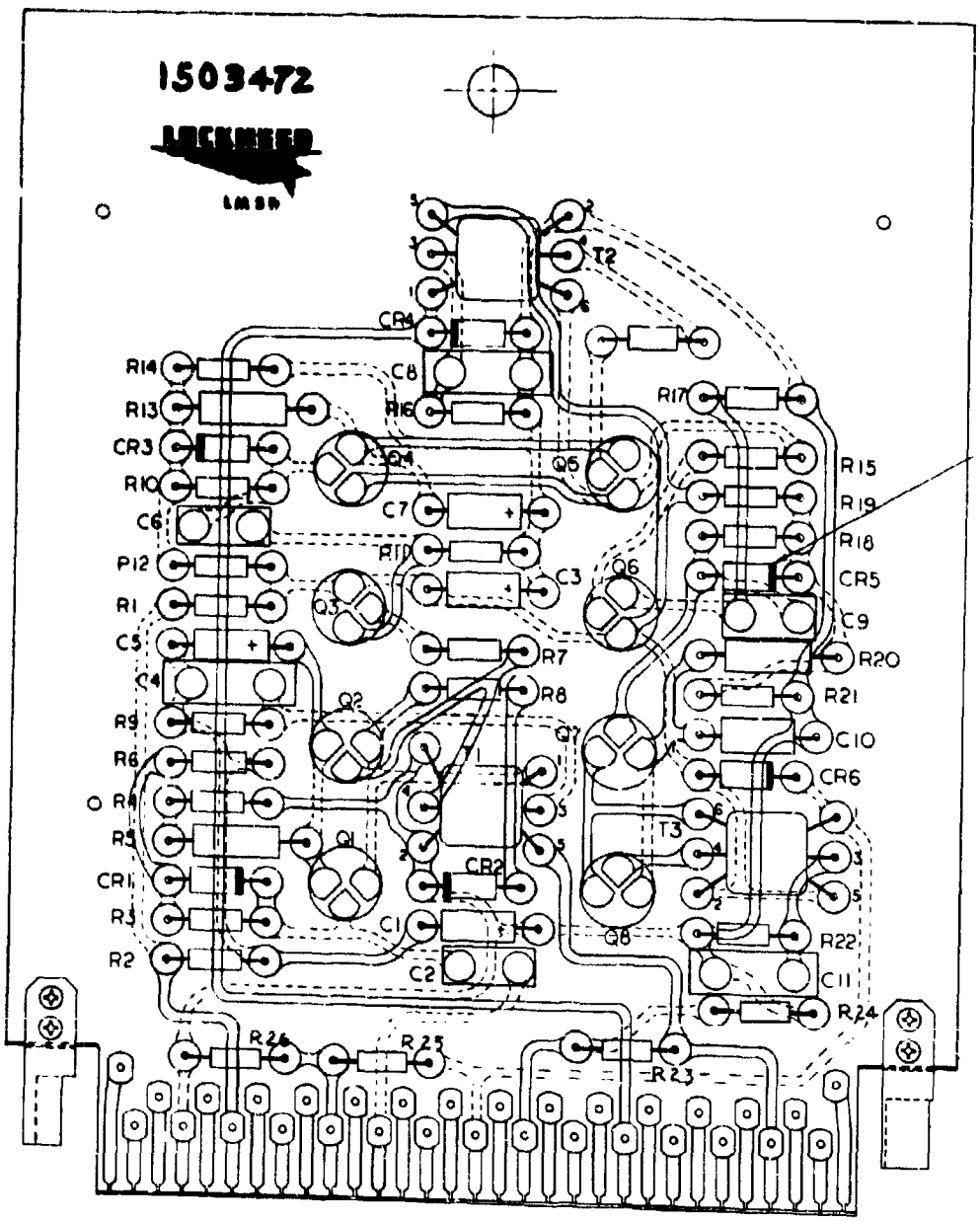


NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTANCE VALUES IN OHMS (K=1000) ±5% TOLERANCE, 1/4 WATT
2. ALL CAPACITANCE VALUES IN MICROFARADS
3. ALL TRANSISTORS 2N414

Fig. A-30 Data Sync Delay Reproduce

1503472



PARTS LIST

Reference Designation	Part No	Vendor or Mfg Item
C1,8		
C2,6,9		
C4		
C5,7,10		
C8,11		
CR1,3,5		
CR2,4,6		
Q1,8		
Q2 thru 7		
R1,8		
R2,4,14,16,18,19,22,25		
R3,12,20		
R6		
R7,15		
R9		
R10,13,21		
R11,17		
R23,24,26		
R12,19		
T1		
T2,3		

J OUTPUT MONITOR

T OUTPUT #3 COMMAND PULS

S OUTPUT #2 DATA SYNC TO D

F -20V

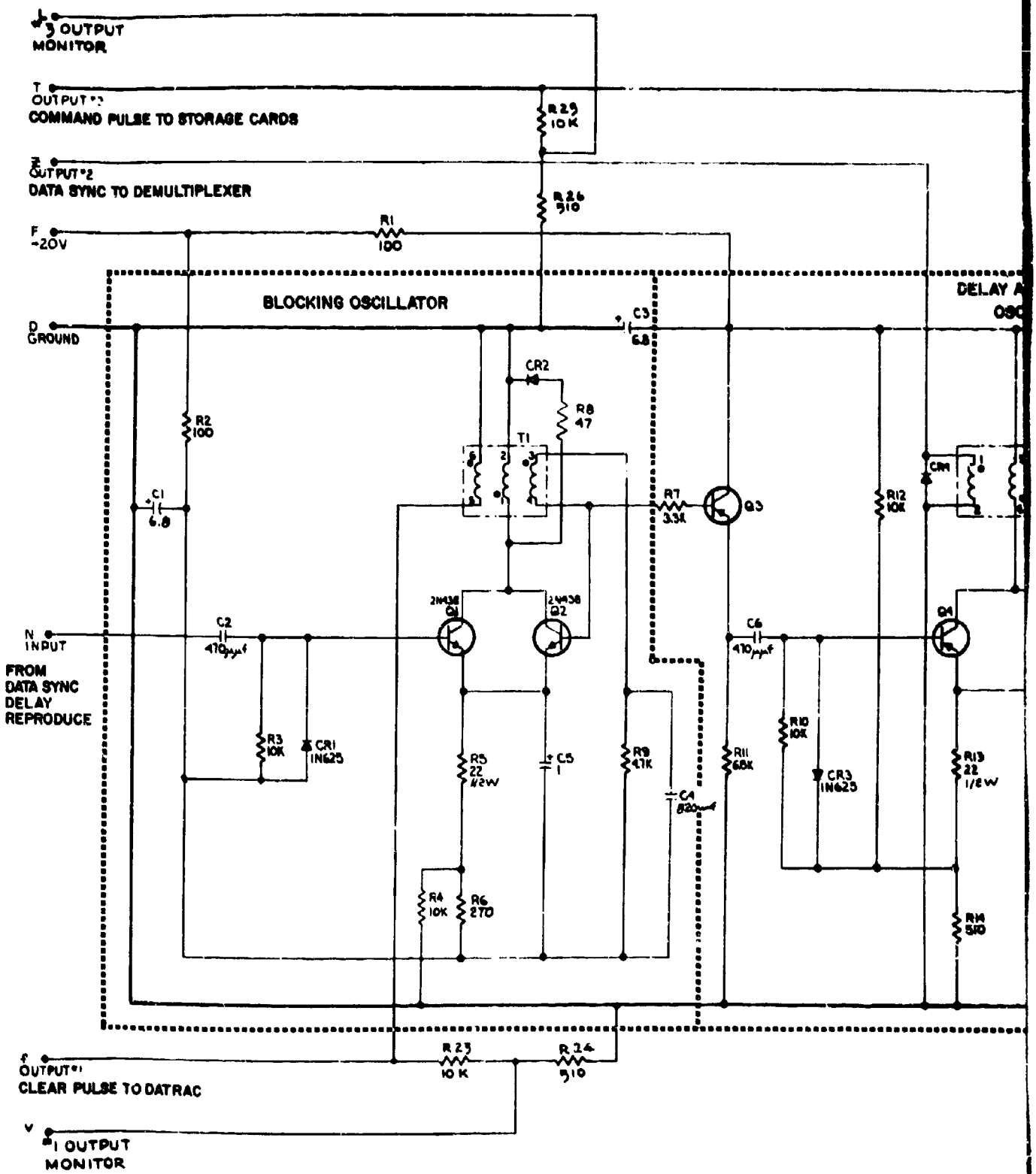
D GROUND

N INPUT - FROM DATA SYNC DELAY REPRODUCE

F OUTPUT #1 CLEAR PULSE T

V OUTPUT MONITOR

A


J OUTPUT MONITOR
T OUTPUT #3 COMMAND PULSE TO STORAGE CARDS
R OUTPUT #2 DATA SYNC TO DEMULTIPLEXER
F -20V
D GROUND
N INPUT FROM DATA SYNC DELAY REPRODUCE
S OUTPUT #1 CLEAR PULSE TO DATRAC
V #1 OUTPUT MONITOR
BLOCKING OSCILLATOR
DELAY A
OSC
R1 100
R2 100
R3 10K
R4 10K
R5 22 1/2W
R6 270
R7 3.3K
R8 47
R9 47K
R10 10K
R11 68K
R12 10K
R13 22 1/2W
R14 510
R23 10K
R24 510
R25 10K
R26 510
C1 6.8
C2 470μμf
C3 6.8
C4 820μμf
C5 1
C6 470μμf
CR1 IN625
CR2
CR3 IN625
CR4
T1
Q1 2N438
Q2 2N438
Q3
Q4

B

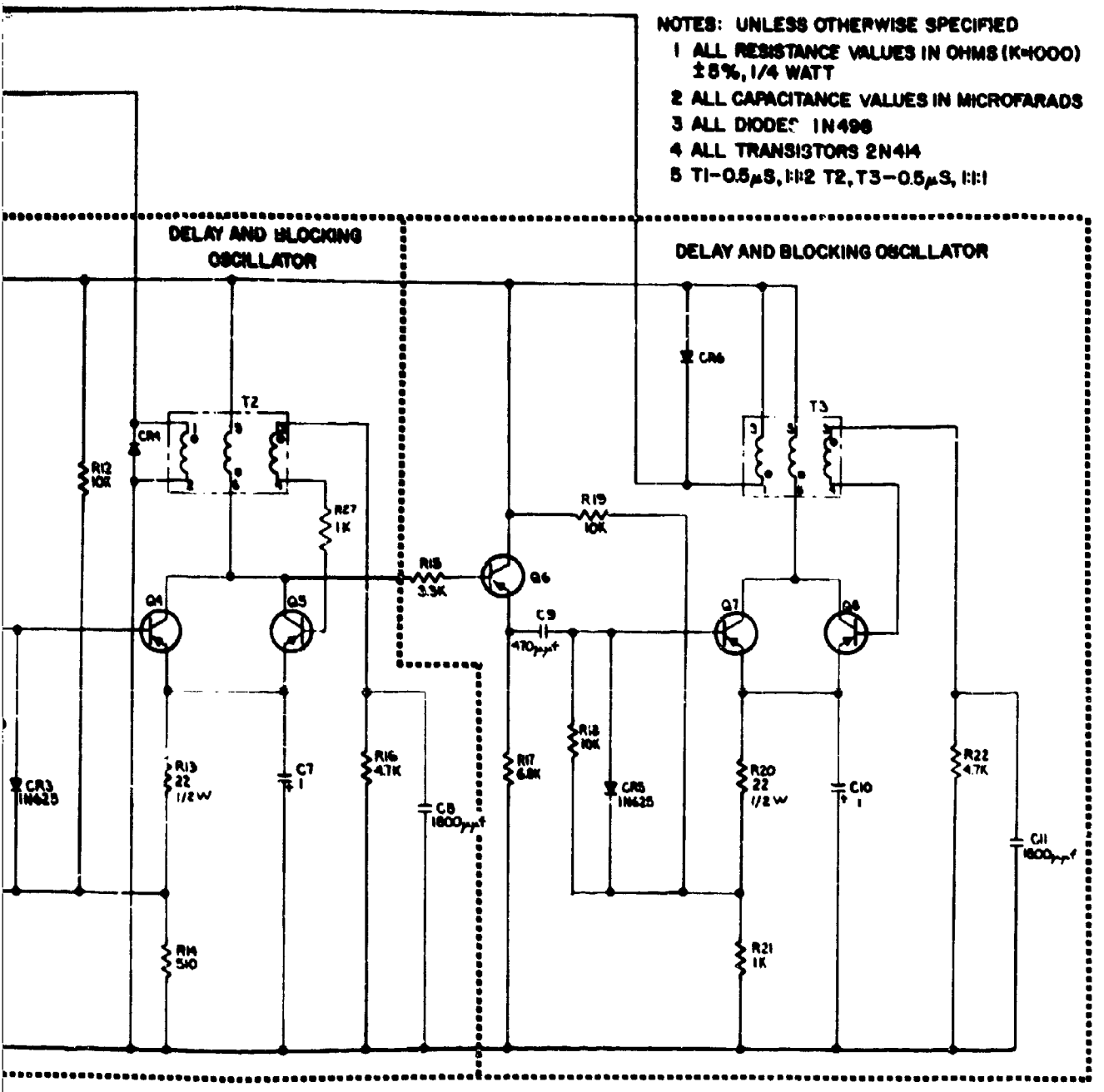
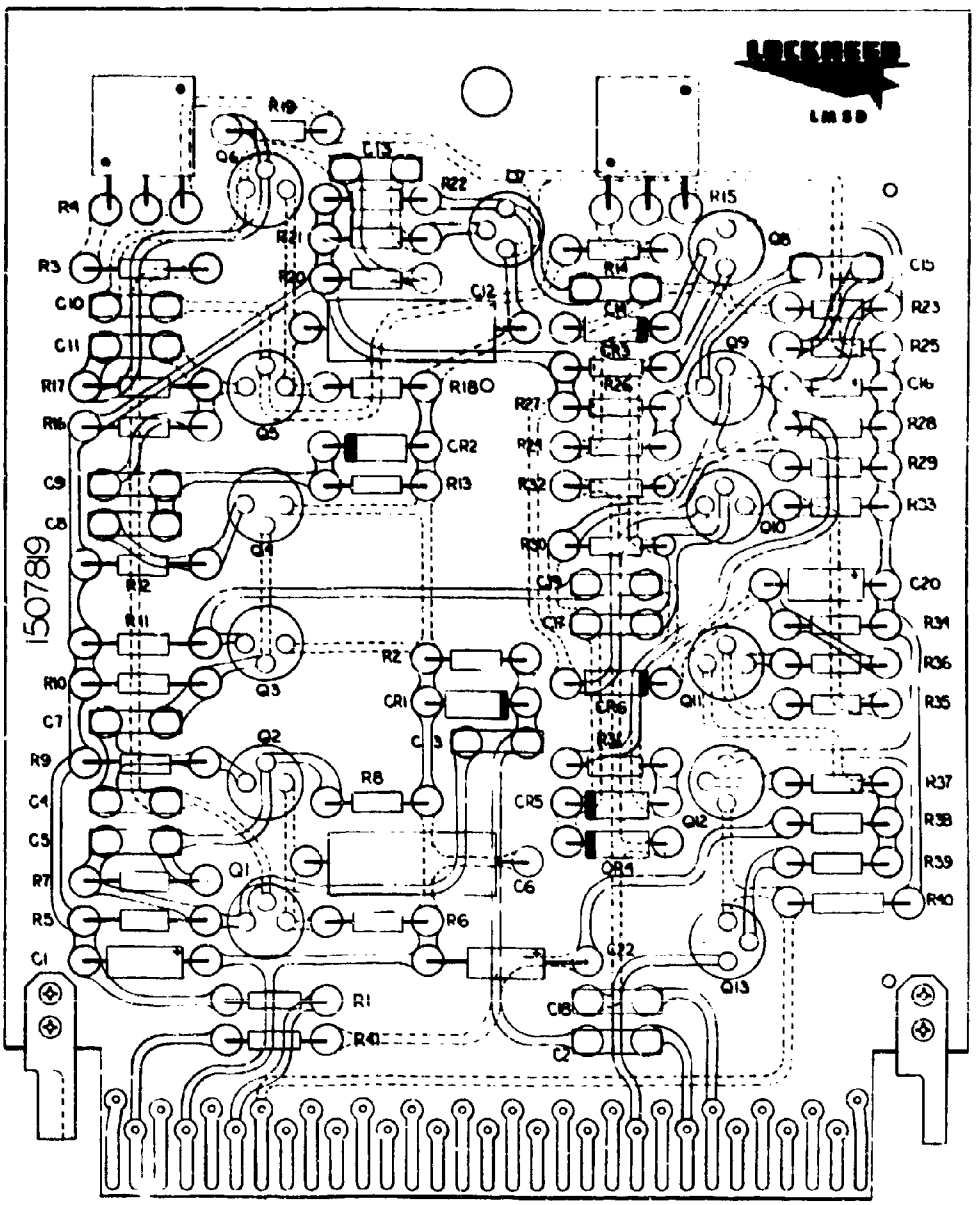


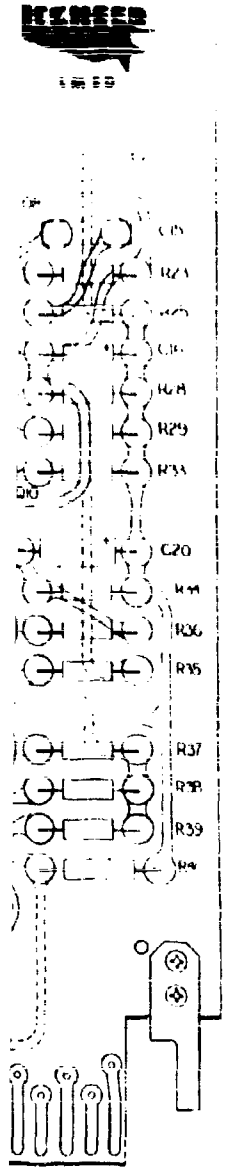
Fig. A-31 Delay Command Pulse

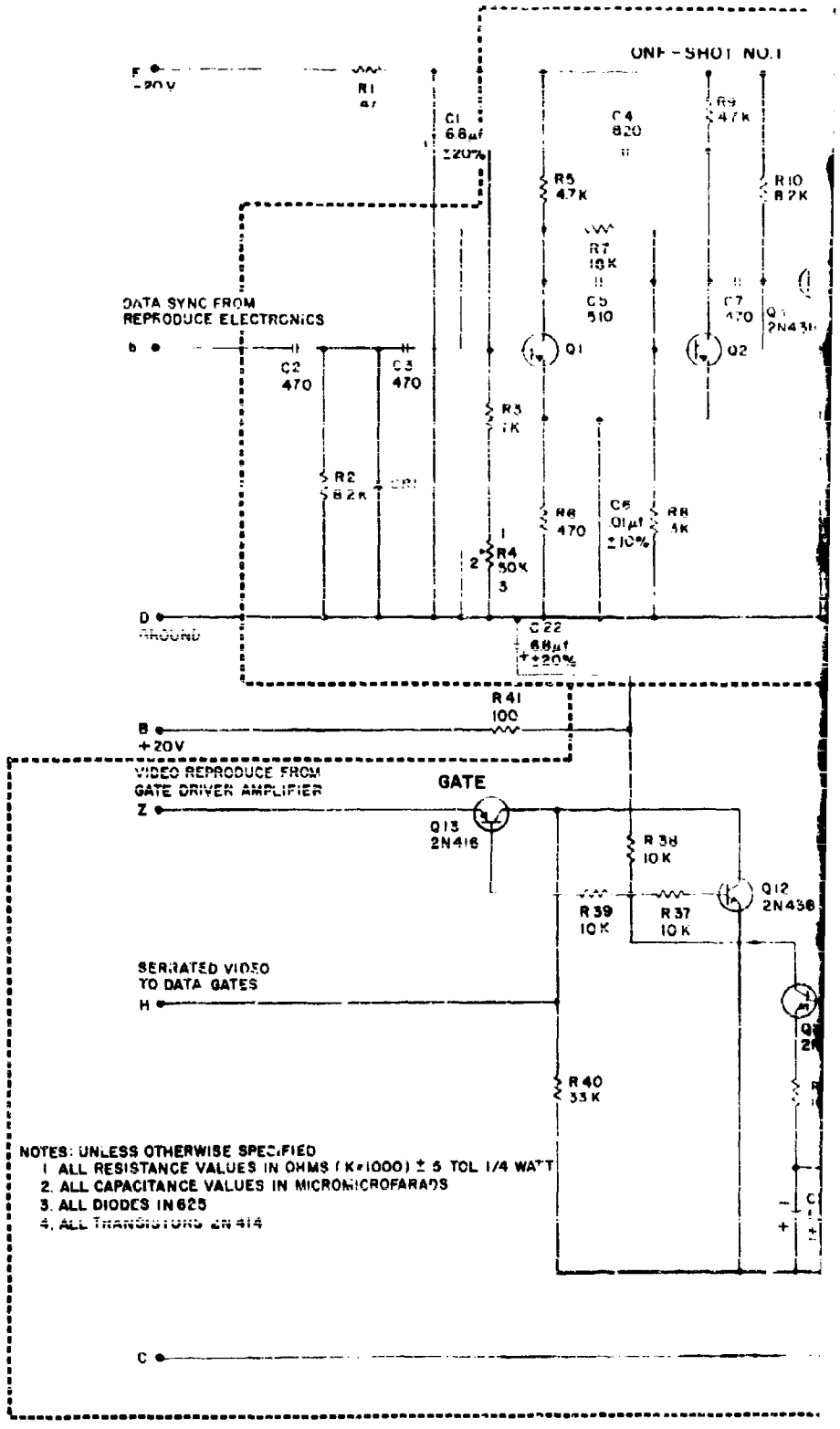


PARTS LIST

Reference Designation	Part No.	Vendor or Mfr. Spec.
C1, 20, 22	150D686X9035B1	Sprague Electric Co., North Adams, Mass.
C2, 3, 7, 8, 9, 13, 14, 15, 17, 18, 19	DM15F471J	El Mesco, Los Angeles, Calif.
C4, 10	DM15F821J	El Mesco, Los Angeles, Calif.
C5, 11	DM15F511J	El Mesco, Los Angeles, Calif.
C6, 12	CPSSA1KB103K1	Sprag. - Electric Co., North Adams, Mass.
C16	150D106X9006A2	Sprague Electric Co., North Adams, Mass.
CR1 thru 7	1N658	Pacific Semiconductor, Culver City, Calif.
CR8	SV138	Transitron, Wakefield, Mass.
Q1, 2, 5, 6, 8, 9, 10	2N414	Raytheon Mfg. Co., Newton, Mass.
Q3, 4, 7, 11, 12	2N438	CBS-Hytron, Danvers, Mass.
Q13	2N416	Raytheon Mfg. Co., Newton, Mass.
R1	RC07GF470J	MIL-R-11
R2, 10, 13, 21	RC07GF822J	MIL-R-11
R3, 14	RC07GF100J	MIL-R-11
R4, 15	313-64-50K	Davenport-Pacific Santa Monica, Calif.
R5, 9, 16, 20	RC07GF471J	MIL-R-11
R6, 18	RC07GF471J	MIL-R-11
R7, 17	RC07GF103J	MIL-R-11
R8, 19, 24, 26, 27, 28	RC07GF302J	MIL-R-11
R11, 22, 29, 30, 33, 34	RC07GF822J	MIL-R-11
R23, 31, 32, 37, 38, 39	RC07GF105J	MIL-R-11
R35	RC07GF751J	MIL-R-11
R36	RC07GF982J	MIL-R-11
R36 41	RC07GF131J	MIL-R-11
R40	MS35649-11	MIL-R-11

A




ONE-SHOT NO.1
-20V
R1
C1
6.8µf
±20%
C4
820
R9
47K
R10
8.2K
R5
4.7K
R7
18K
C5
510
C7
470
Q1
2N438
Q2
DATA SYNC FROM
REPRODUCE ELECTRONICS
C2
470
C3
470
R3
1K
R2
8.2K
CR1
R6
470
C6
.01µf
±10%
R8
4K
R4
50K
D
GROUND
C22
6.8µf
±20%
R41
100
B
+20V
VIDEO REPRODUCE FROM
GATE DRIVER AMPLIFIER
GATE
Z
Q13
2N416
R38
10K
Q12
2N438
R39
10K
R37
10K
SERRATED VIDEO
TO DATA GATES
H
R40
33K
NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTANCE VALUES IN OHMS (K=1000) ± 5 TOL 1/4 WATT
2. ALL CAPACITANCE VALUES IN MICROMICROFARADS
3. ALL DIODES IN625
4. ALL TRANSISTORS 2N414
C

B

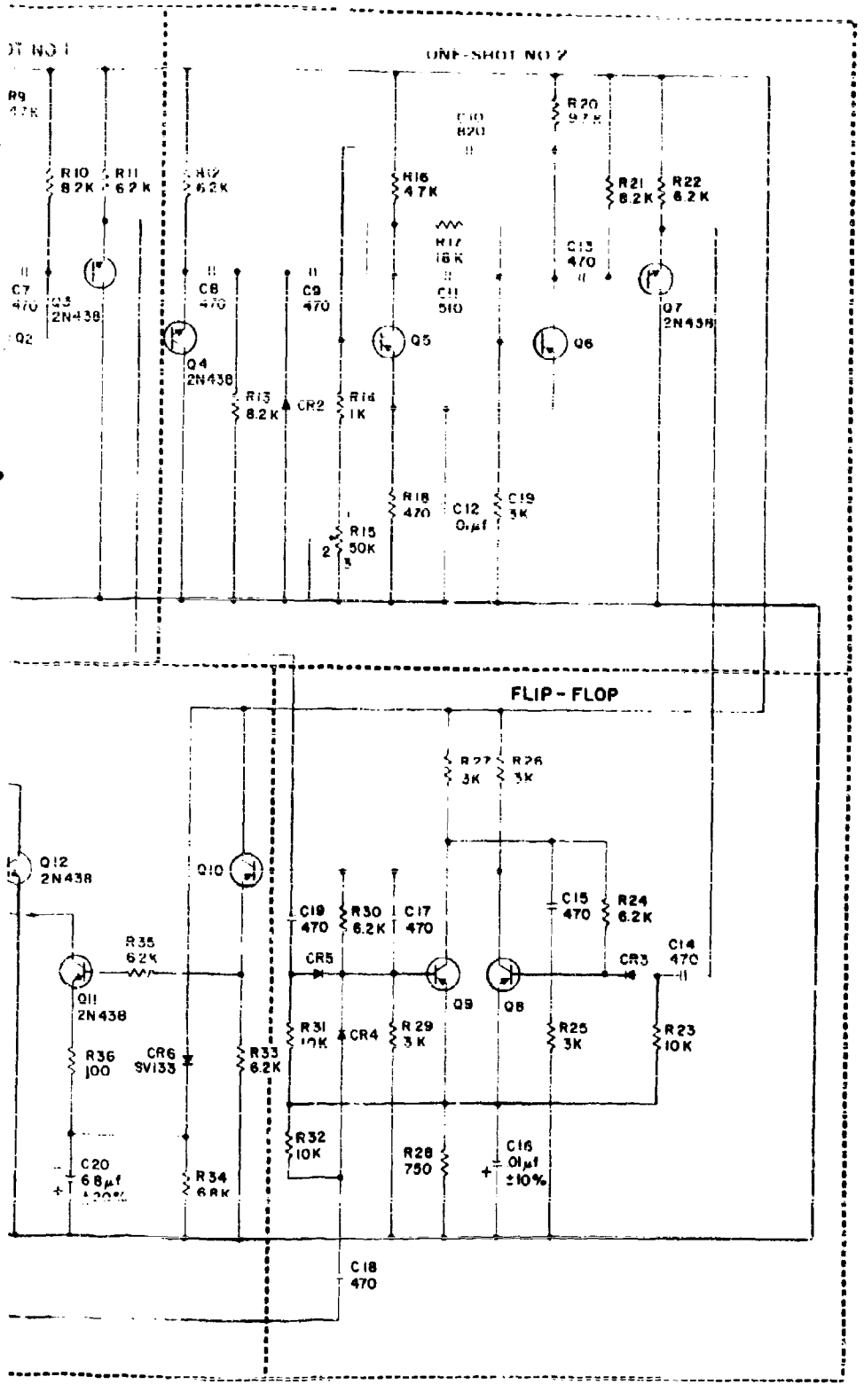
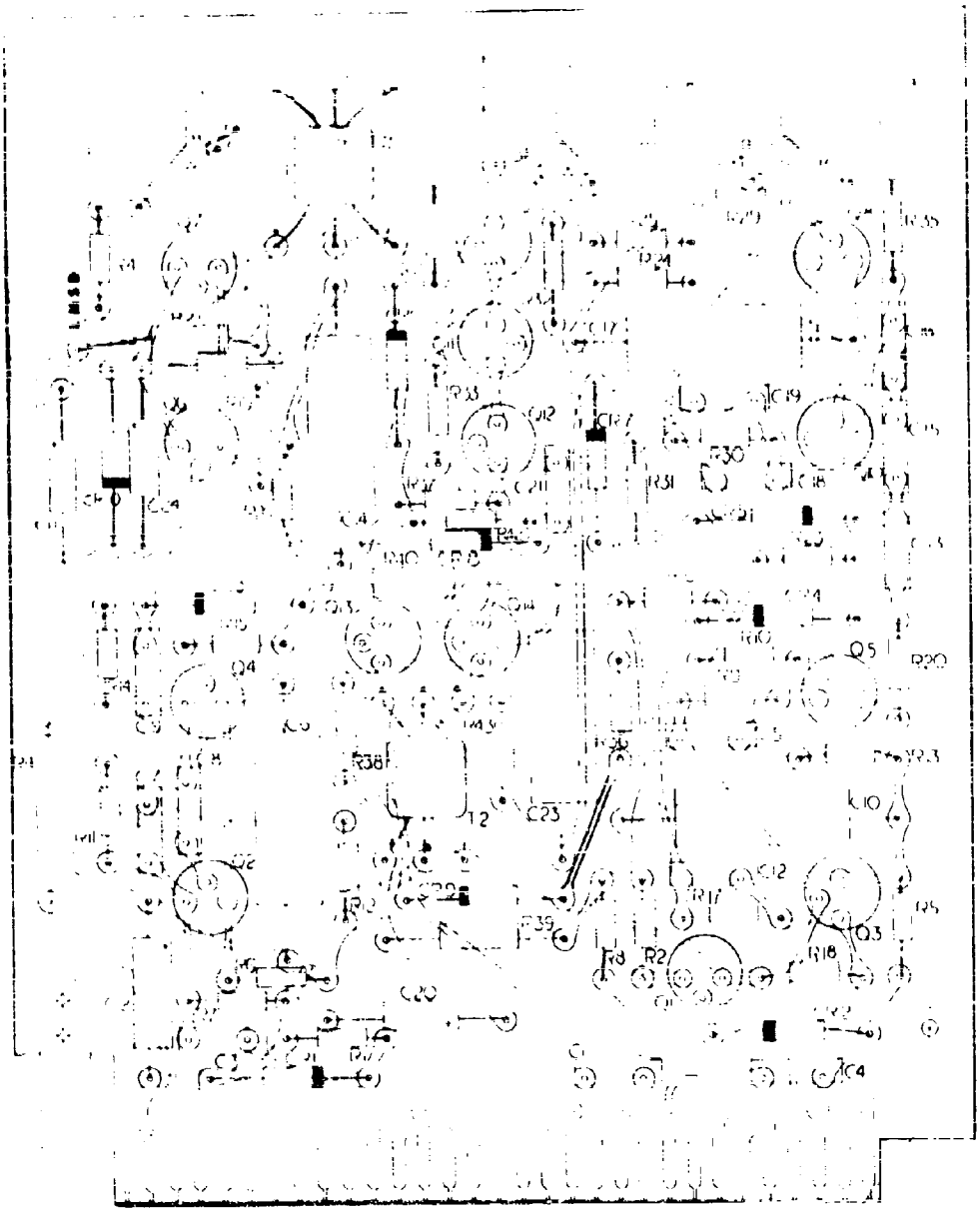
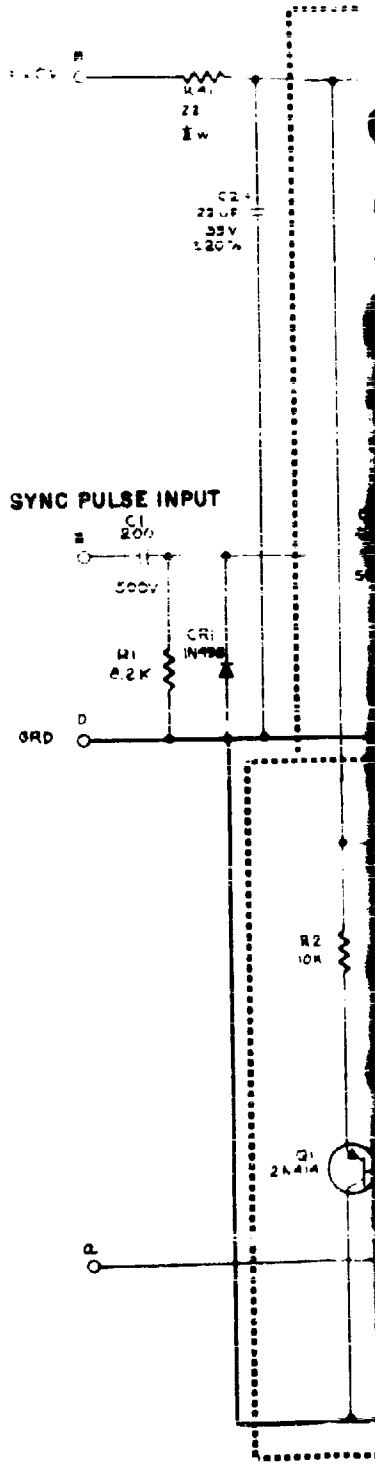


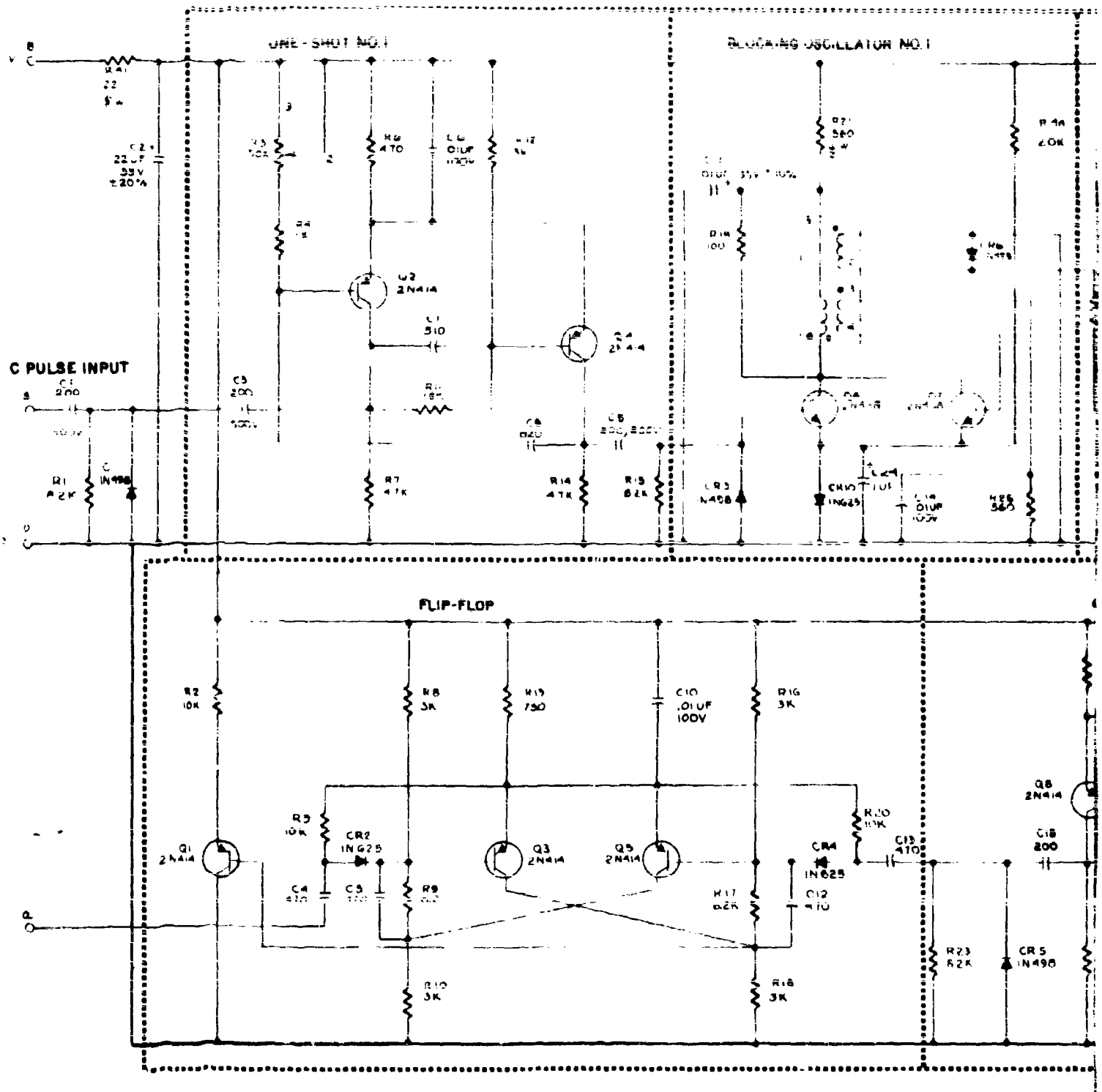
Fig. A-32 Duty Cycle I





PARTS LIST

Reference Designation	CRC Ctl	Vendor or Mfg Name
C1, 5, 8, 14, 15, 21	DM15F-B3J	El Mento, Los Angeles, Calif
C9	1500A47A2x3GA4	Sprague Electric Co., North Adams, Mass
C2, 3, 12, 13	DM15F-A2J	El Mento, Los Angeles, Calif
C6, 10, 16, 17, 18	[illegible]	Sprague Electric Co., North Adams, Mass
C7, 19	DM15E-B4J	El Mento, Los Angeles, Calif
C11, 20	DM15F-B2J	El Mento, Los Angeles, Calif
C22	[illegible]	Sprague Electric Co., North Adams, Mass
C24	150D104X9050A2	Sprague Electric Co., North Adams, Mass
CR1, 2, 3	1N456	GE Semi., Syracuse, Mass
CR4, 5, 10	1N456	Sperry Semiconductor, Palmer City
Q1 thru 3, 8, 9, 10	2N438	Raytheon, Newton, Mass
Q4, 7, 8, 11, 13, 14	2N438	Gen Electric, Syracuse, Mass
Q12	2N438	Gen Electric, Syracuse, Mass
R1, 15, 24, 40	RC07GF682J	MIL R 11
R2, 5, 36, 39	RC07GF103J	MIL R 11
R3, 34	Same as R2	Laboratory Prod'ts, Santa Monica, Calif, and MIL R 11
R4, 30, 34	RC07GF104J	MIL R 11
R6, 26, 27, 31	RC07GF471J	MIL R 11
R7, 14, 16, 37, 41	RC07GF473J	MIL R 11
R8, 12, 18, 28, 38, 40	RC07GF822J	MIL R 11
R9, 17	RC07GF223J	MIL R 11
R10	RC07GF392J	MIL R 11
R11	RC07GF331J	MIL R 11
R13	RC07GF151J	MIL R 11
R19, 35	RC07GF152J	MIL R 11
R21, 29	RB3B4065 6%	MIL R 11
R22, 42	RB3B4065 5%	MIL R 11
R23, 33	RC07GF561J	MIL R 11
R25	See R2 ckt	Laboratory Prod'ts, Santa Monica, Calif
R32, 37	RC07GF105M	MIL R 11
R101	MF-1B4F1.5T	MIL R 11
R44	[illegible]	MIL R 11
T1, 2	TOF 6-1	Chalkman, Santa Monica, Calif


ONE-SHOT NO.1
BLOCKING OSCILLATOR NO.1
C PULSE INPUT
FLIP-FLOP
Q2 2N414
Q4 2N414
CR1 IN498
CR2 IN625
CR3 IN498
CR4 IN625
CR5 IN498
Q1 2N414
Q3 2N414
Q5 2N414
Q6 2N414
R1 2.2K
R2 10K
R3 10K
R4 1K
R5 10K
R6 470
R7 4.7K
R8 3K
R9 620
R10 3K
R11 18K
R12 2K
R13 750
R14 4.7K
R15 8.2K
R16 3K
R17 8.2K
R18 3K
R19 750
R20 10K
R21 560
R22 2.0K
R23 8.2K
R24 565
C1 200
C2 22 UF 35V ±20%
C3 200
C4 620
C5 200
C6 620
C7 510
C8 200, 500
C9 .01UF 1000V
C10 .01UF 100V
C11 .01UF 1000V
C12 470
C13 470
C14 1 UF
C15 .01UF 100V
C16 200

B

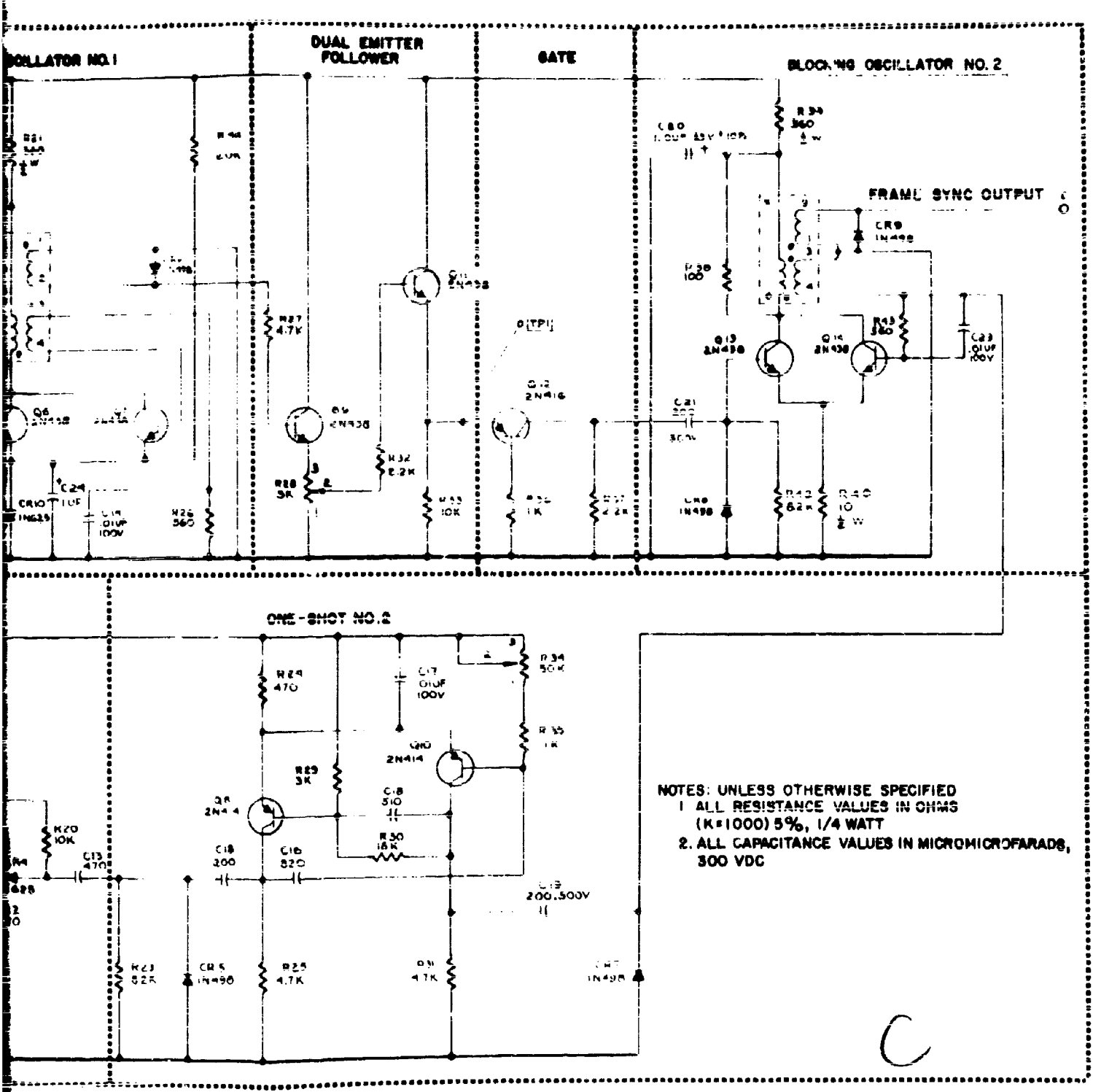
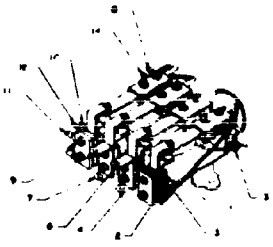


Fig. A-33 Frame Sync Delay Reproduce, Vibration



ASEKIS RELAYS

A

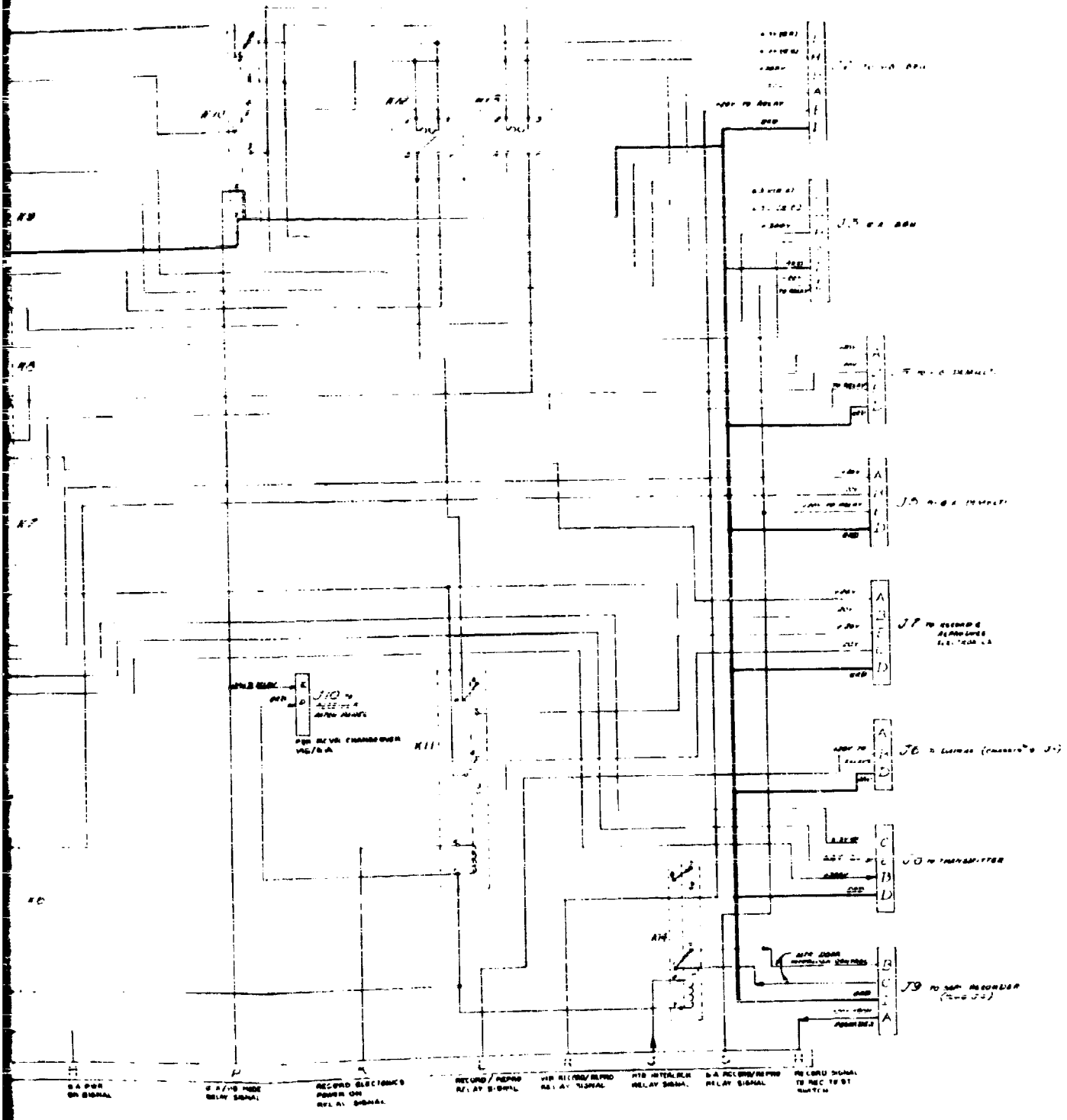
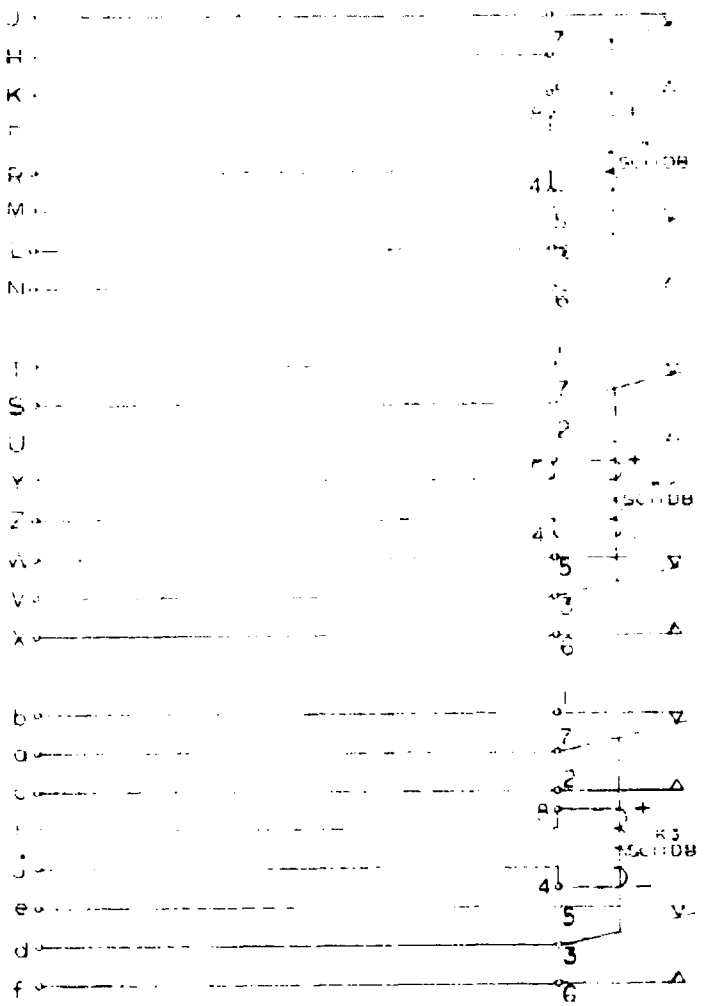
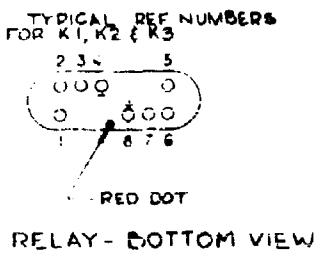


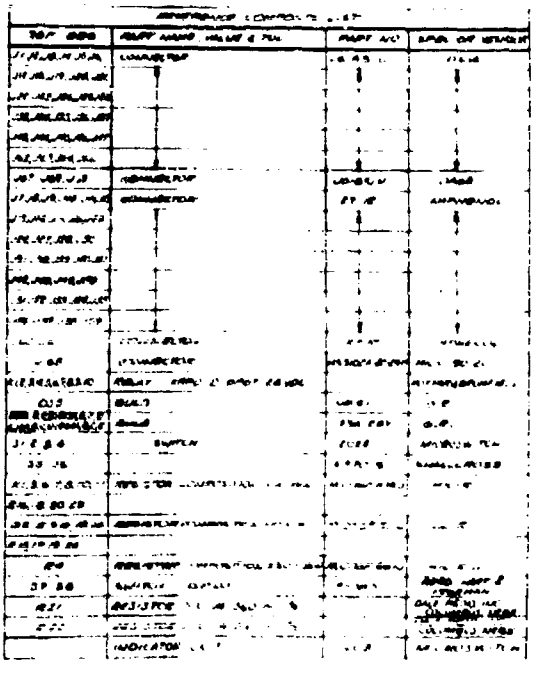
Fig. A-34 Power Supply Interlock

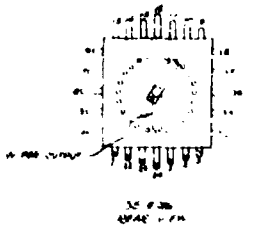


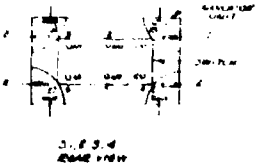


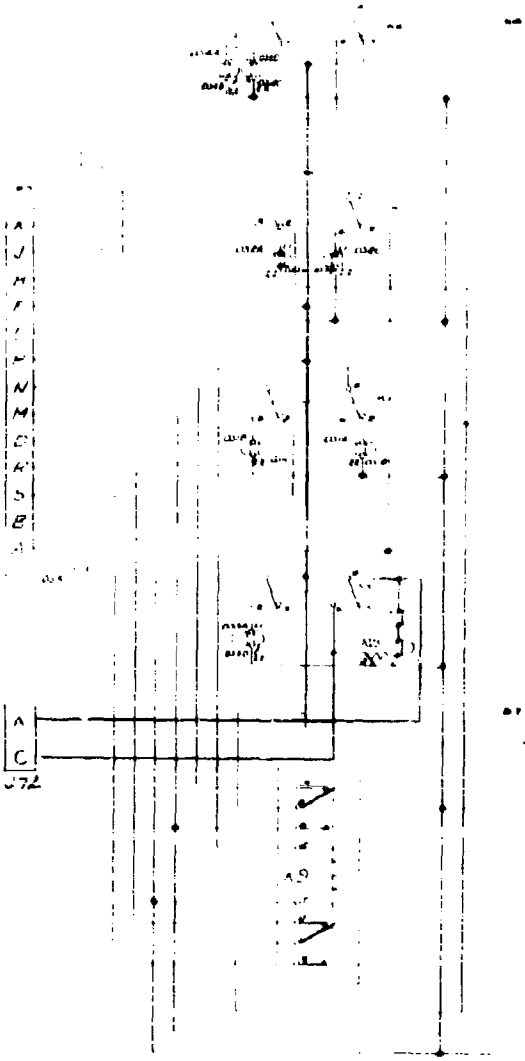
RELAY - BOTTOM VIEW

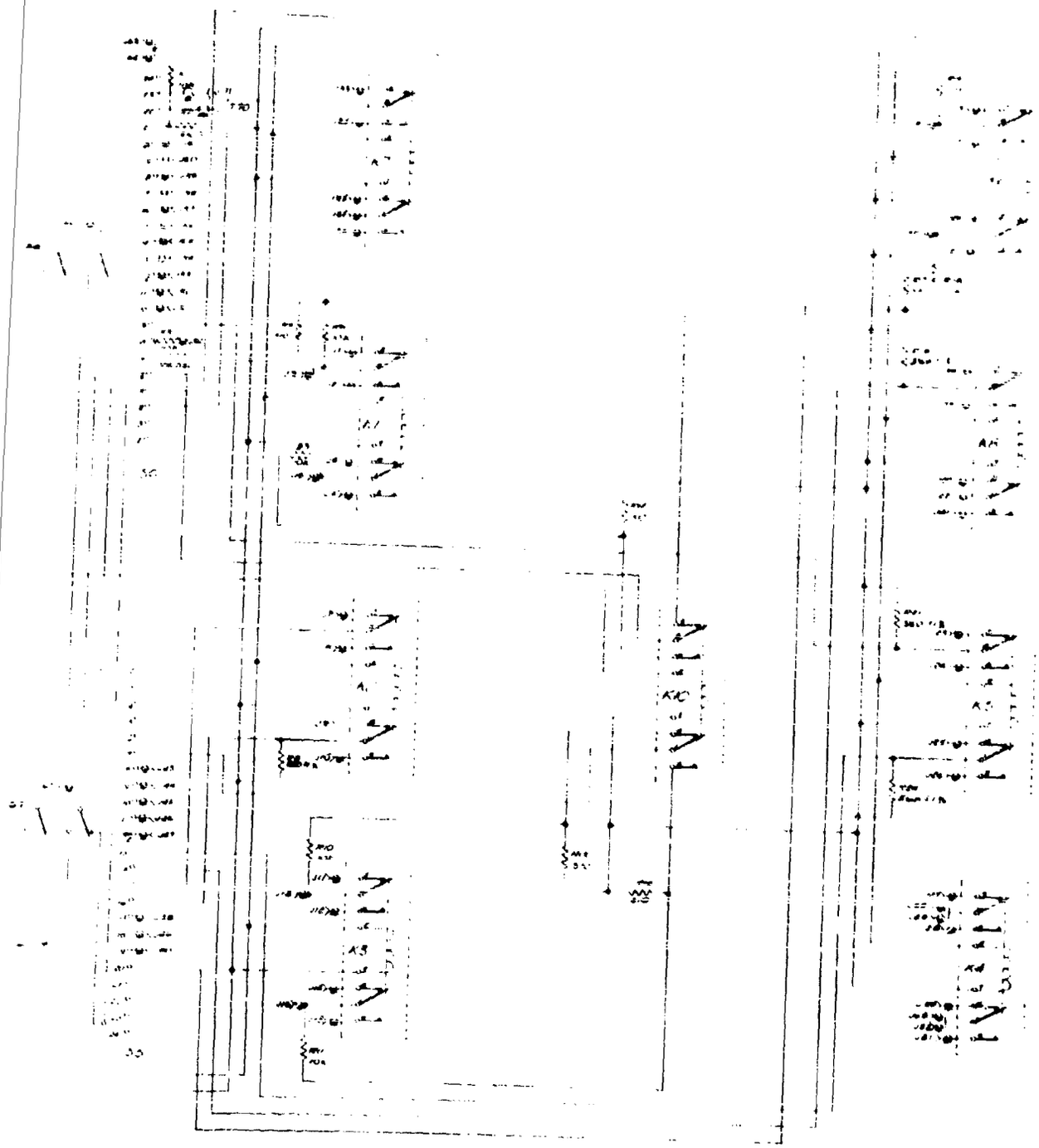
Fig. A-35 Relay Board





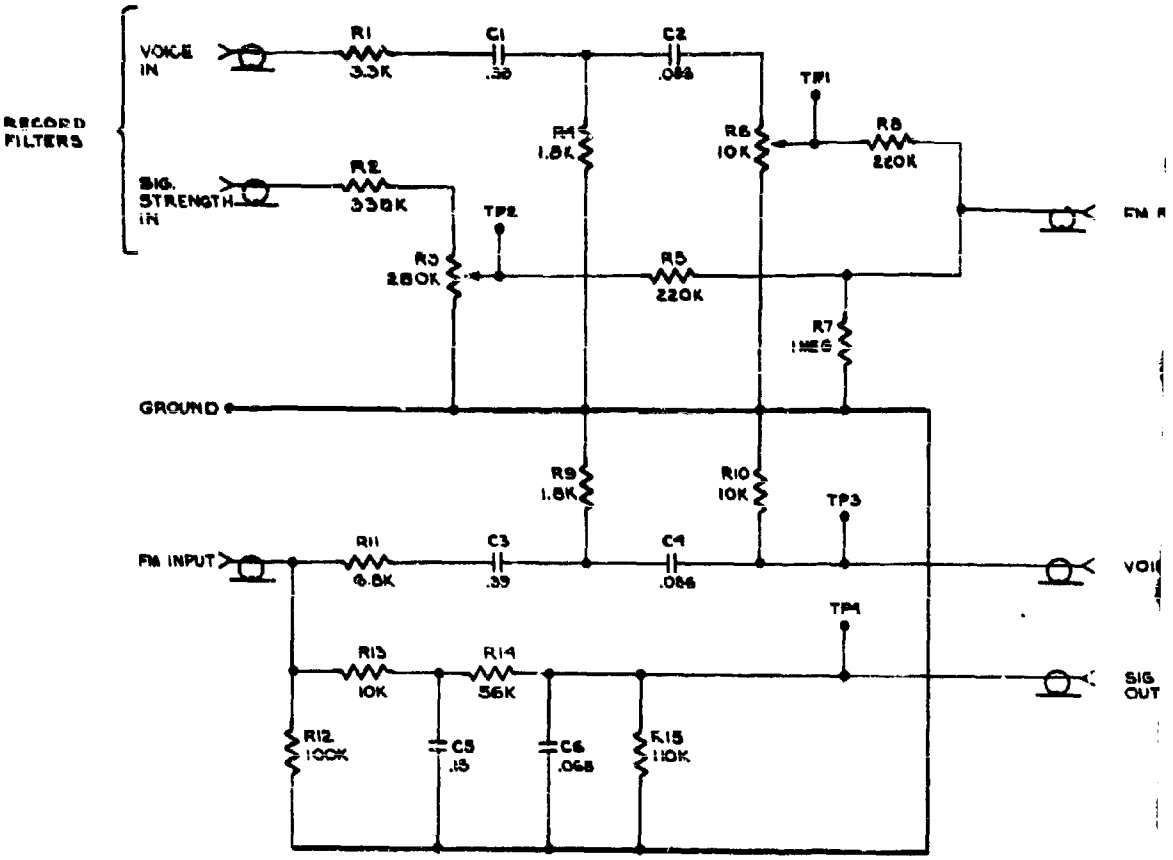






B

Fig. A-36 Monitor Panel

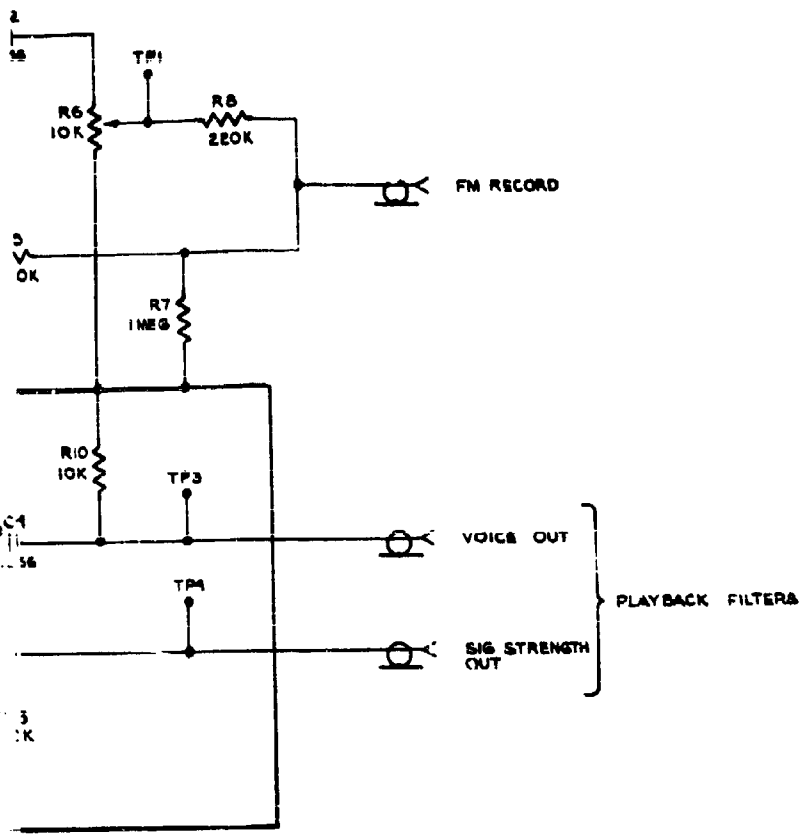


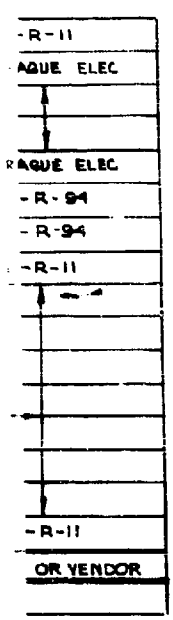
REF DES	PART NAME VALUE & TOLERANCE	PART NO.	SPEC. OR VENDOR
R14	RESISTOR COMP 56K, 1/4 WATT, 5% TOL	RC07GF563J	MIL-R-11
C6	CAPACITOR .068 UF 100V 10%	96P6839154	SPRAGUE ELEC.
C5	.15 UF	96P1549154	↕
C2, 4	.036 UF	96P3639154	↕
C1, 3	CAPACITOR .39 UF 100V 10%	96P3949154	SPRAGUE ELEC.
R6	POTENTIOMETER 10K	RV4LAYSA103A	MIL-R-94
R3	POTENTIOMETER 250K	RV4LAY50254A	MIL-R-94
R16	RESISTOR, COMP 110K 1/4 WATT, 5% TOL	RC07GF114J	MIL-R-11
R12	100K	RC07GF104J	↕
R11	6.8K	RC07GF682J	↕
R7	1 MEG	RC07GF105J	↕
R 10, 13	10K	RC07GF103J	↕
R5, 8	220K	RC07GF224J	↕
R4, 9	1.8K	RC07GF182J	↕
R2	330K	RC07GF334J	↕
R1	RESISTOR COMP 3.3K 1/4 WATT, 5% TOL	RC07GF332J	MIL-R-11

REFERENCE COMPONENTS LIST

NOTES:
1. ALL RESISTANCE VALUES IN
2. ALL CAPACITANCE VALUES

A



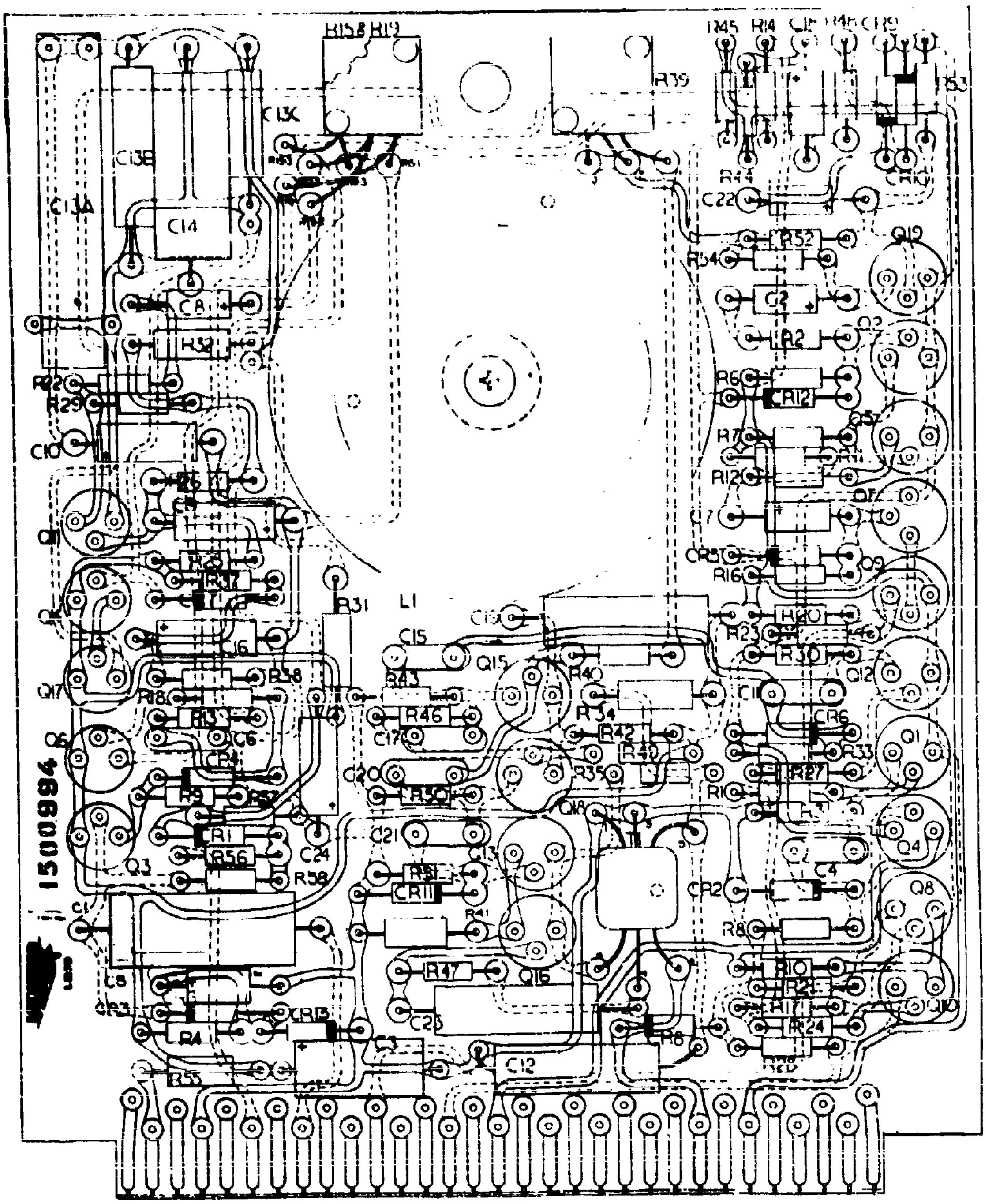


B

2. ALL CAPACITANCE VALUES IN MICRO FARADS.
1. ALL RESISTANCE VALUES IN OHMS (K=1000) 1/4 WATT 5% TOL.

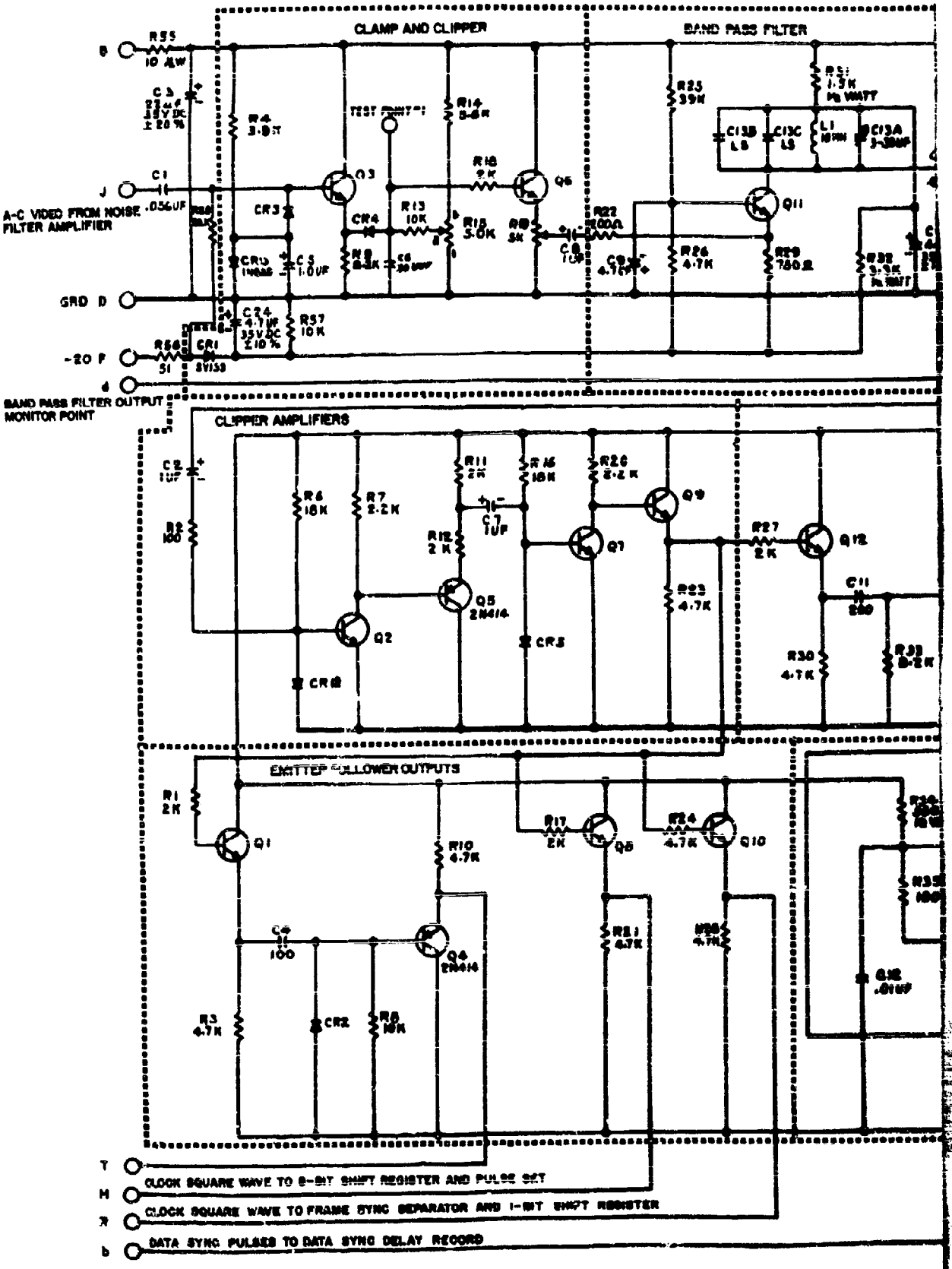
NOTES:

Fig. A-37 Signal Strength and Voice Record and Reproduce Filters

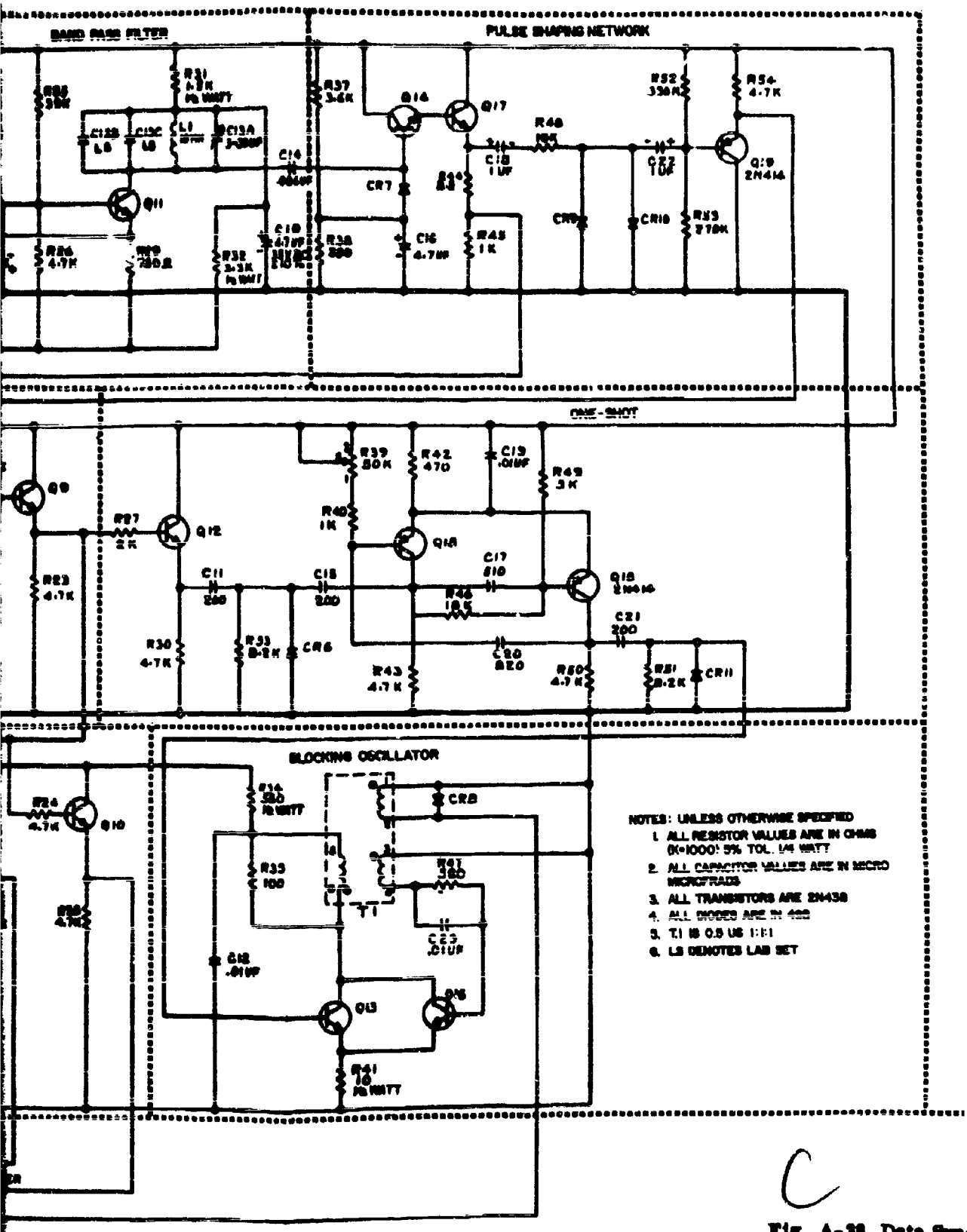


PARTS LIST

Reference Designation	[illegible] No.	Vendor or MIL Spec.
C1, 14	[illegible]	Sprague Elec. Co., North Adams, Mass.
C2, 7, 8, 10	[illegible]	Sprague Elec. Co., North Adams, Mass.
C3	[illegible]	[illegible]
C4	[illegible]	El Menco, Los Angeles, Calif.
C5, [illegible]	[illegible]	Sprague Elec. Co., North Adams, Mass.
C6	[illegible]	El Menco, Los Angeles, Calif.
C9, 10, 16, [illegible]	[illegible]	Sprague Elec. Co., North Adams, Mass.
C11, 18, [illegible]	[illegible]	El Menco, Los Angeles, Calif.
C12, 19, 20	[illegible]	Sprague Elec. Co., North Adams, Mass.
C13A	[illegible]	JFD Electronics, Brooklyn [illegible], N.Y.
C13B	[illegible]	El Menco, Los Angeles, Calif.
C13C	[illegible]	El Menco, Los Angeles, Calif.
C17	[illegible]	El Menco, Los Angeles, Calif.
C[illegible]	[illegible]	El Menco, Los Angeles, Calif.
CR1	[illegible]	Transitron, Wakefield, Mass.
CR2 thru 8, 11, 1[illegible]	[illegible]	[illegible], Danvers, Mass.
CR9, 10, 12	[illegible]	Pacific Semiconductor, Culver City, Calif.
Q1, 2, 3, [illegible] thru 10, 12, 13, 14, 16, 17	[illegible]	[illegible], Danvers, Mass.
Q[illegible], 5, 15, 18, 19	[illegible]	[illegible], [illegible], Mass.
Q11	[illegible]	Texas Inst., Dallas
R1, 11, 12, 17, 1[illegible], [illegible], [illegible]	[illegible]	MIL-R-11
R[illegible], [illegible]	[illegible]	MIL-R-11
R[illegible], 10, [illegible], [illegible], [illegible], [illegible], [illegible]		
[illegible], [illegible], [illegible]	[illegible]	MIL-R-11
R[illegible]	[illegible]	MIL-R-11
R[illegible], [illegible], [illegible]	[illegible]	MIL-R-11
R[illegible], [illegible]	[illegible]	MIL-R-11
R[illegible], 1[illegible], [illegible], [illegible]	[illegible]	MIL-R-11
R[illegible], [illegible], [illegible]	[illegible]	MIL-R-11
R[illegible]	[illegible]	MIL-R-11
R[illegible], 1[illegible]	[illegible]	Daystrom Pacific, Santa Monica, Calif.
R[illegible]	[illegible]	MIL-R-11
R[illegible], [illegible]	[illegible]	MIL-R-11
R[illegible]	[illegible]	MIL-R-11
R[illegible]	[illegible]	MIL-R-11
R[illegible]	[illegible]	MIL-R-11
R[illegible]	[illegible]	MIL-R-11
R[illegible]	[illegible]	Daystrom Pacific, Santa Monica, Calif.
R[illegible]	[illegible]	MIL-R-11
R[illegible], [illegible]	[illegible]	MIL-R-11
R[illegible]	[illegible]	MIL-R-11
R[illegible]	[illegible]	MIL-R-11
R[illegible]	[illegible]	MIL-R-11
R[illegible]	[illegible]	MIL-R-11
R[illegible]	[illegible]	MIL-R-11
R[illegible]	[illegible]	MIL-R-11
R[illegible]	[illegible]	MIL-R-11
R[illegible]	[illegible]	MIL-R-11
T1	[illegible]	[illegible] Co., Santa Monica, Calif.
L1	[illegible]	[illegible] Transformer, Brooklyn [illegible], N.Y.

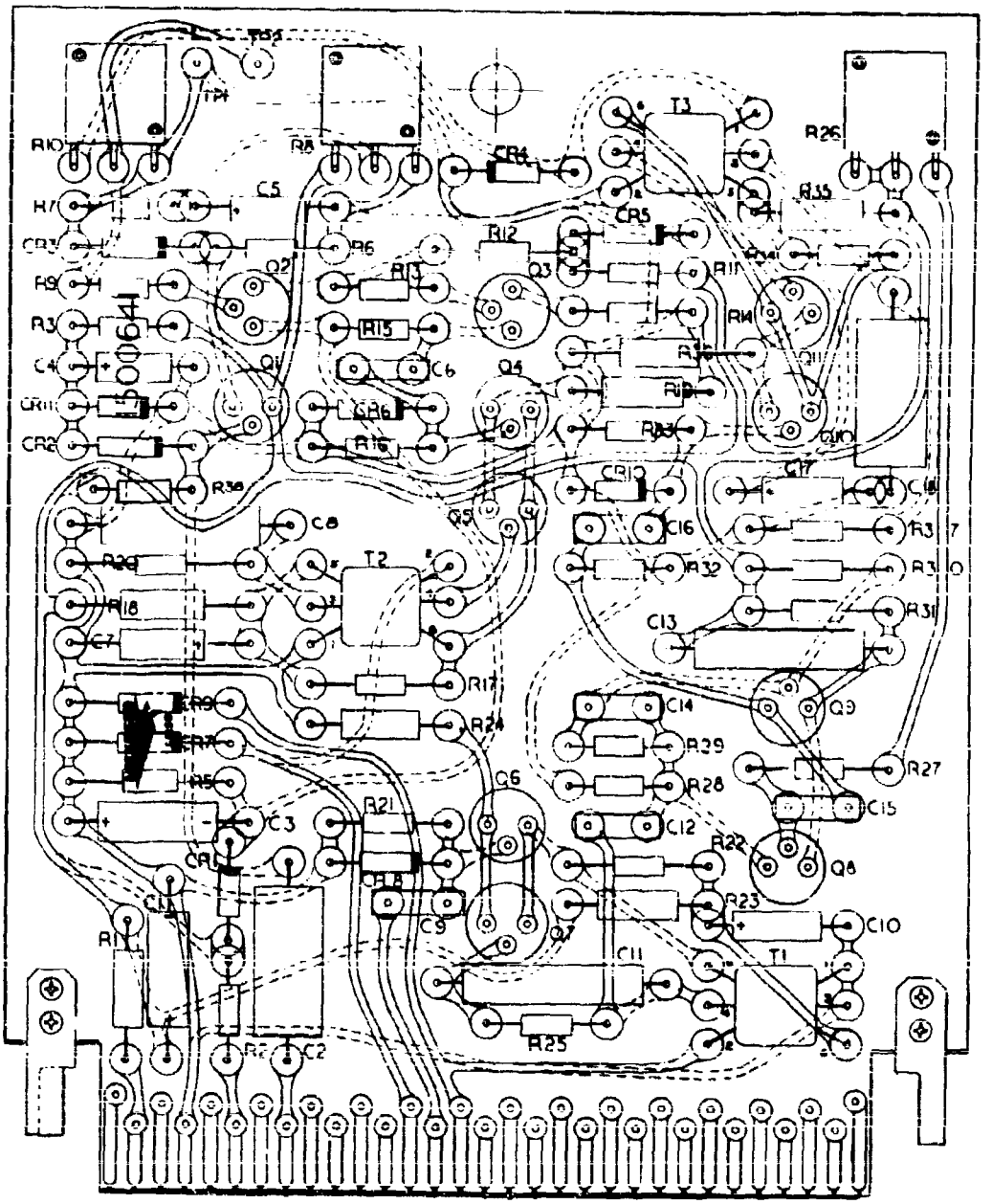

CLAMP AND CLIPPER
BAND PASS FILTER
A-C VIDEO FROM NOISE FILTER AMPLIFIER
GRD D
-20 P
BAND PASS FILTER OUTPUT MONITOR POINT
CLIPPER AMPLIFIERS
EMITTER FOLLOWER OUTPUTS
T CLOCK SQUARE WAVE TO 8-BIT SHIFT REGISTER AND PULSE SET
H CLOCK SQUARE WAVE TO FRAME SYNC SEPARATOR AND 1-BIT SHIFT REGISTER
b DATA SYNC PULSES TO DATA SYNC DELAY RECORD

B



C

Fig. A-38 Data Sync Separator, G-A

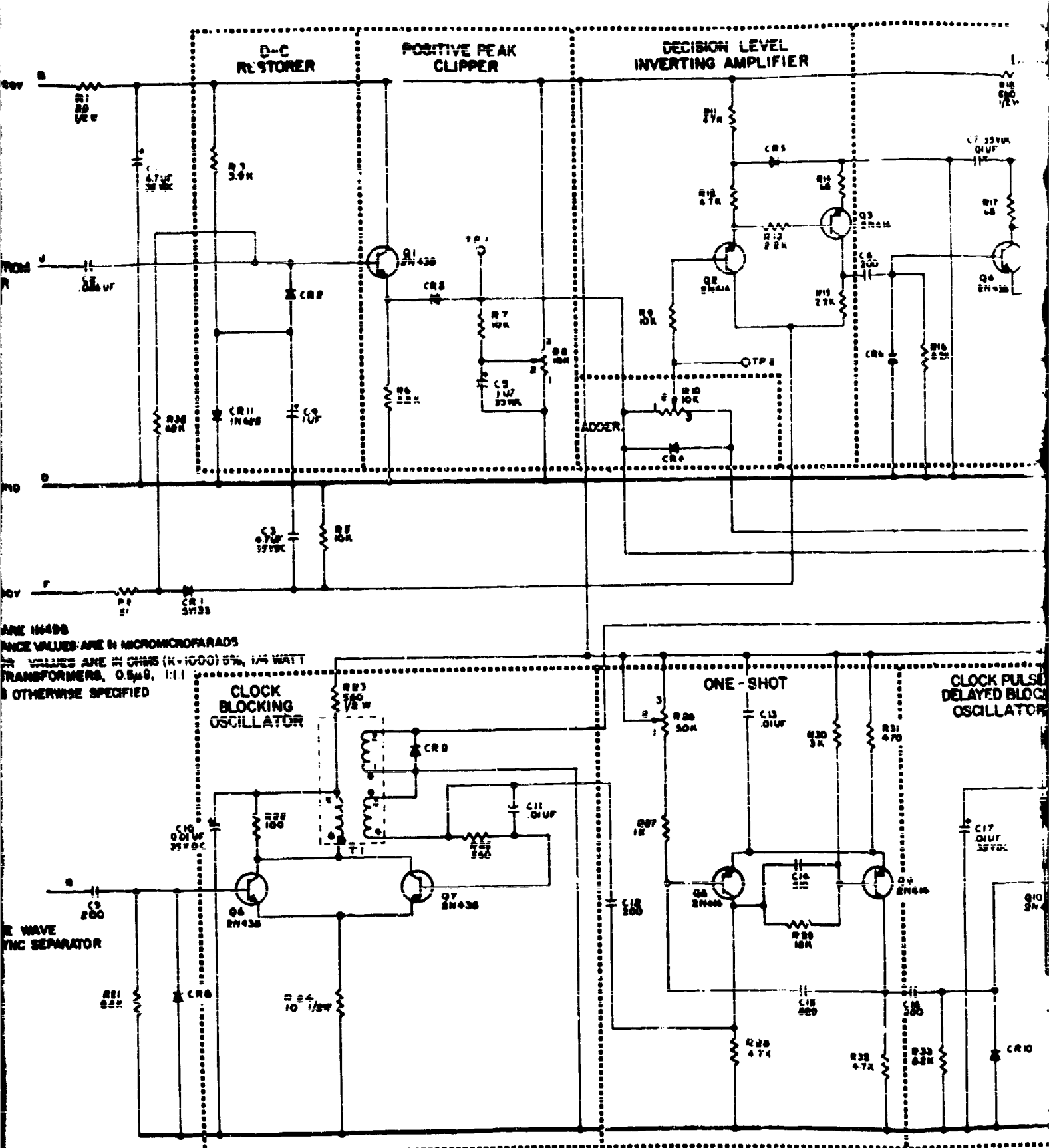


1. ALL DIODES ARE IN456
2. ALL CAPACITANCE VALUES ARE
3. ALL RESISTOR VALUES ARE
4. ALL PULSE TRANSFORMERS,

NOTES: UNLESS OTHERWISE SPECIFIED

PARTS LIST

A


D-C
RESTORER
POSITIVE PEAK
CLIPPER
DECISION LEVEL
INVERTING AMPLIFIER
ADDER
CLOCK
BLOCKING
OSCILLATOR
ONE-SHOT
CLOCK PULSE
DELAYED BLOCK
OSCILLATOR
ARE IN MICROMICROFARADS
ARE IN OHMS (K=1000) 5%, 1/4 WATT
TRANSFORMERS, 0.5μ9, 1:1:1
OTHERWISE SPECIFIED
E WAVE
NC SEPARATOR

B

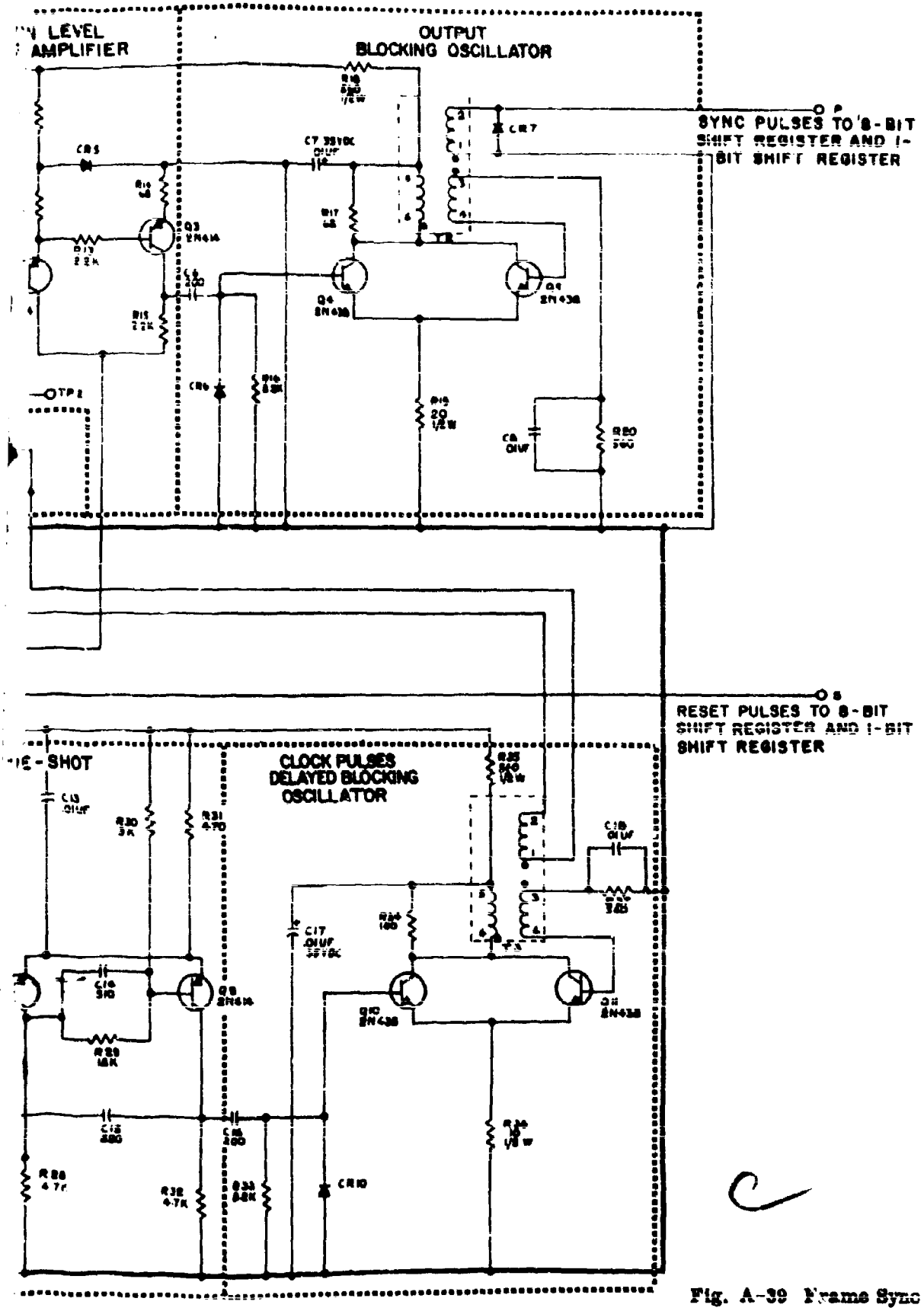
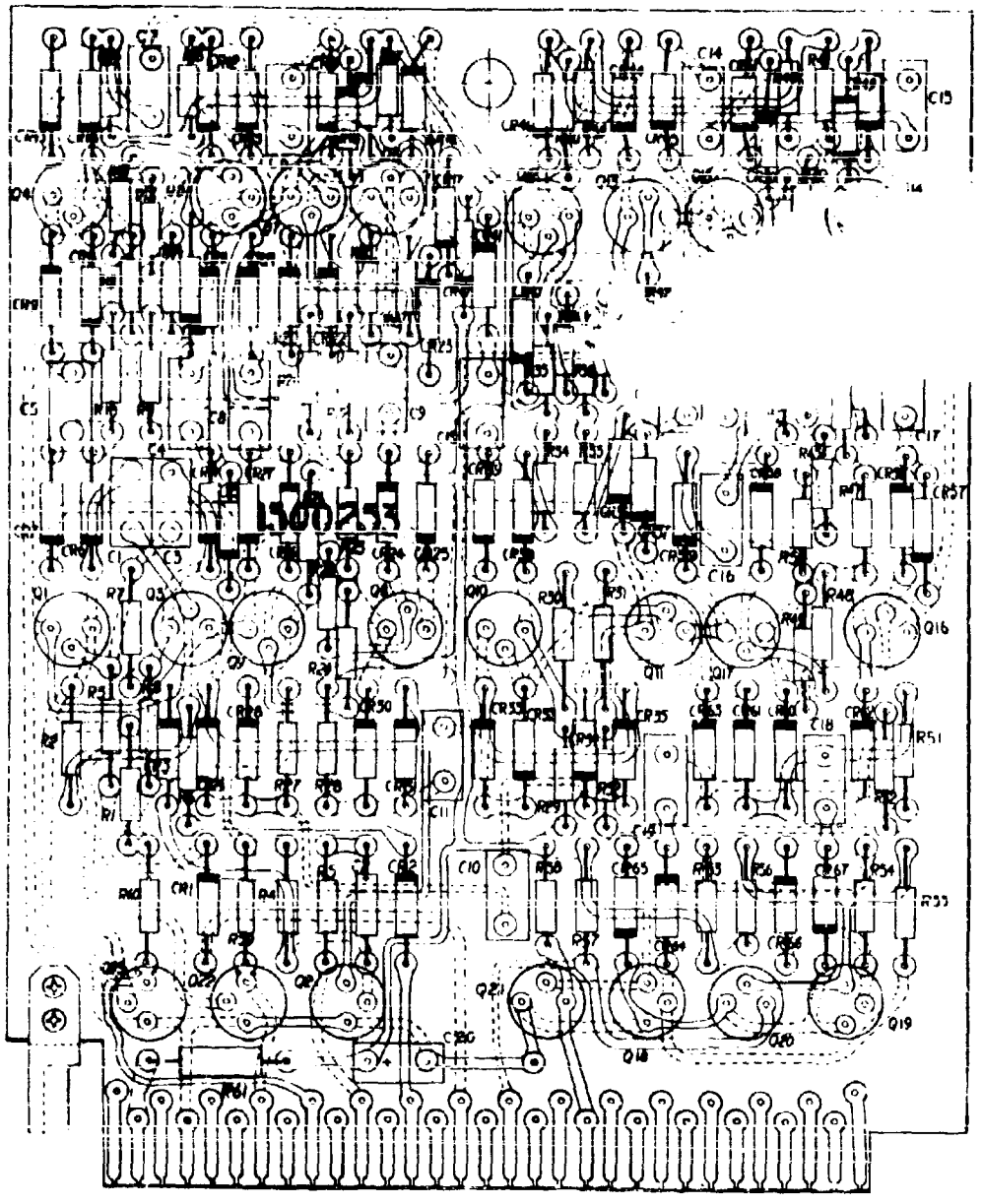
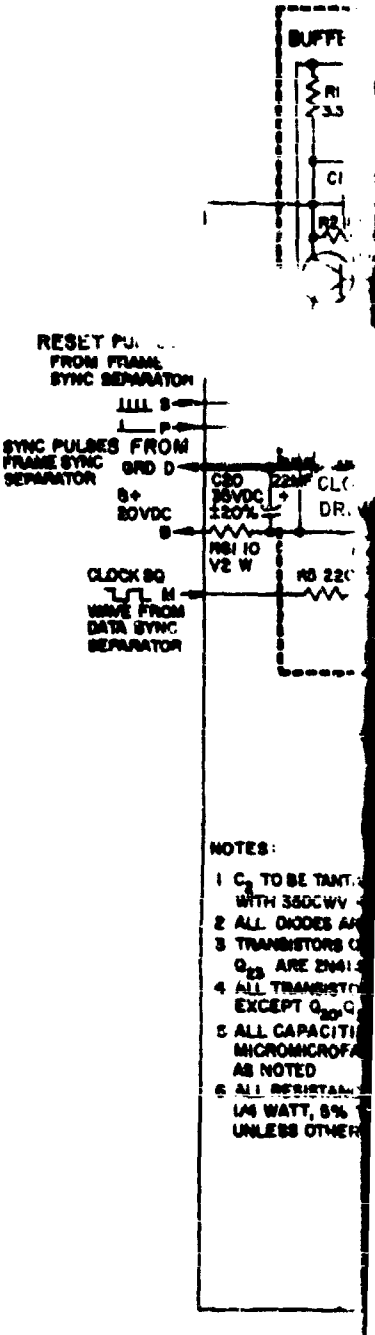


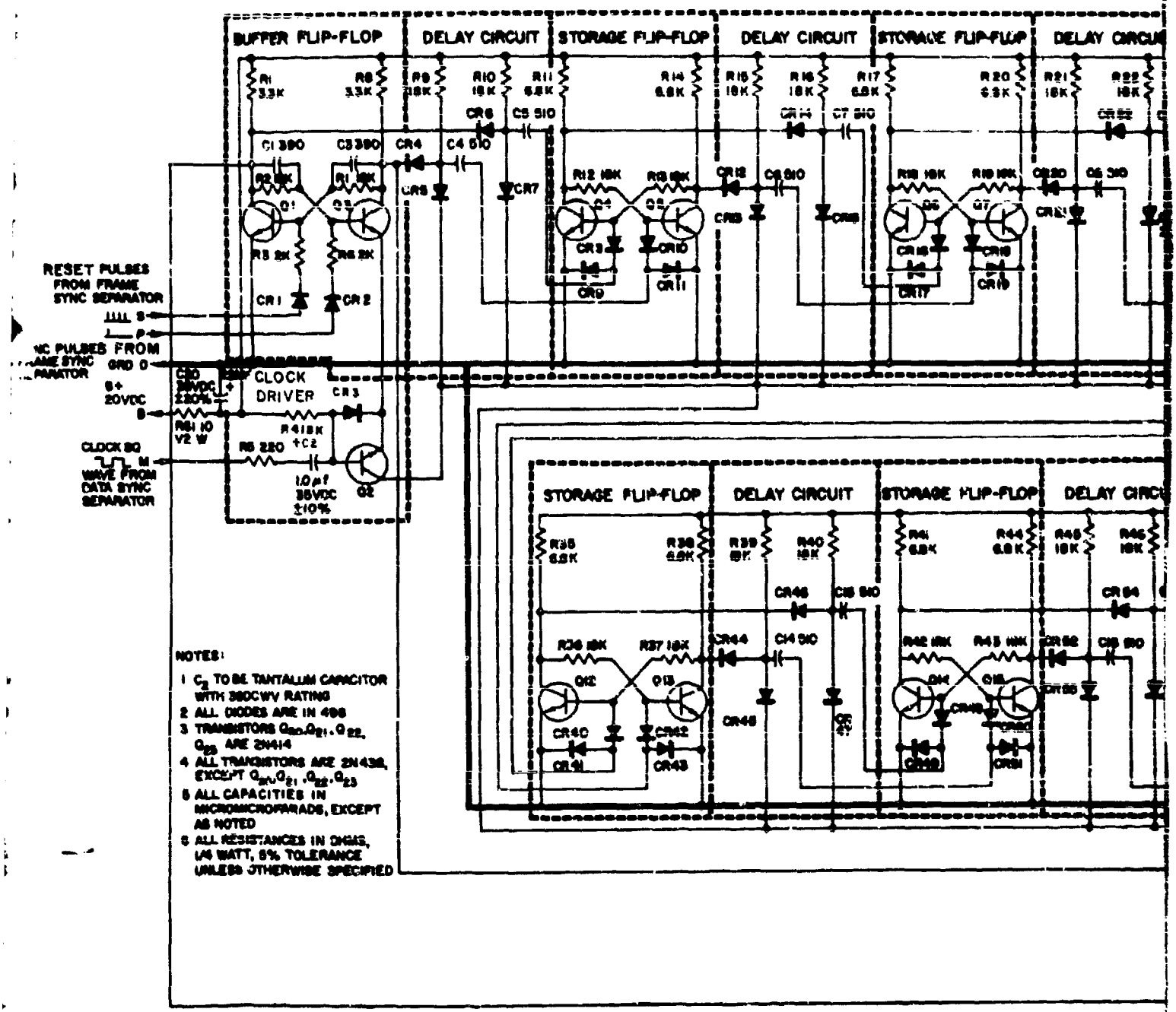
Fig. A-39 Frame Sync Separator, G-A





PARTS LIST

Reference Designation	Part No.	Vendor or MIL Spec.
C1, 3		
C2		
C4 thru 10		
C30		
CR1 thru 67		
Q1 thru 19		
Q20 thru 23		
R1 +		
R2, 4, 9, 10, 12, 13, 14, 15, 19, 20, 21, 22, 24, 25, 27, 28, 29, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 42, 43, 44, 45, 46, 47, 48, 49, 51, 52, 53		
R3 +		
R5 +		
R11, 16, 17, 30, 23, 26, 41, 50, 54, 55, 56		
R8		


BUFFER FLIP-FLOP
DELAY CIRCUIT
STORAGE FLIP-FLOP
DELAY CIRCUIT
STORAGE FLIP-FLOP
DELAY CIRCUIT
RESET PULSES FROM FRAME SYNC SEPARATOR
S
P
SYNC PULSES FROM FRAME SYNC SEPARATOR
GRD
B+ 20VDC
B
CLOCK SQ WAVE FROM DATA SYNC SEPARATOR
M
CLOCK DRIVER
STORAGE FLIP-FLOP
DELAY CIRCUIT
STORAGE FLIP-FLOP
DELAY CIRCUIT
NOTES:
1 C_2 TO BE TANTALUM CAPACITOR WITH 350CWV RATING
2 ALL DIODES ARE IN 498
3 TRANSISTORS $Q_{20}, Q_{21}, Q_{22}, Q_{23}$ ARE 2N414
4 ALL TRANSISTORS ARE 2N438, EXCEPT $Q_{20}, Q_{21}, Q_{22}, Q_{23}$
5 ALL CAPACITIES IN MICROMICROFARADS, EXCEPT AS NOTED
6 ALL RESISTANCES IN OHMS, 1/4 WATT, 5% TOLERANCE UNLESS OTHERWISE SPECIFIED

B

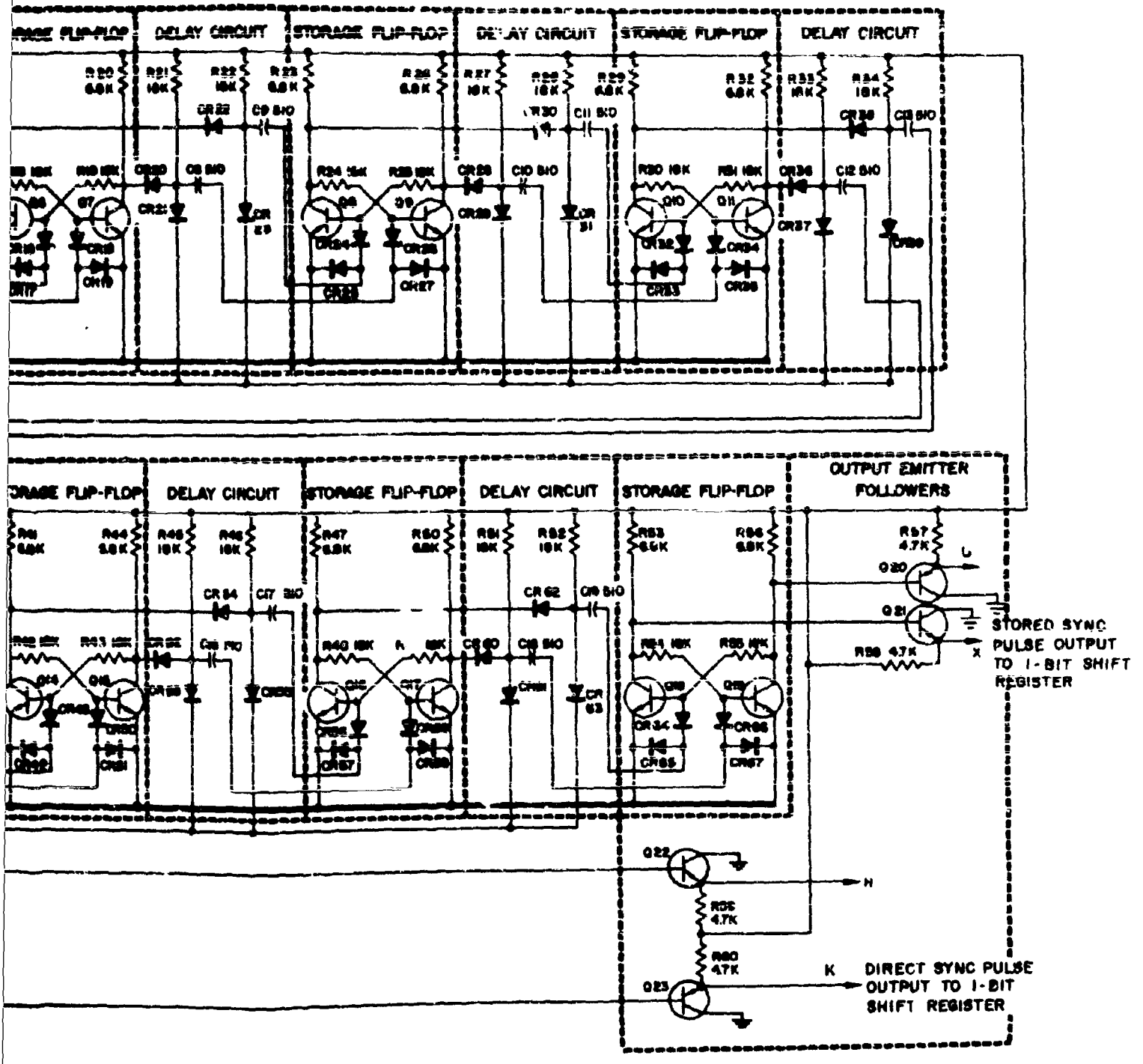
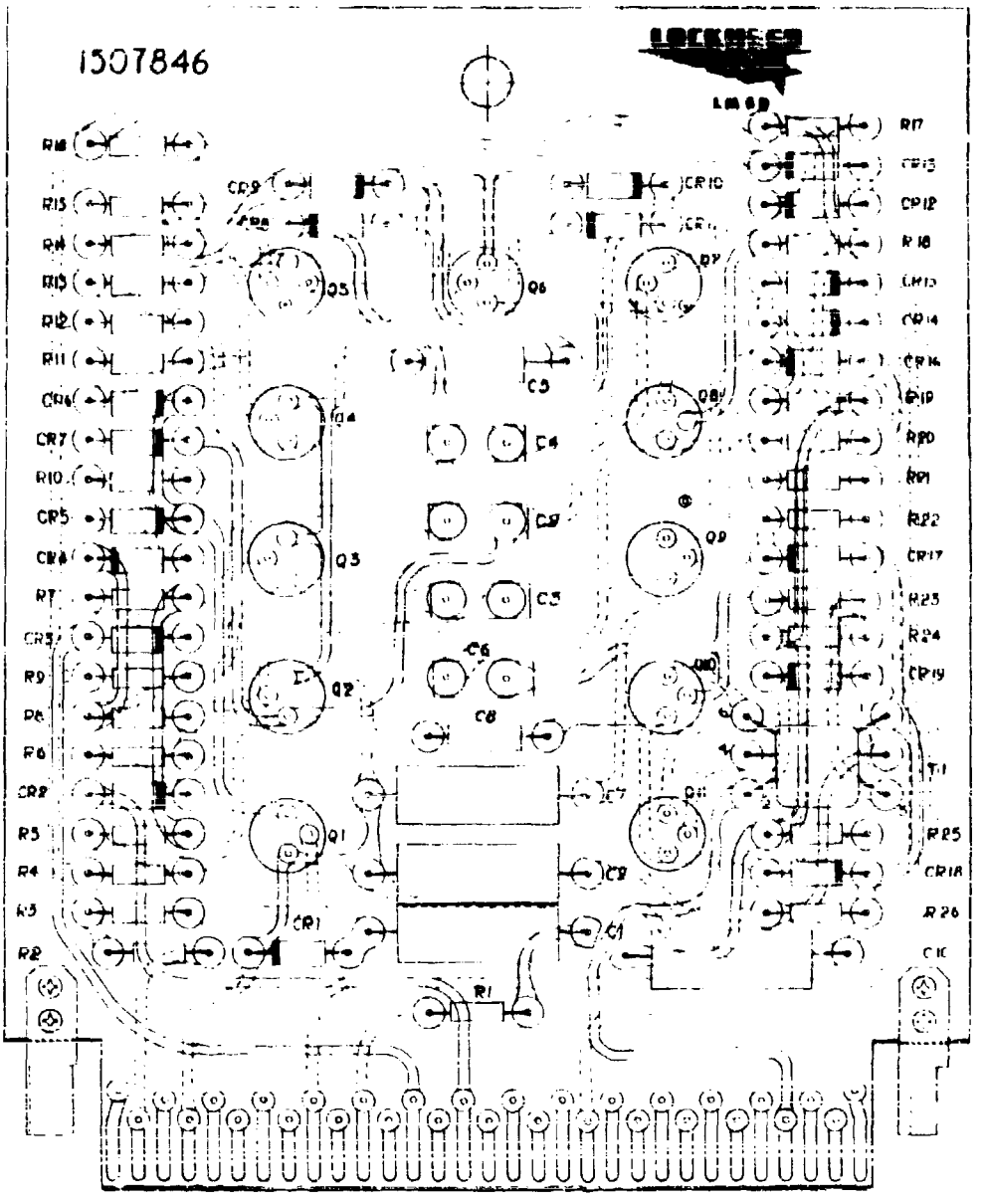
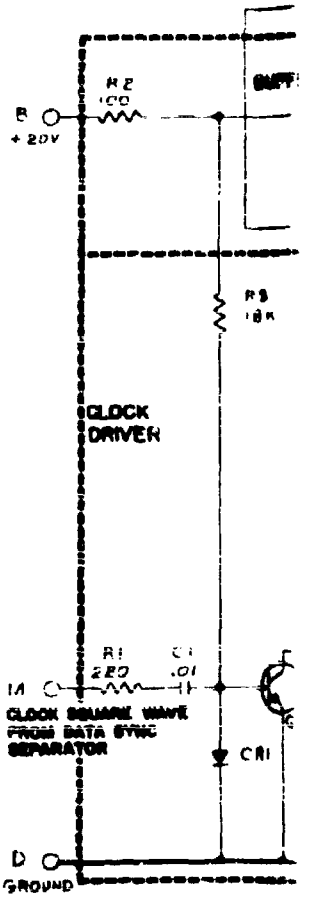


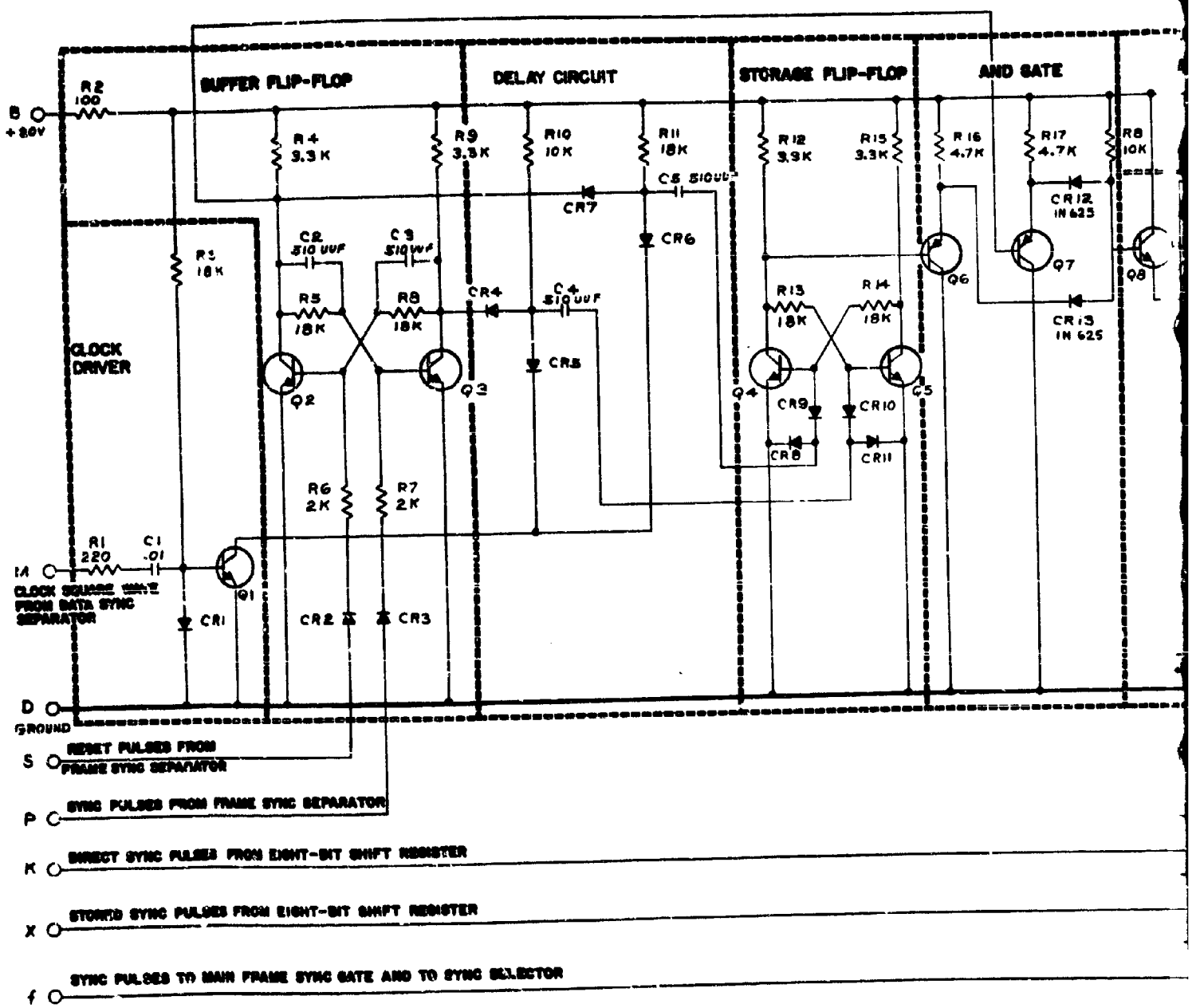
Fig. A-40 Eight-Bit Shift Register, G-A



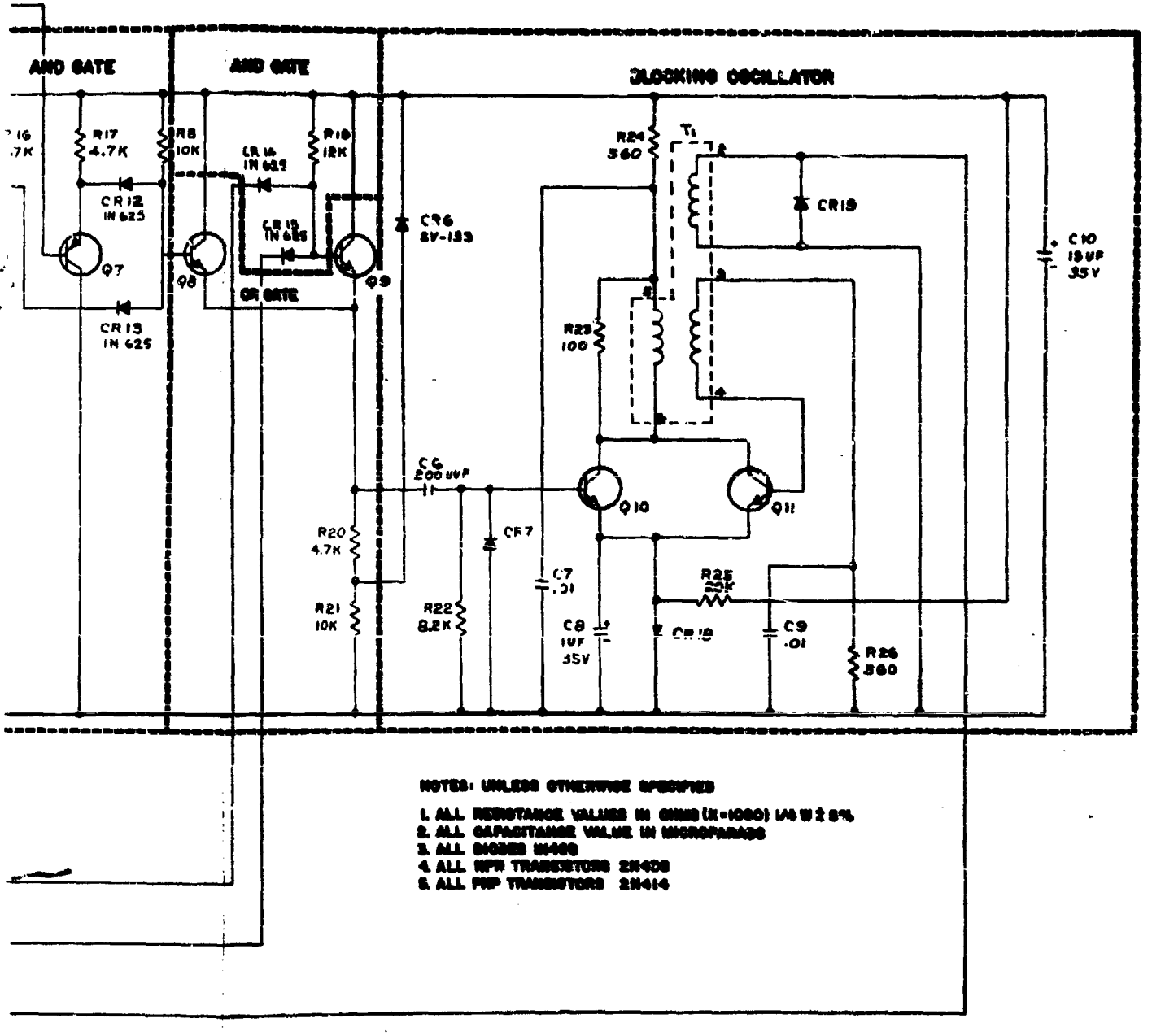


PARTS LIST

Reference Designation	Part No.	Vendor or Mil. Spec.
C1, 7, 9	CS-95A1EB104K	Sprague Electric Co., North Adams, Mass.
C2 thru 5	DM15F911J	El Monte, Los Angeles, Calif.
C6	DM15F561J	El Monte, Los Angeles, Calif.
C8	196D106X9035A2	Sprague Electric Co., North Adams, Mass.
C10	196D105X9035B1	Sprague Electric Co., North Adams, Mass.
CR1 thru 11, 18, 19	1N456	CBS-Hytron, Danvers, Mass.
CR12 thru 16, 17	1N458	Pacific Semiconductor, Culver City, Calif.
CR18	SV128	Transitron, Wakefield, Mass.
Q1 thru 5, 8 thru 11	2N438	CBS-Hytron, Danvers, Mass.
Q6, 7	2N414	Raytheon Mfg. Co., Newton, Mass.
R1	RC07GF221J	MIL-R-11
R2, 20	RL07GF101J	MIL-R-11
R3, 5, 8, 10, 11, 13, 14	RC07GF103J	MIL-R-11
R4, 6, 12, 15	RC07GF682J	MIL-R-11
R16, 7	RC07GF392J	MIL-R-11
R18, 17, 00	RC07GF473J	MIL-R-11
R19, 21	RC07GF102J	MIL-R-11
R19	RC07GF1.2MJ	MIL-R-11
R22	RC07GF682J	MIL-R-11
R24, 26	RC07GF561J	MIL-R-11
R25	RC07GF303J	MIL-R-11
T1	10T-6-1111	Quinsana Co., Bara Mesa, Calif.


BUFFER FLIP-FLOP
DELAY CIRCUIT
STORAGE FLIP-FLOP
AND GATE
CLOCK DRIVER
B
+20V
R2 100
R4 3.3K
R9 3.3K
R10 10K
R11 18K
C5 510UUF
CR7
CR6
R12 3.9K
R15 3.3K
R16 4.7K
R17 4.7K
R8 10K
CR12 IN625
CR13 IN625
Q6
Q7
Q8
R3 18K
C2 510 UUF
C3 510 UUF
R5 18K
R8 18K
CR4
C4 510 UUF
CR5
R13 18K
R14 18K
Q2
Q3
Q4
Q5
CR9
CR10
CR8
CR11
R6 2K
R7 2K
R1 220
C1 .01
A
CLOCK SQUARE WAVE FROM DATA SYNC SEPARATOR
Q1
CR1
CR2
CR3
D
GROUND
S
RESET PULSES FROM FRAME SYNC SEPARATOR
P
SYNC PULSES FROM FRAME SYNC SEPARATOR
K
DIRECT SYNC PULSES FROM EIGHT-BIT SHIFT REGISTER
X
STORED SYNC PULSES FROM EIGHT-BIT SHIFT REGISTER
f
SYNC PULSES TO MAIN FRAME SYNC GATE AND TO SYNC SELECTOR

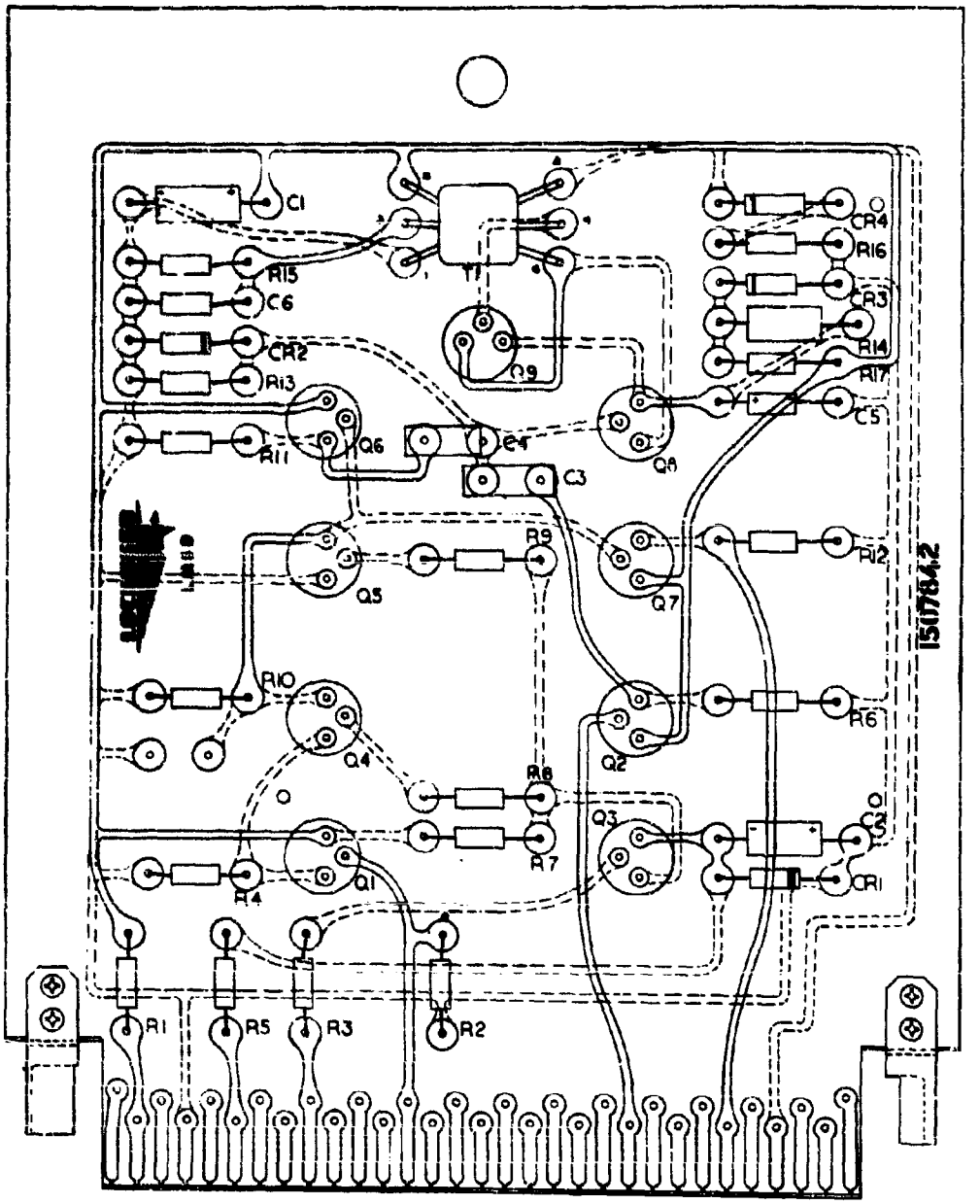
B



NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTANCE VALUES IN OHMS (K=1000) 1/4 W ± 5%
2. ALL CAPACITANCE VALUE IN MICROFARADS
3. ALL DIODES IN400
4. ALL NPN TRANSISTORS 2N408
5. ALL PNP TRANSISTORS 2N414

Fig. A-41 One-Bit Shift Register



GROUND D

MAIN FRAME SYNC FROM SYNC GATE Z

+20V B

SYNC PULSES FROM 1-BIT SHIFT REGISTER P

SUBCOM SYNC PULSES TO SYNC GATE d

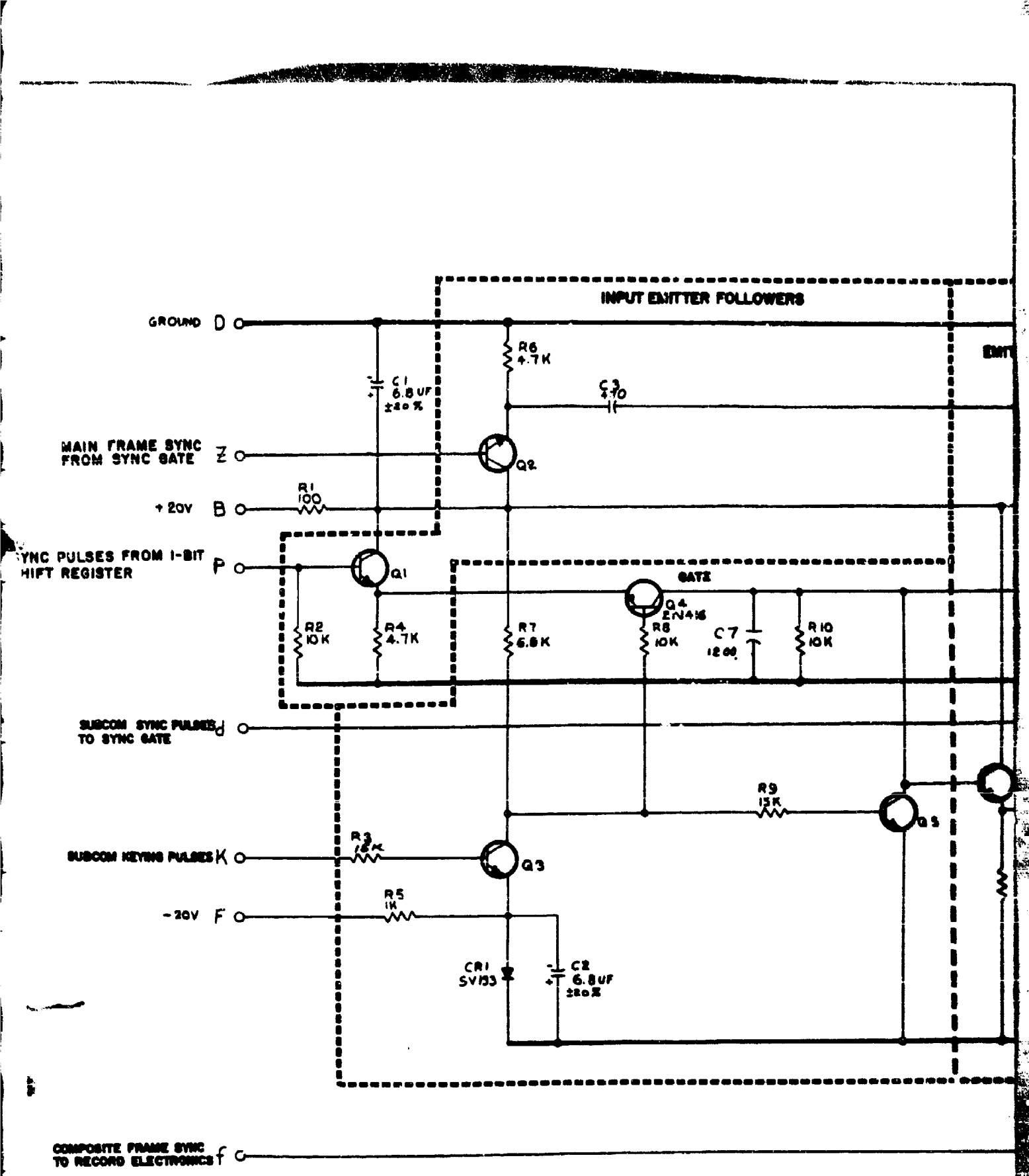
SUBCOM KEYING PULSES K

-20V F

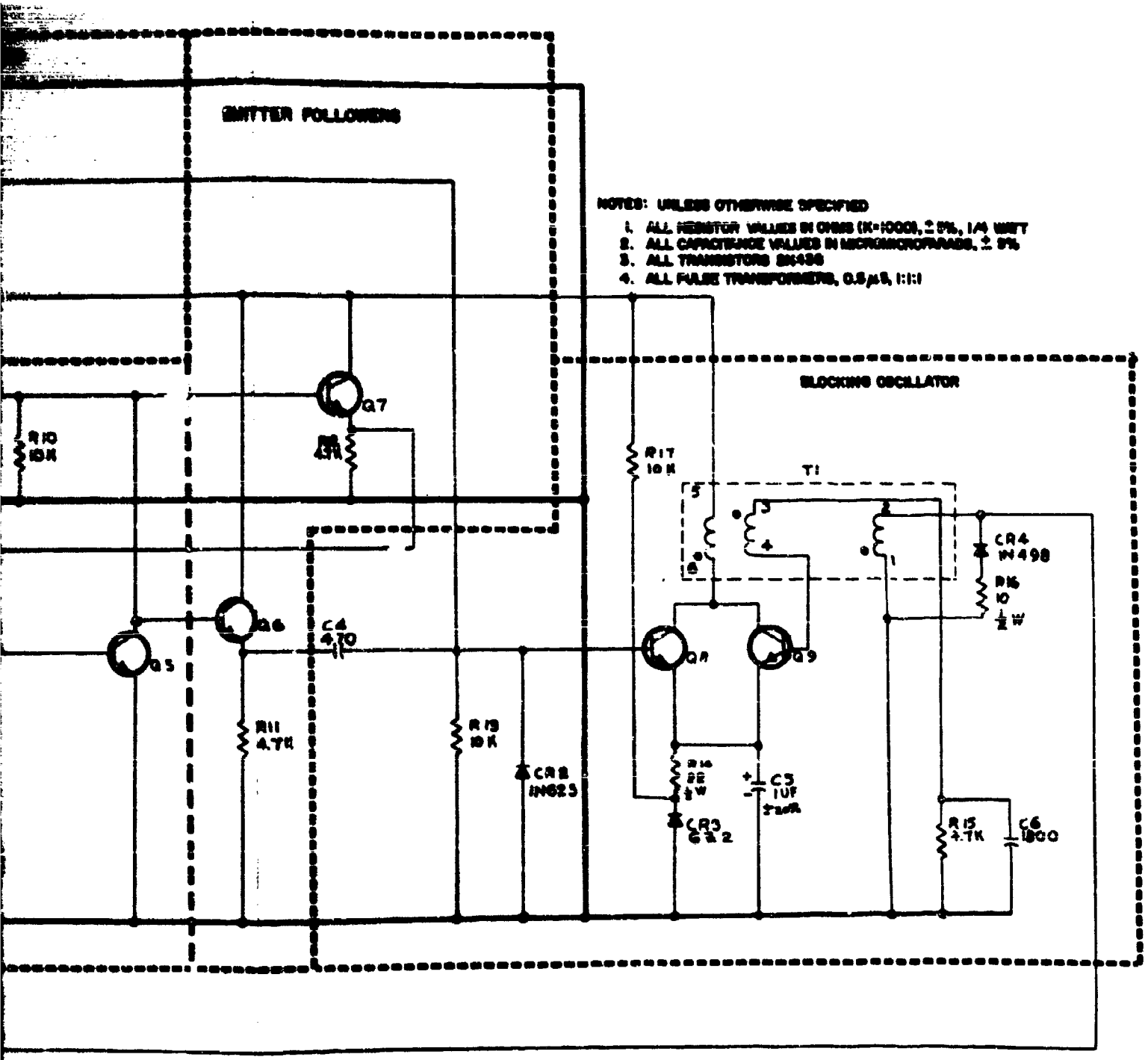
COMPOSITE FRAME SYNC TO RECORD ELECTRONICS f

PARTS LIST

Reference Designation	Part No.	Name and Description
C1		
C2		
C3		
C4		
C5		
C6		
CR1		
CR2		
CR4		
Q1, 2, 3, 4, 5, 6, 7, 8, 9		
R1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17		
T1		

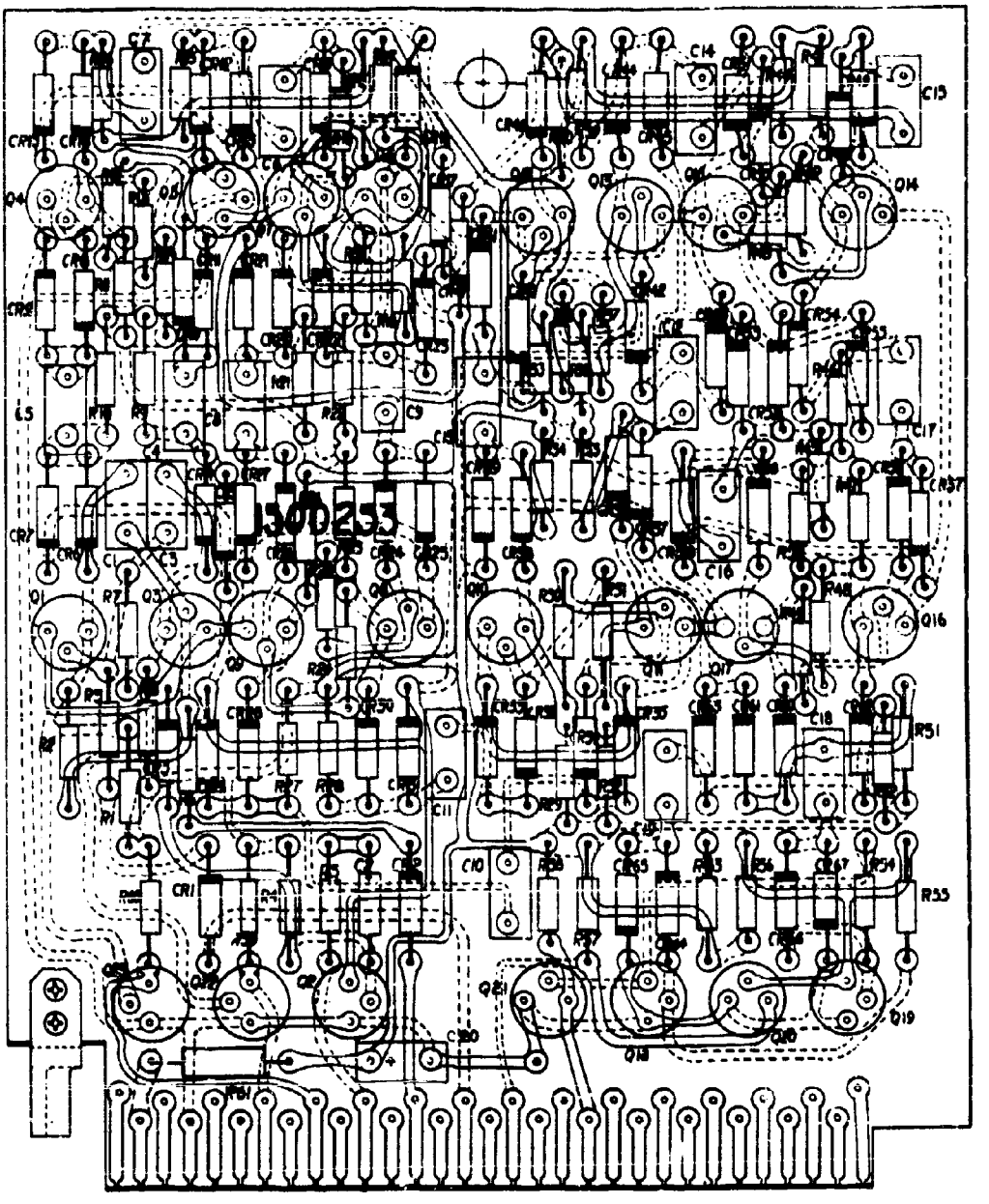

INPUT EMITTER FOLLOWERS
GROUND D
C1 6.8 UF ±20 %
R6 4.7K
C3 .10
MAIN FRAME SYNC FROM SYNC GATE Z
Q2
R1 100
+20V B
SYNC PULSES FROM 1-BIT SHIFT REGISTER P
Q1
GATE
Q4 2N416
R2 10K
R4 4.7K
R7 6.8K
R8 10K
C7 1200
R10 10K
SUBCOM SYNC PULSES TO SYNC GATE d
R9 13K
Q5
R3 12K
SUBCOM KEYING PULSES K
Q3
R5 1K
-20V F
CR1 SV133
C2 6.8 UF ±20 %
COMPOSITE FRAME SYNC TO RECORD ELECTRONICS f

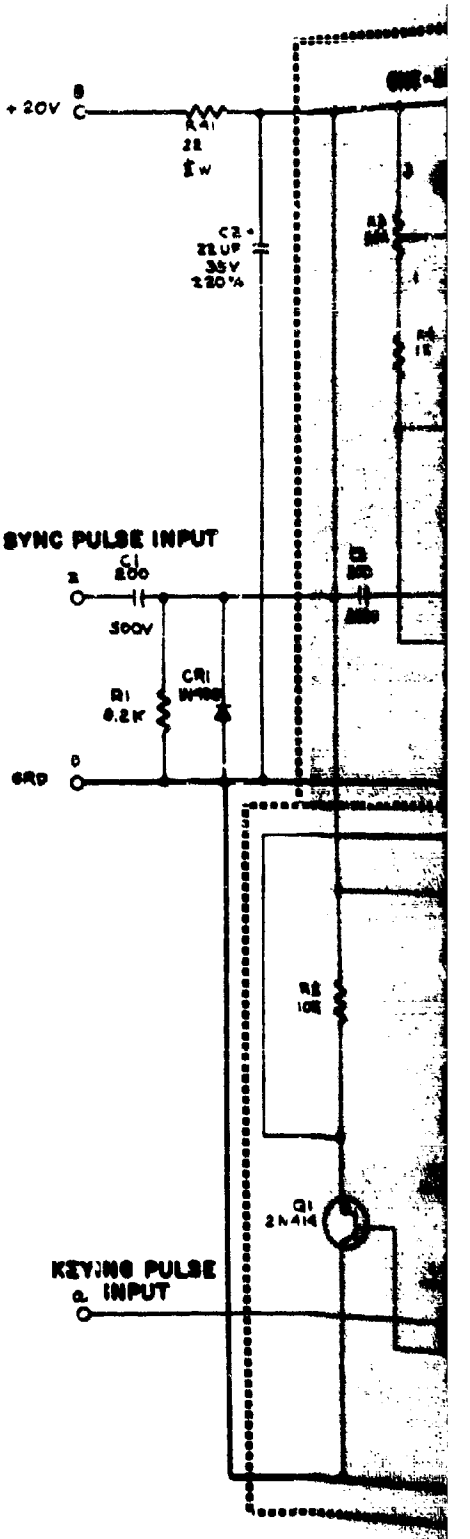
B



C

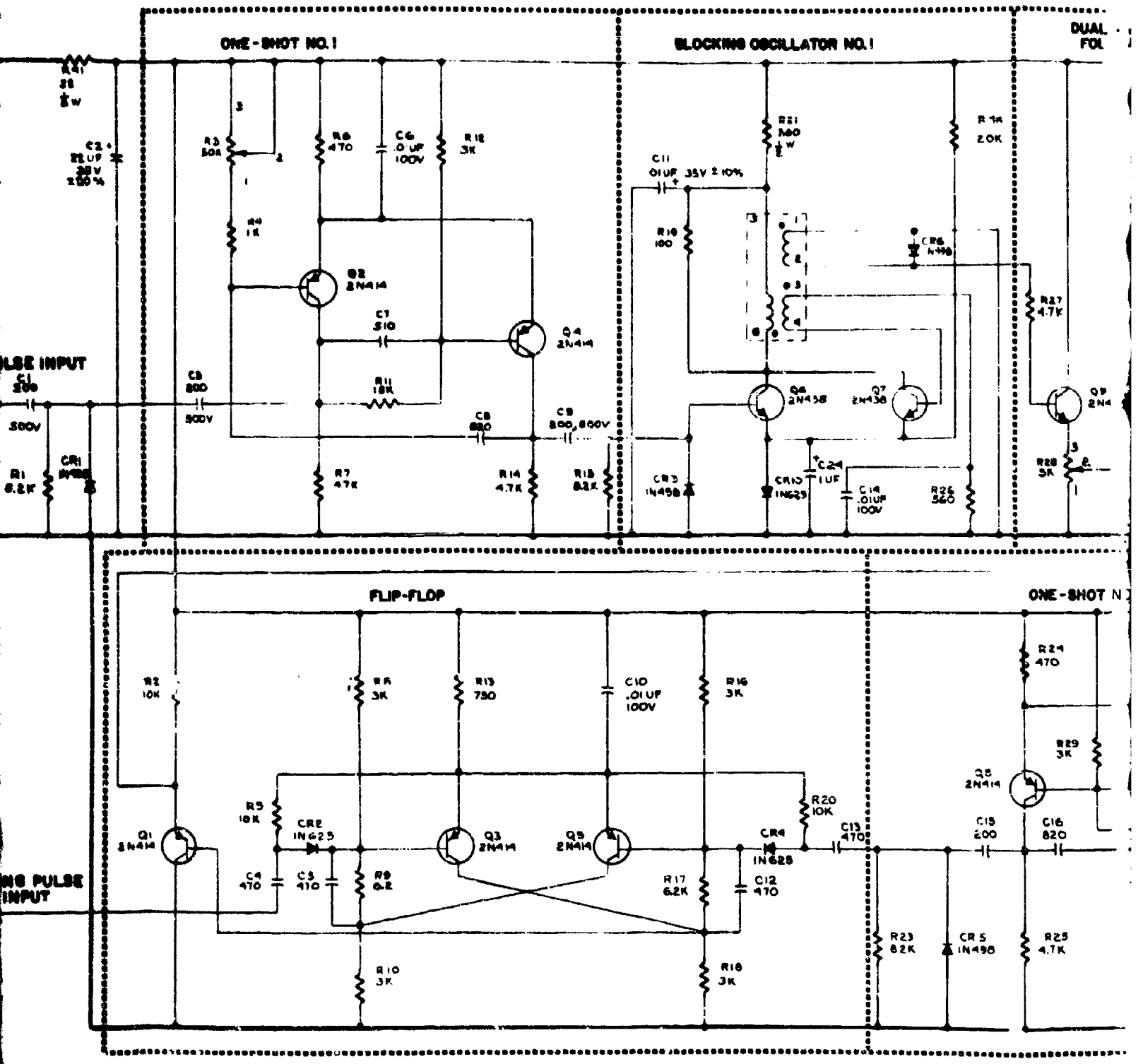
Fig. A-42 Sync Selector, G-A



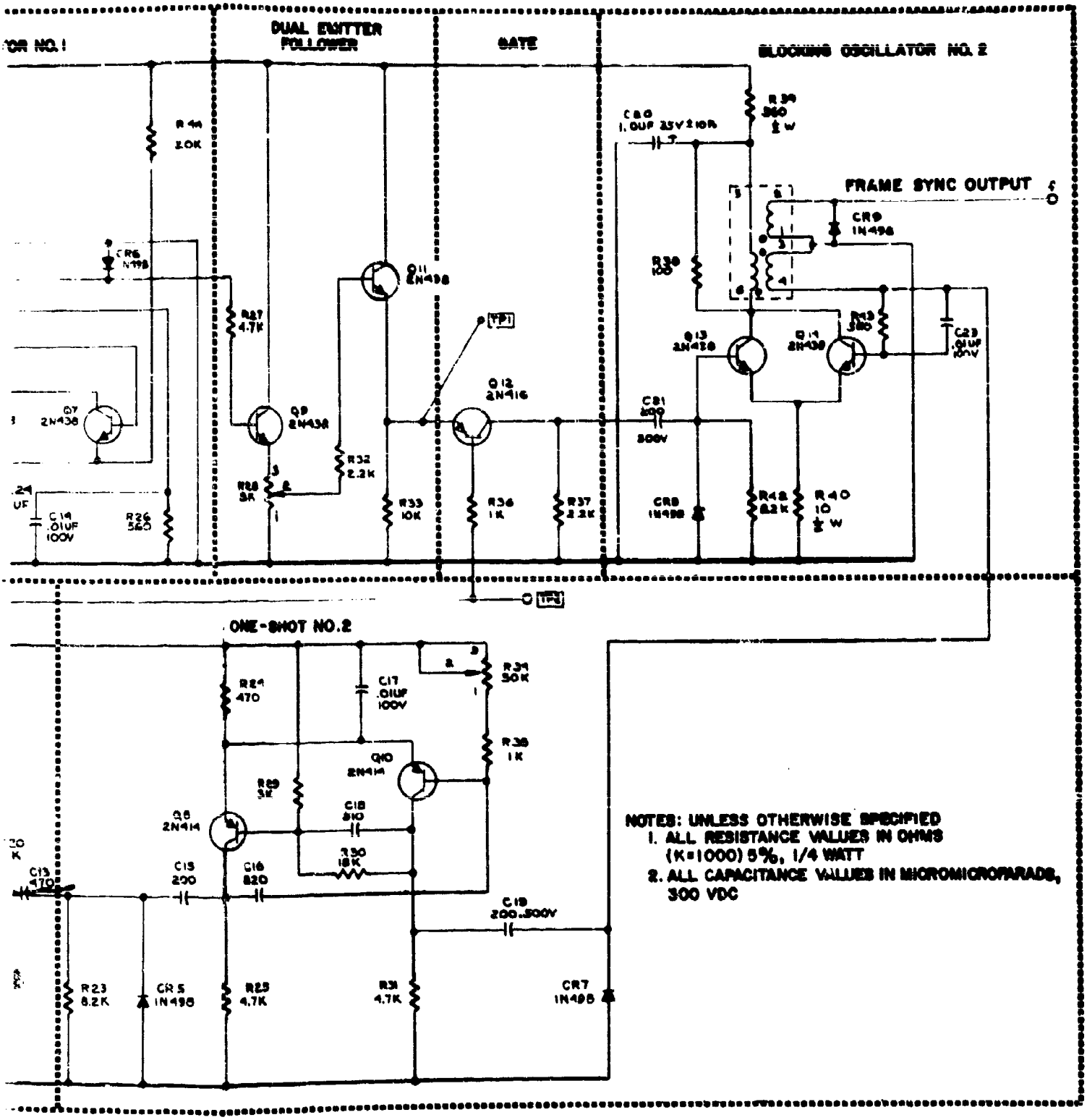


PARTS LIST

Reference Designation	Part No.	Vendor or Mil Spec.
C1.8	DM15F201J	El Monco. Los Angeles. Calif.
C2	130D163X9063A2	Sprague Electric Co., North Adams. Mass.
C4 thru 19	DM15F511J	El Monco. Los Angeles. Calif.
C20	130D226X9063B2	Sprague Electric Co., North Adams. Mass.
CR1 thru 47	1N480	CBS-Hytron. Danvers. Mass.
Q1 thru 15	2N438	CBS-Hytron. Danvers. Mass.
Q16 thru 19	2N414	Raytheon Mfg. Co., Newton. Mass.
R1.4	RC07GF202J	MIL-R-11
R2.4.7.9.10.12.13. 15.16.19.21.23 24.25.27.28.30.31 35.36.37.39.40. 42.43.45.46.48.49.		
R11.14.17.18.20.26. 29.32.33.38.41.44. 47.50.52.54	RC07GF103J	MIL-R-11
R6.8	RC07GF302J	MIL-R-11
R3	RC07GF224J	MIL-R-11
R51	RC07GF104J	MIL-R-11
R48	30253042-20	MIL-R-11

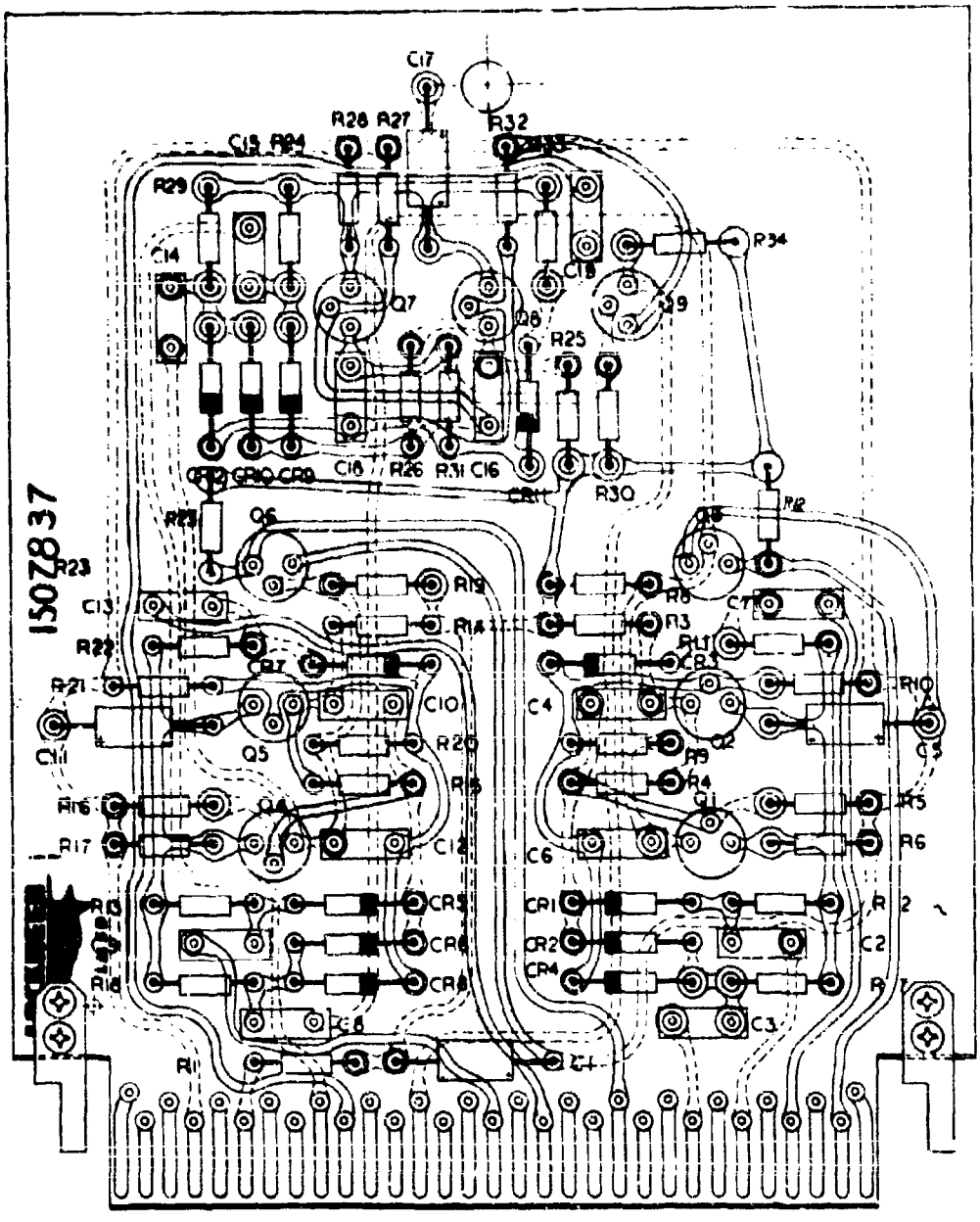

ONE-SHOT NO.1
BLOCKING OSCILLATOR NO.1
DUAL FOL
FLIP-FLOP
ONE-SHOT N
R41 28 ½W
C2 .1UF 35V ±20%
R3 50K
R6 470
C6 .01UF 100V
R18 3K
R9 1K
Q2 2N414
C7 .510
Q4 2N414
C1 200
C8 800 500V
R11 18K
C8 800
C9 800,600V
R1 8.2K
CR1 IN498
R7 47K
R14 4.7K
R15 82K
R21 360 ½W
R19 2.0K
C11 .01UF 35V ±10%
R10 100
CR6 IN498
Q6 2N438
Q7 2N438
C24 1UF
CR3 IN498
CR10 IN625
C14 .01UF 100V
R26 360
R27 4.7K
Q9 2N4
R28 5K
R2 10K
R8 3K
R13 750
C10 .01UF 100V
R16 3K
R5 10K
CR2 IN625
Q1 2N414
Q3 2N414
Q5 2N414
CR4 IN625
R20 10K
C13 470
C4 470
C5 470
R9 6.2
R17 6.2K
C12 470
R10 3K
R18 3K
R24 470
R29 3K
Q8 2N414
C15 600
C16 820
R23 82K
CR5 IN498
R25 4.7K
ULSE INPUT
NG PULSE INPUT

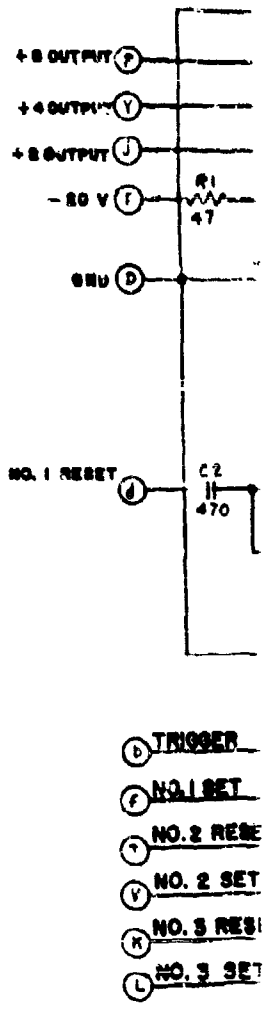
B



C

Fig. A-43 Sync Gate, G-A

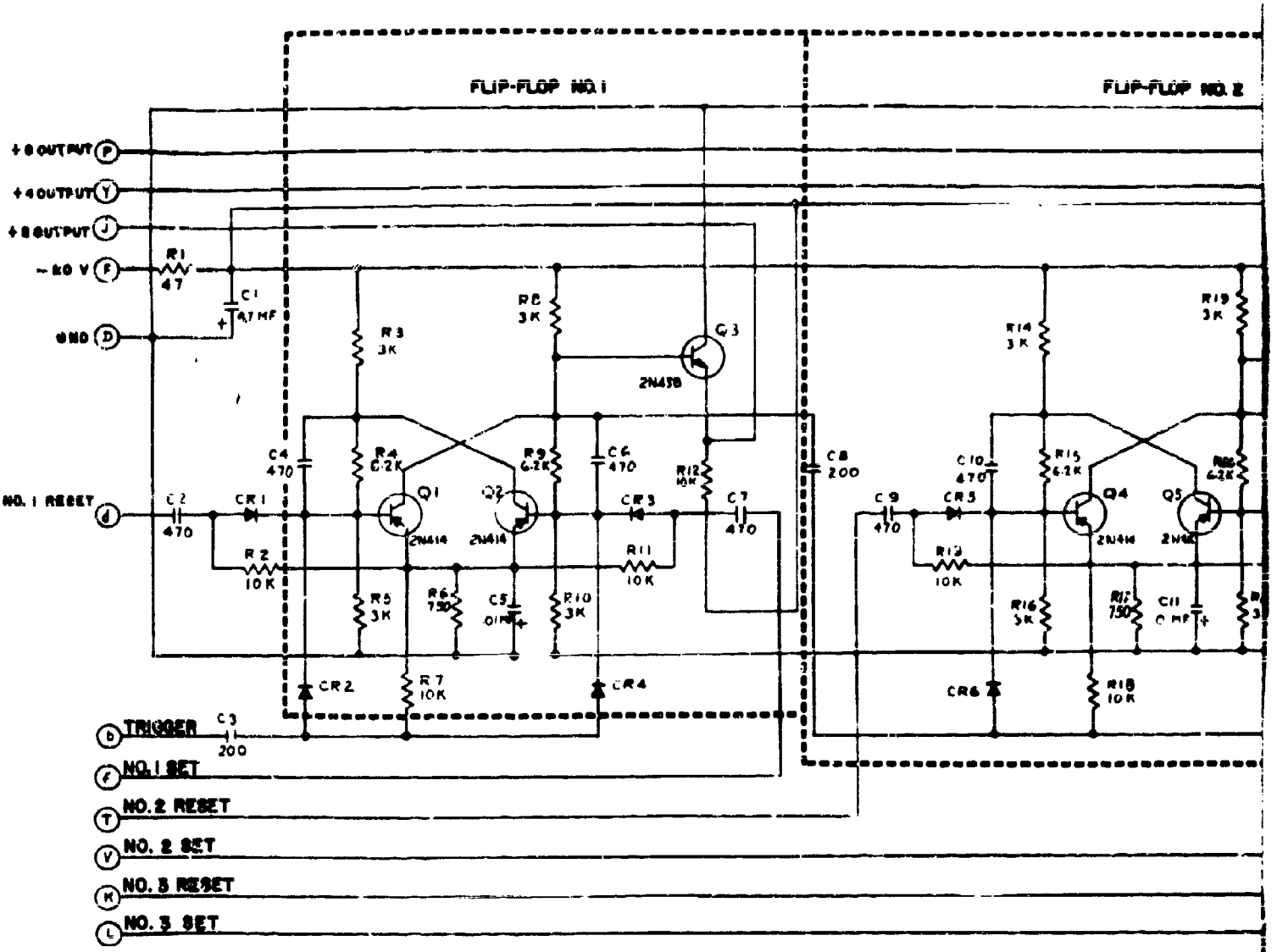




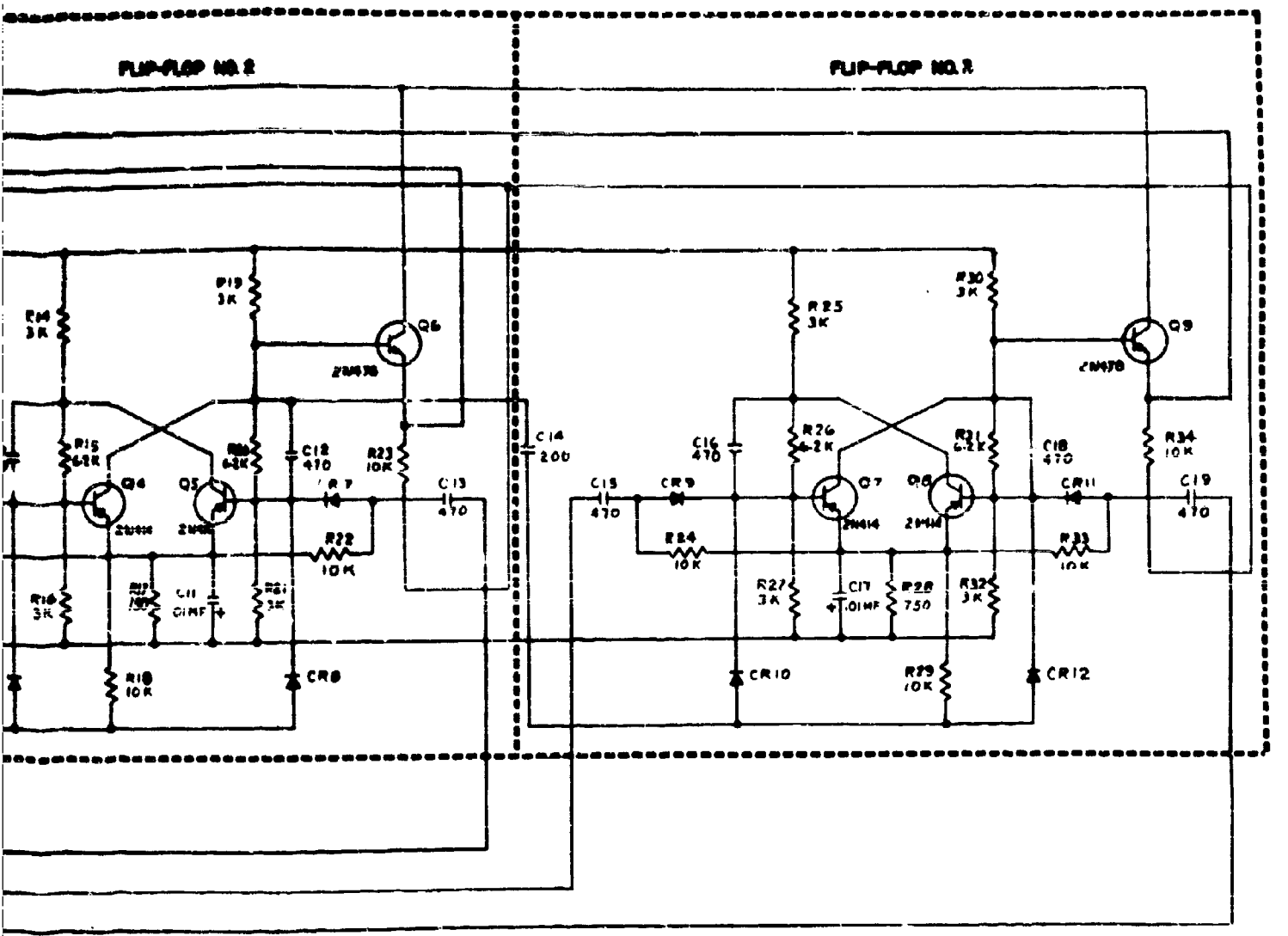
PARTS LIST

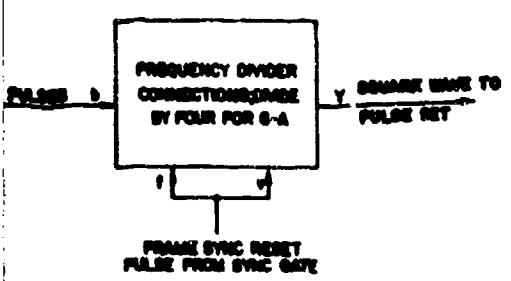
Reference Designation	Part No.	Vendor or Mil. Spec.
C1	150D475X9006A2	Sprague Electric Co., North Adams, Mass.
C2 3,4,6 7 9,10,12, 13		
15,16,18,19	DM15F471J	El Menco, Los Angeles, Calif.
C5,11,17	150D156X9006A2	Sprague Electric Co., North Adams, Mass.
C8,14	DM15F101J	El Menco, Los Angeles, Calif.
C20 thru 28	1N5818	Pacific Semiconductor, Culver City, Calif.
Q1 thru 9	2N414	Raytheon Mfg. Co., Newton, Mass.
R1	RC07GF470J	MIL-R-11
R2,7,11,13,15,18,22, 24,26 29,32,34,36	RC07GF102J	MIL-R-11
R3,5,9,10,14,16,19 21,25,27,30,33	RC07GF560J	MIL-R-11
R4,8,12,20,23,31	RC07GF182J	MIL-R-11
R6,17,28	RC07GF101J	MIL-R-11

A


FLIP-FLOP NO. 1
FLIP-FLOP NO. 2
+8 OUTPUT P
+4 OUTPUT Y
+2 OUTPUT J
-20 V F
GND D
NO. 1 RESET d
TRIGGER b
NO. 1 SET f
NO. 2 RESET T
NO. 2 SET V
NO. 3 RESET H
NO. 3 SET L
R1 47
C1 4.7 MF
R3 3K
R8 3K
Q3 2N438
C4 470
R4 6.2K
R9 6.2K
C6 470
R12 10K
C8 200
C2 470
CR1
Q1 2N414
Q2 2N414
CR3
C7 470
R2 10K
R11 10K
R5 3K
R6 750
C5 .01 MF
R10 3K
CR2
R7 10K
CR4
C3 200
R14 3K
R19 3K
C10 470
R15 6.2K
R20 6.2K
C9 470
CR5
Q4 2N414
Q5 2N414
R13 10K
R16 5K
R17 750
C11 .1 MF
CR6
R18 10K
DATA SYNC PULSES b
FREQUENCY DIVIDER CONNECTION; DIVIDE BY EIGHT FOR VIBRATION
P TRIGGER PULSE'S FOR SUBCOM PULSE SEQUENCER
d K T
FRAME SYNC RESET PULSE FROM SYNC GATE
DATA SYNC PULSES b
FREQUENCY DIVIDER CONNECTION; DIVIDE BY FOUR FOR S-A
f V
FRAME SYNC RESET PULSE FROM SYNC GATE

B



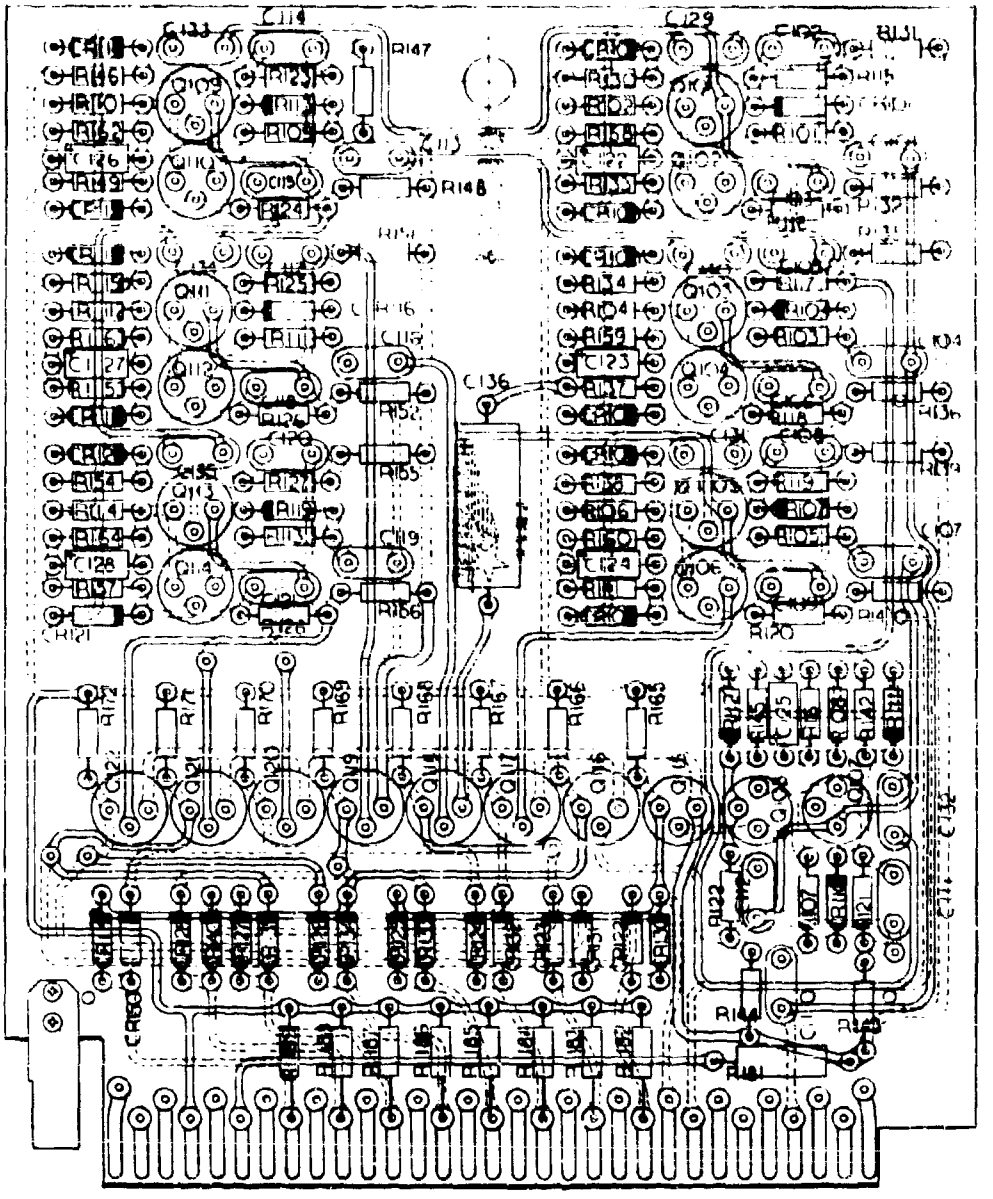


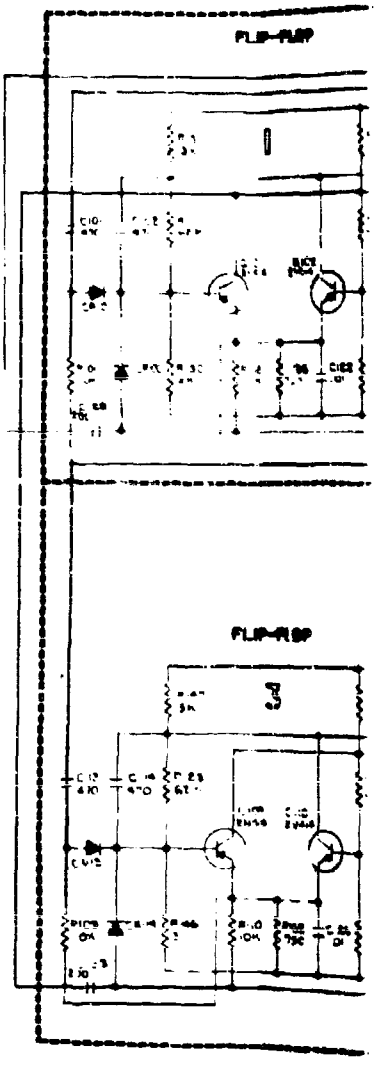
1. ALL RESISTANCE VALUES IN OHMS UX-10000±5% 1/4 WATT
2. ALL CAPACITANCE VALUES IN MICROMICROFARADS
3. ALL DIODES 1N625

NOTE: UNLESS OTHERWISE SPECIFIED

C

Fig. A-44 Frequency Divider, G-A

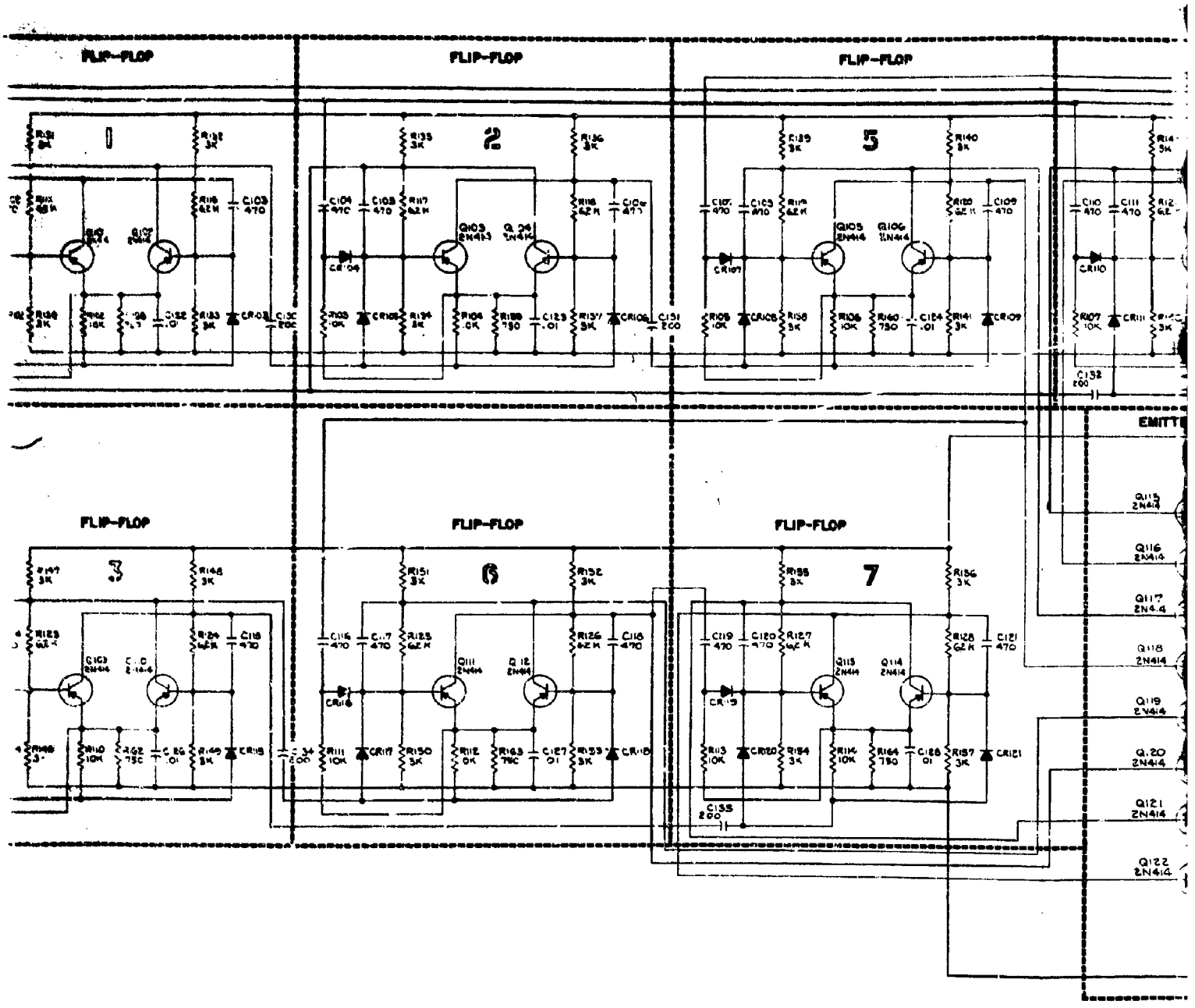




PARTS LIST

Reference Designation	Part No.	Vendor or Mfr. Name
C101 thru 151	[illegible]	[illegible]
C102 thru 154	[illegible]	[illegible]
C103 thru 155	[illegible]	[illegible]
C105	[illegible]	[illegible]
CR101 thru 105, 108, 109	[illegible]	[illegible]
Q101 thru 103	[illegible]	[illegible]
R101 thru 134, 165 thru 170	[illegible]	[illegible]
R115 thru 150	[illegible]	[illegible]
R150 thru 157	[illegible]	[illegible]
R158 thru 164	[illegible]	[illegible]
R161	[illegible]	[illegible]
R168 thru 169	[illegible]	[illegible]

A


FLIP-FLOP
FLIP-FLOP
FLIP-FLOP
FLIP-FLOP
FLIP-FLOP
FLIP-FLOP
EMITT

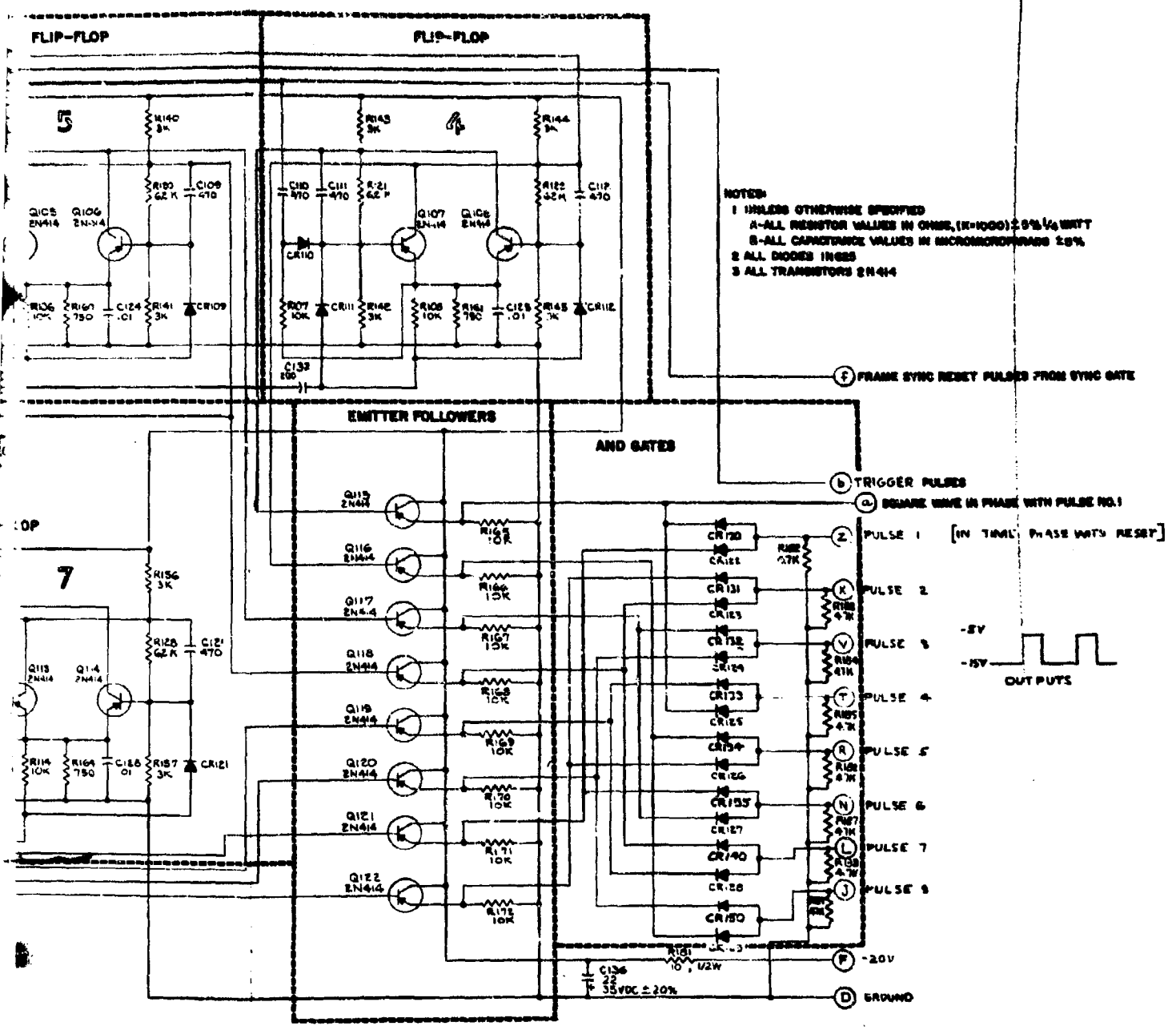
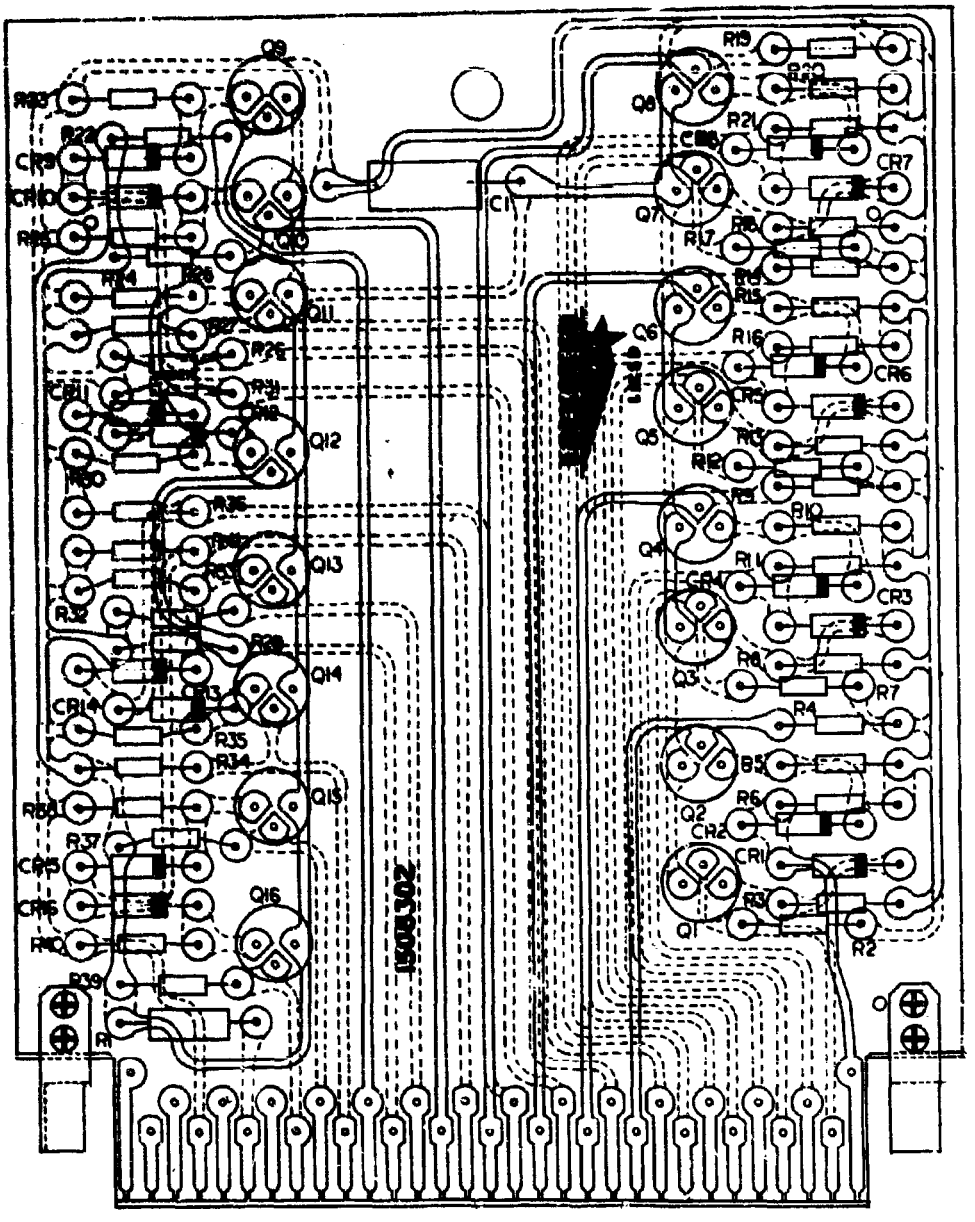
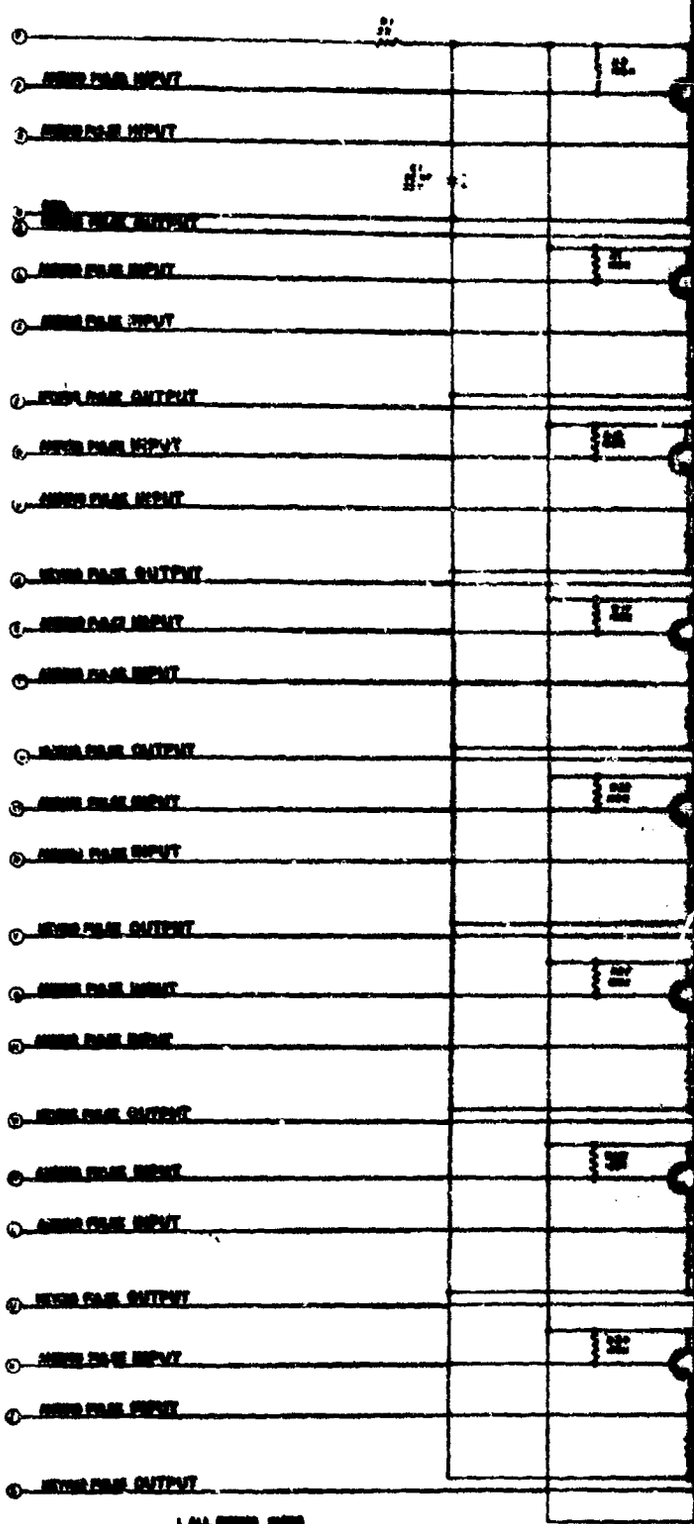


Fig. A-45 Eight-Channel Pulse Sequencer, G-A

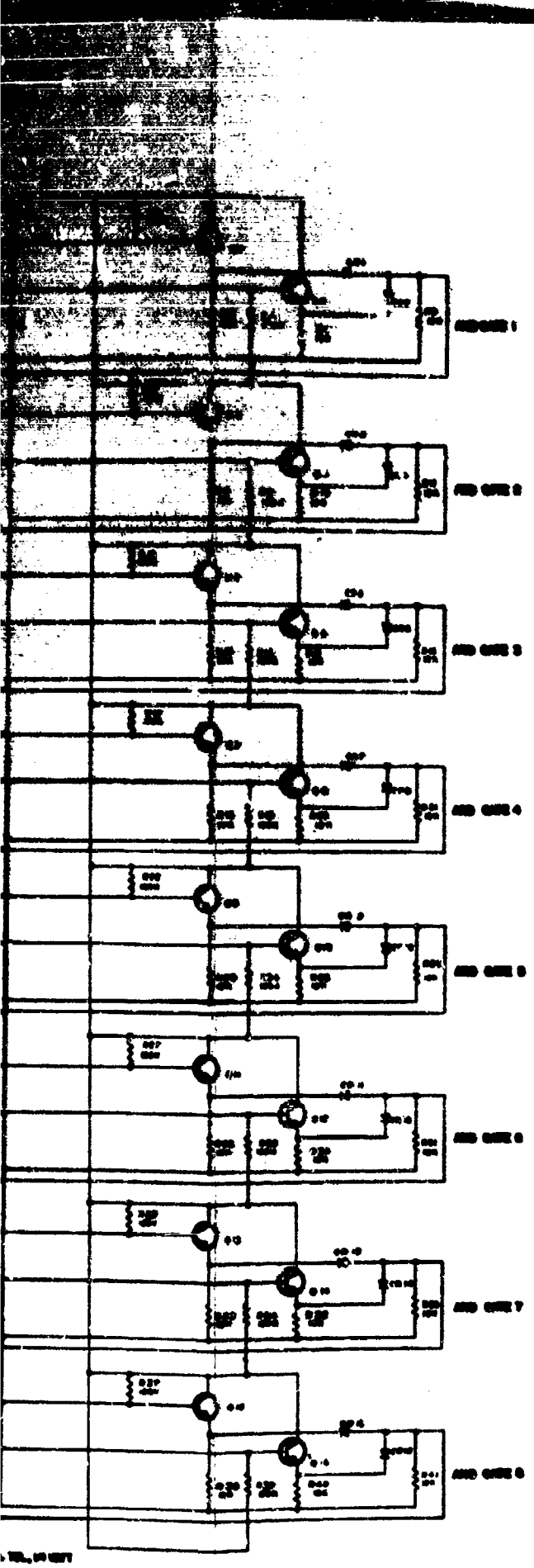


PARTS LIST

Reference Designation	Part No.	Vendor or Mil. Spec.
C1	1N3032,1N3032R1	Sprague Electric Co., North Adams, Mass.
CR1 thru 10	1N485	Pacific Semiconductor, Culver City, Calif.
Q1 thru 10	2N414	Raytheon Co., Needham Hts., Mass.
R1 R3, 4, 7, 9, 12, 14, 17, 19, 22, 24, 27, 30, 33, 36, 39 R2, 5, 6, 8, 10, 11, 13, 15, 16, 18, 20, 21, 23, 25, 26, 28, 29, 31, 32, 34, 35, 37, 38, 40, 41	RC07GF104J RC07GF102J	MIL-R-11 MIL-R-11

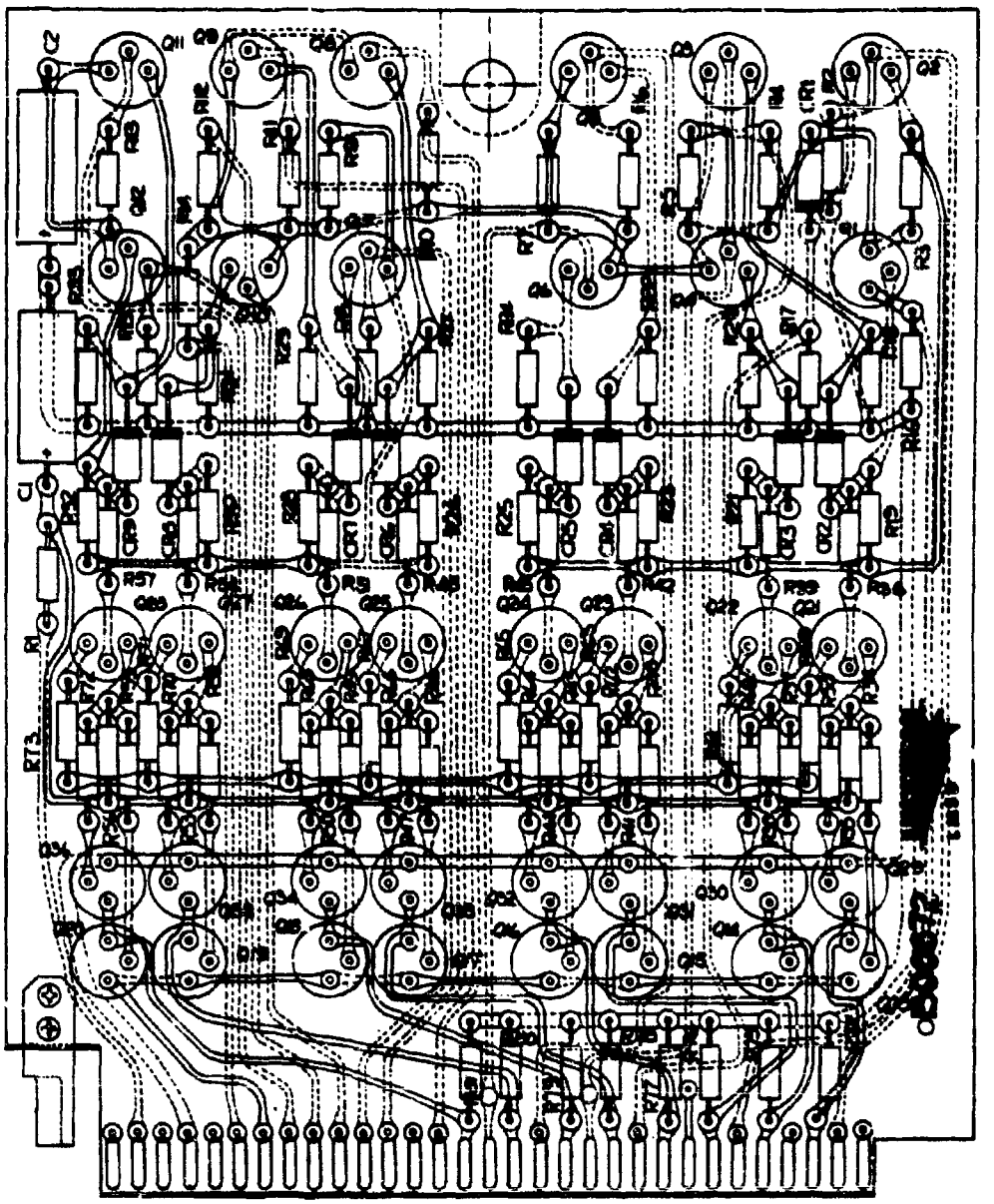


B



C

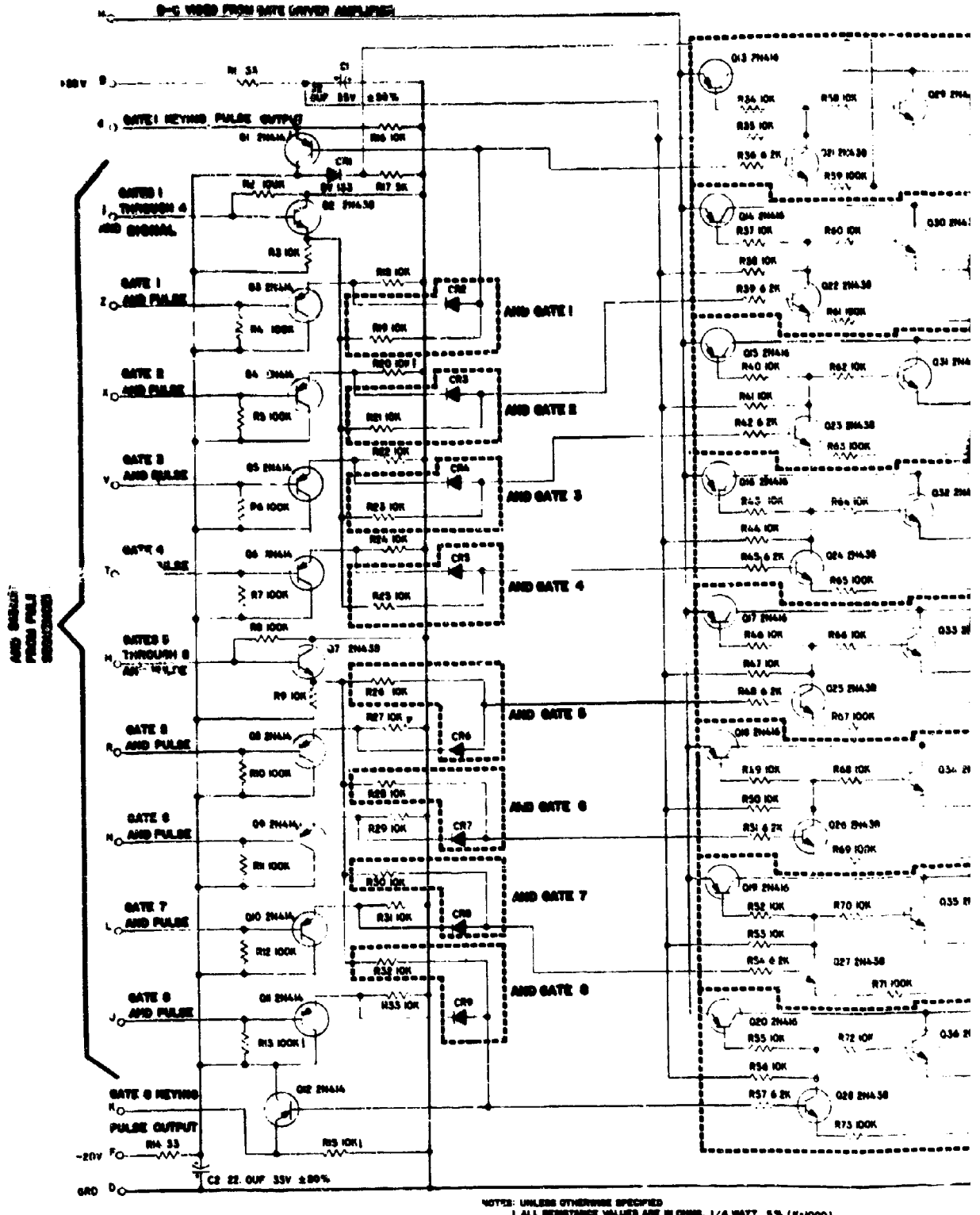
Fig. A-46 Matrix



PARTS LIST

Reference Designation	Part No.	Vendor or MIL Desc.
C1, 2	1N6B6B3Z*0.1MB1	Sprague Electric Co., North Adams, Mass.
CR1	1N746	Transitron, Wakefield, Mass.
CR2 thru 9	1N625	Fairchild Semiconductor, Culver City, Calif.
Q1, 3 thru 6, 8 thru 12	2N414	Raytheon, Newton, Mass.
Q2, 7, 31 thru 38	2N430	CBS-Hytron, Danvers, Mass.
Q13 thru 30	2N410	Raytheon, Newton, Mass.
R1, 14	RC07GF680J	MIL-R-11
R2, 4, 5, 6 thru 9, 10 thru 13	RC07GF104J	MIL-R-11
R3, 9, 11, 16, 18 thru 23, 27, 32, 35, 41, 45, 46, 47, 48, 52, 53, 54, 58, 59, 60, 63, 64, 65, 66, 70, 72, 74 thru 81	RC07GF106J	MIL-R-11
R17	RC07GF680J	MIL-R-11
R24, 25, 43, 44, 49, 51, 55, 57	RC07GF105J	MIL-R-11
R26, 31, 33, 34, 37, 39 71, 73	RC07GF104J	MIL-R-11

A


AND GATE 1
AND GATE 2
AND GATE 3
AND GATE 4
AND GATE 5
AND GATE 6
AND GATE 7
AND GATE 8
GATE 8 KEYING PULSE OUTPUT
GND
-20V
+18V

B

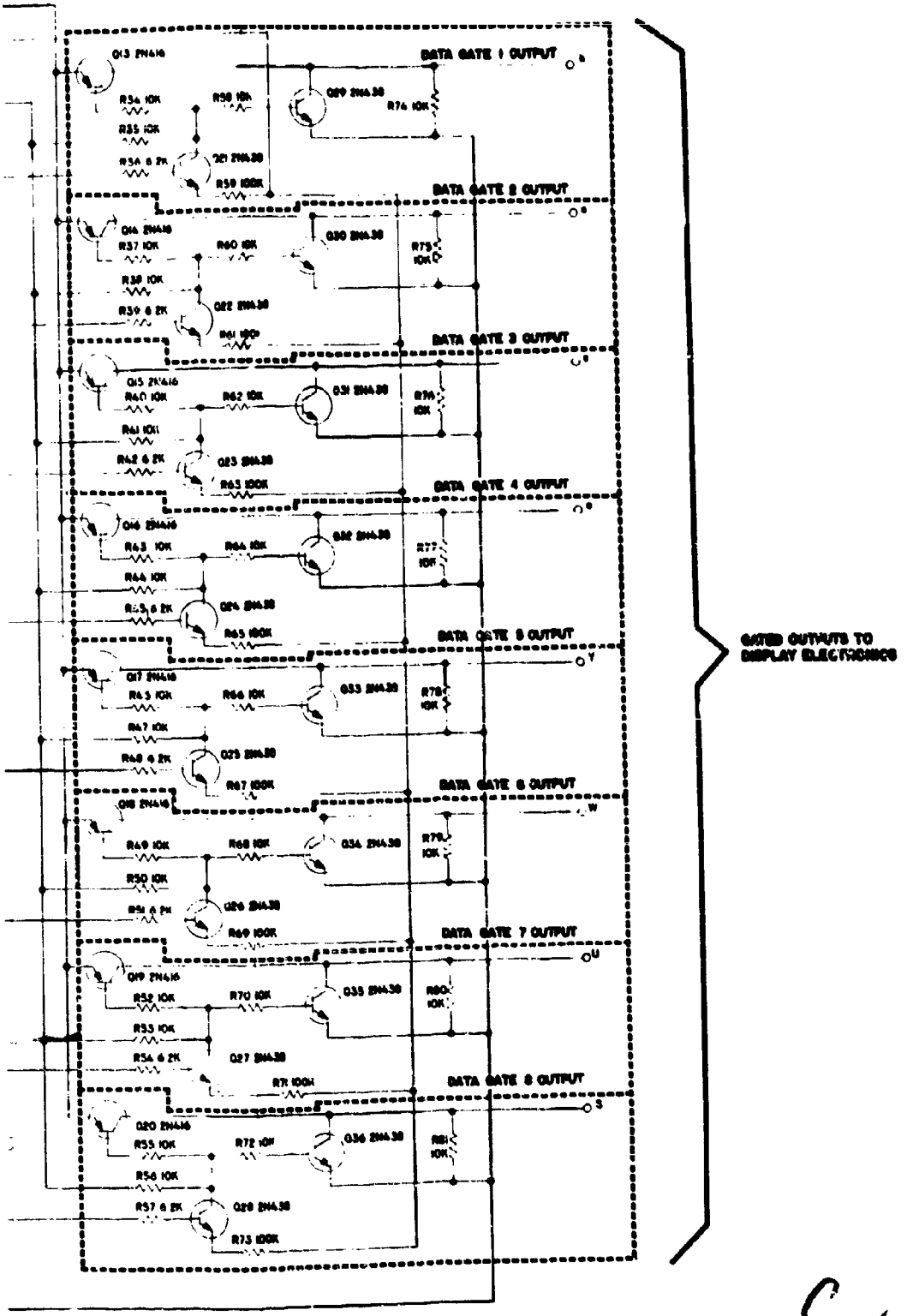
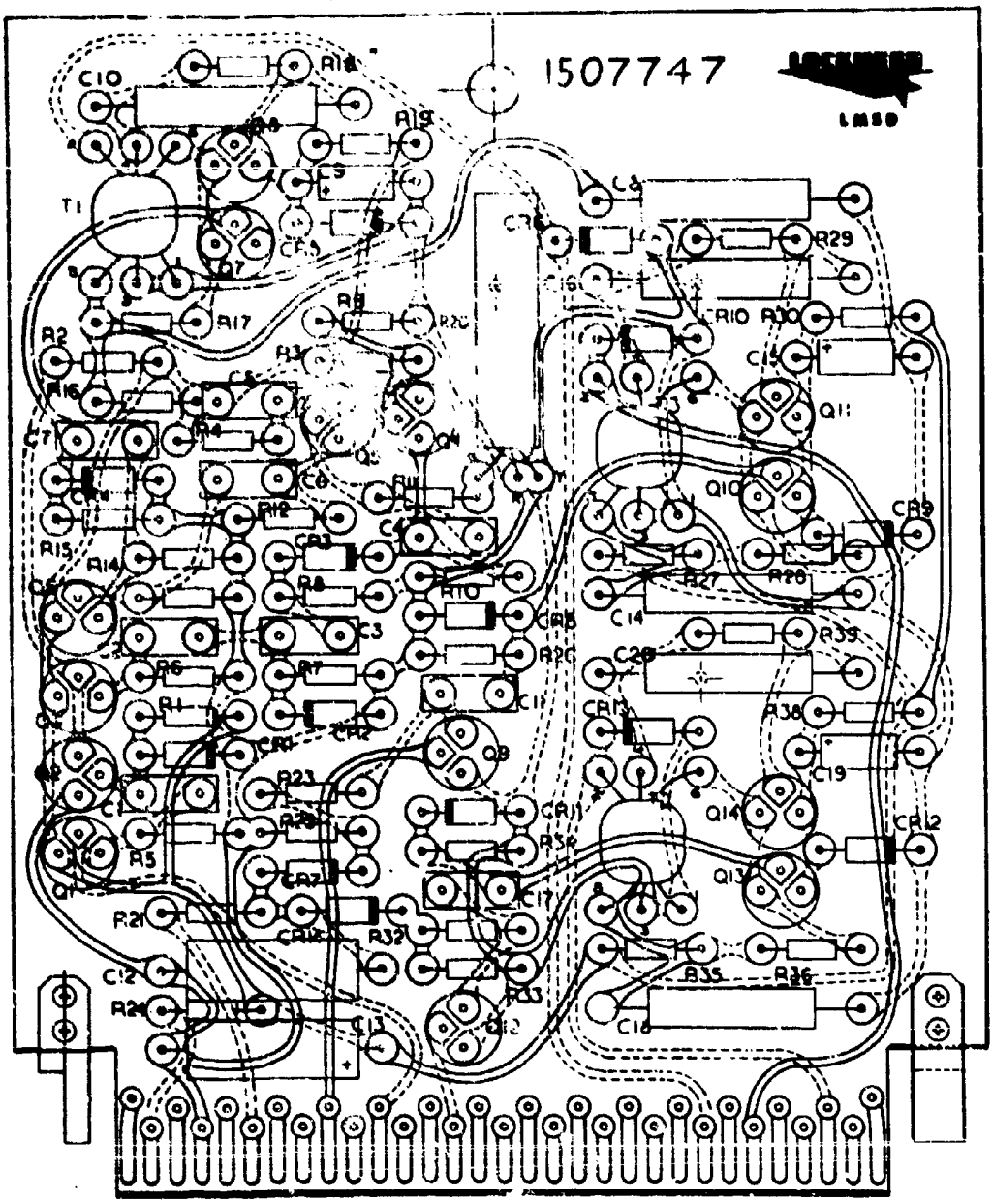


Fig. A-47 Data Gates, G-A



CLOCK SQUARE WAVE FROM DATA SYNC SEPARATOR

M

GRD

F+20

B+20

INPUT FROM 4:1 FREQUENCY DIVIDER

K

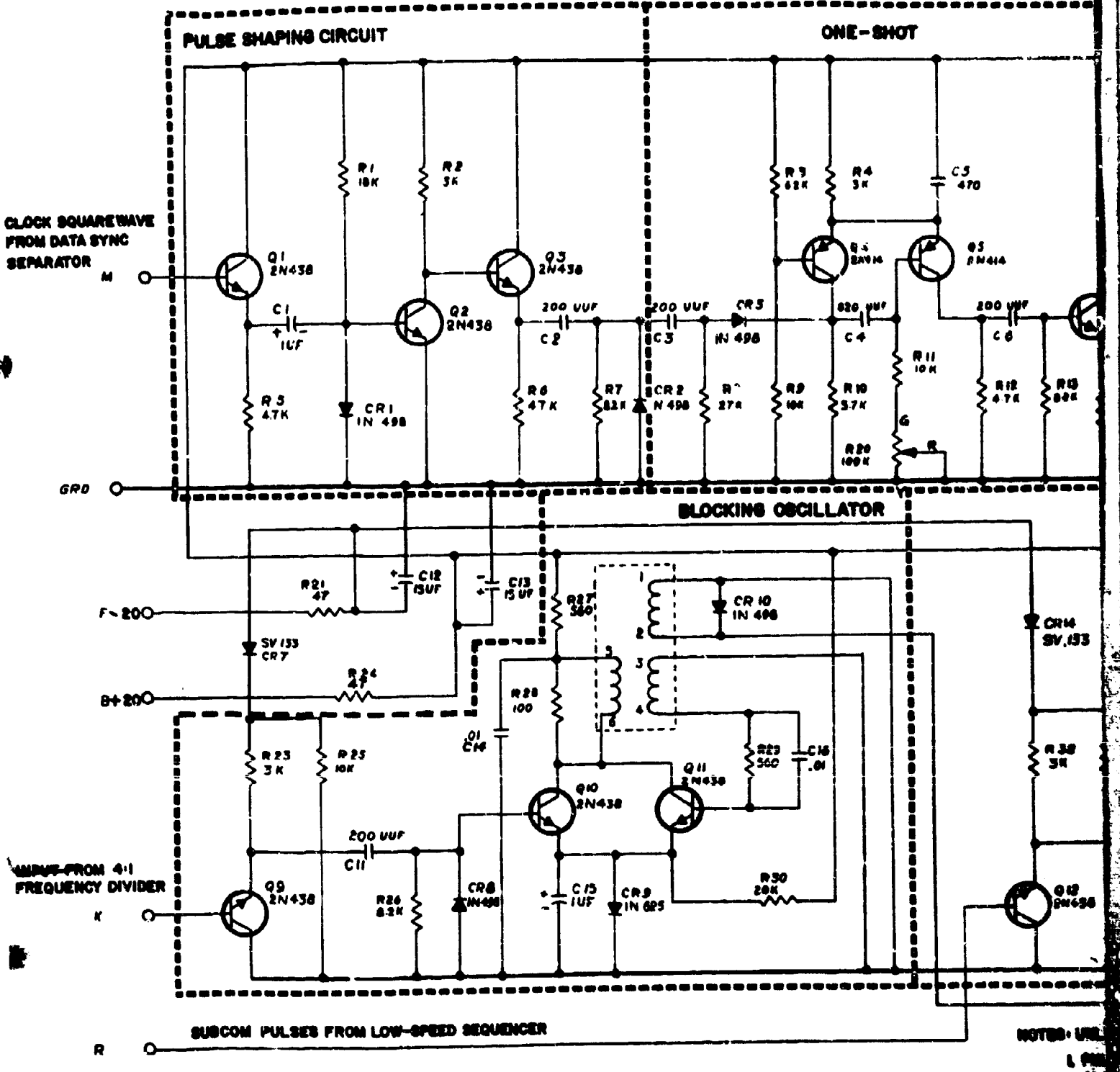
SUBCO

R

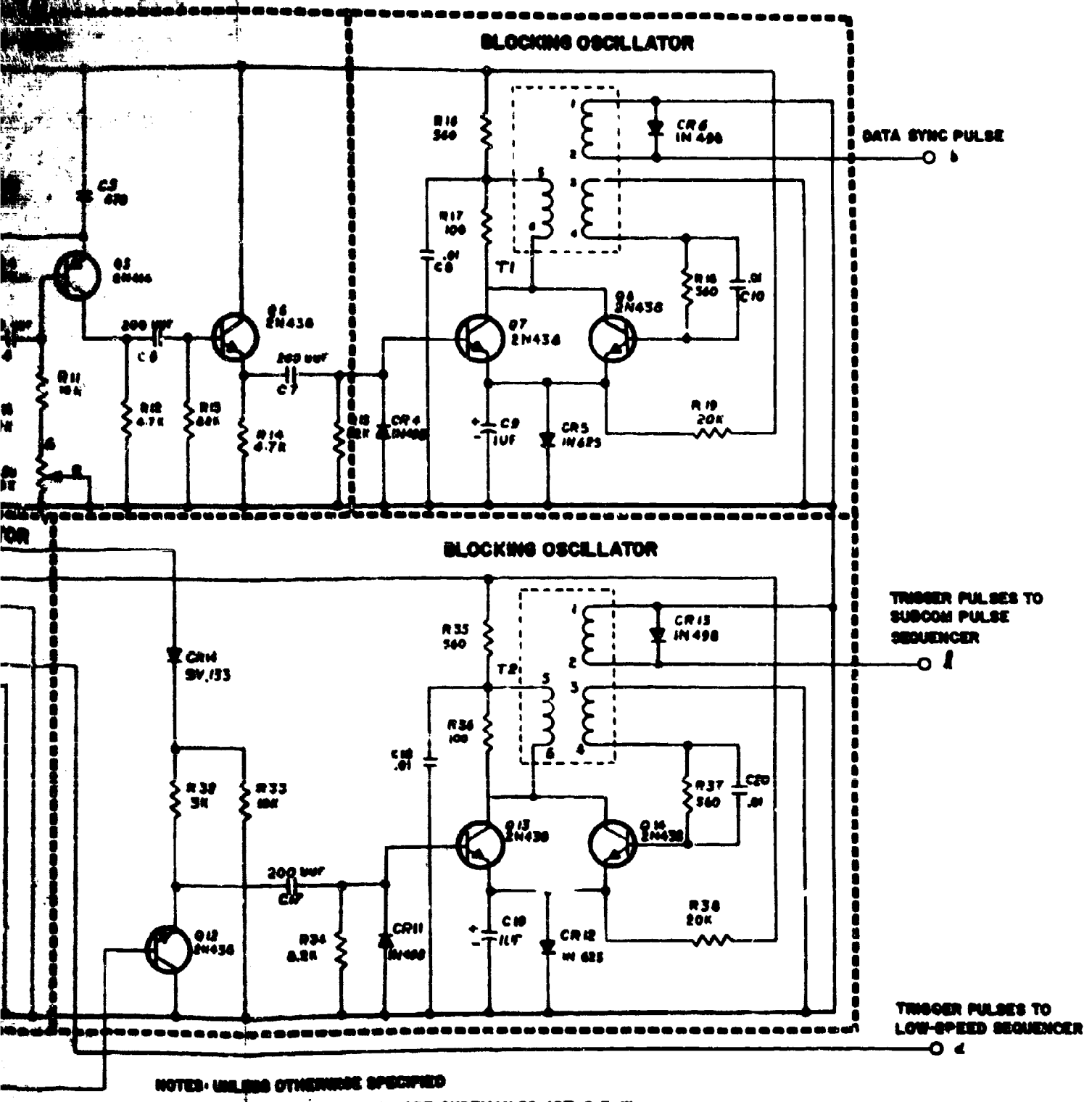
PARTS LIST

Reference Designation	Part No.	Vendor or Mfg. Desn.
C1, 4, 10, 19	1500[illegible]A1	Sprague Electric Co., North Adams, Mass.
C2, 3, 6, 7, 11, 17	[illegible]	[illegible]
C8, 16, 18, 20, 21	[illegible]	[illegible]
C9	[illegible]	Sprague Electric Co., North Adams, Mass.
C12, 13	[illegible]	Sprague Electric Co., North Adams, Mass.
CR1 thru 6, 8, 9 thru 12	1N[illegible]	Corp., Calif.
CR7	[illegible]	Transitron, Wakefield, Mass.
CR8, 9, 13 thru 14	[illegible]	Corp., Calif.
	[illegible]	Raytheon, Newton, Mass.
	[illegible]	MIL-S-11
R1, 4, 22, 23	[illegible]	MIL-S-11
R2, 3, 12, 14	[illegible]	MIL-S-11
R5, 11, 13, 28, 34	[illegible]	MIL-S-11
R6, 11, 25, 33	[illegible]	MIL-S-11
R7	[illegible]	MIL-S-11
R8, 10, 27, 29, 36, 37	[illegible]	MIL-S-11
R17, 38, 39	[illegible]	MIL-S-11
R18, 35, 36	[illegible]	MIL-S-11
R26	150-15-100000	Electro, Riverside, Calif.
R31, 34	[illegible]	MIL-S-11
T1, 2, 3	107 C & P-111	Corporation, Santa Monica, Calif.

A


PULSE SHAPING CIRCUIT
ONE-SHOT
BLOCKING OSCILLATOR
CLOCK SQUAREWAVE FROM DATA SYNC SEPARATOR
M
GRD
F~20
B+20
K
R
SUBCOM PULSES FROM LOW-SPEED SEQUENCER
INPUT FROM 4:1 FREQUENCY DIVIDER
Q1 2N438
Q2 2N438
Q3 2N438
Q9 2N438
Q10 2N438
Q11 2N438
R1 18K
R2 5K
R3 62K
R4 5K
C5 470
C1 1UF
200 UUF C2
200 UUF C3
CR3 IN 498
820 UUF C4
200 UUF C6
R5 4.7K
CR1 IN 498
R6 47K
R7 82K
CR2 IN 498
R8 27K
R9 10K
R10 5.7K
R11 10K
R12 4.7K
R13 82K
R20 100K
R21 47
C12 15UF
C13 15 UF
R27 360
CR10 IN 498
CR14 SV133
SV133 CR7
R24 47
R28 100
.01 C14
R23 3K
R25 10K
R29 560
C16 .01
R38 3K
200 UUF C11
R26 8.2K
CR8 IN498
C15 1UF
CR9 IN 625
R30 20K
CR12 SV133
NOTES: UNL
1. PIN
2. ALL
3. ALL

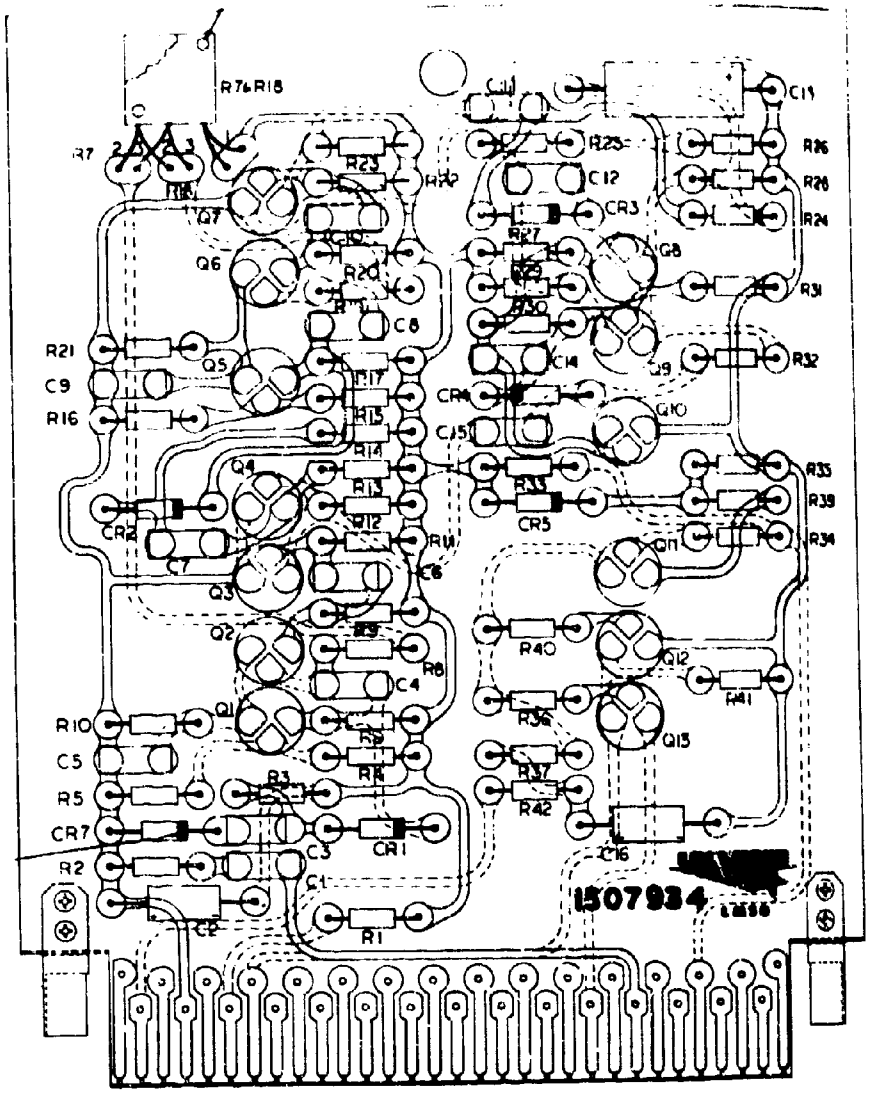
B



NOTES: UNLESS OTHERWISE SPECIFIED

1. PULSE TRANSFORMERS ARE SUDEMAN CO. NST. 0-5-III
2. ALL CAPACITANCE VALUES IN MICROFARADS
3. ALL RESISTANCE VALUES IN OHMS (K=1000) ± 5% TOLERANCE, 1/4 WATT

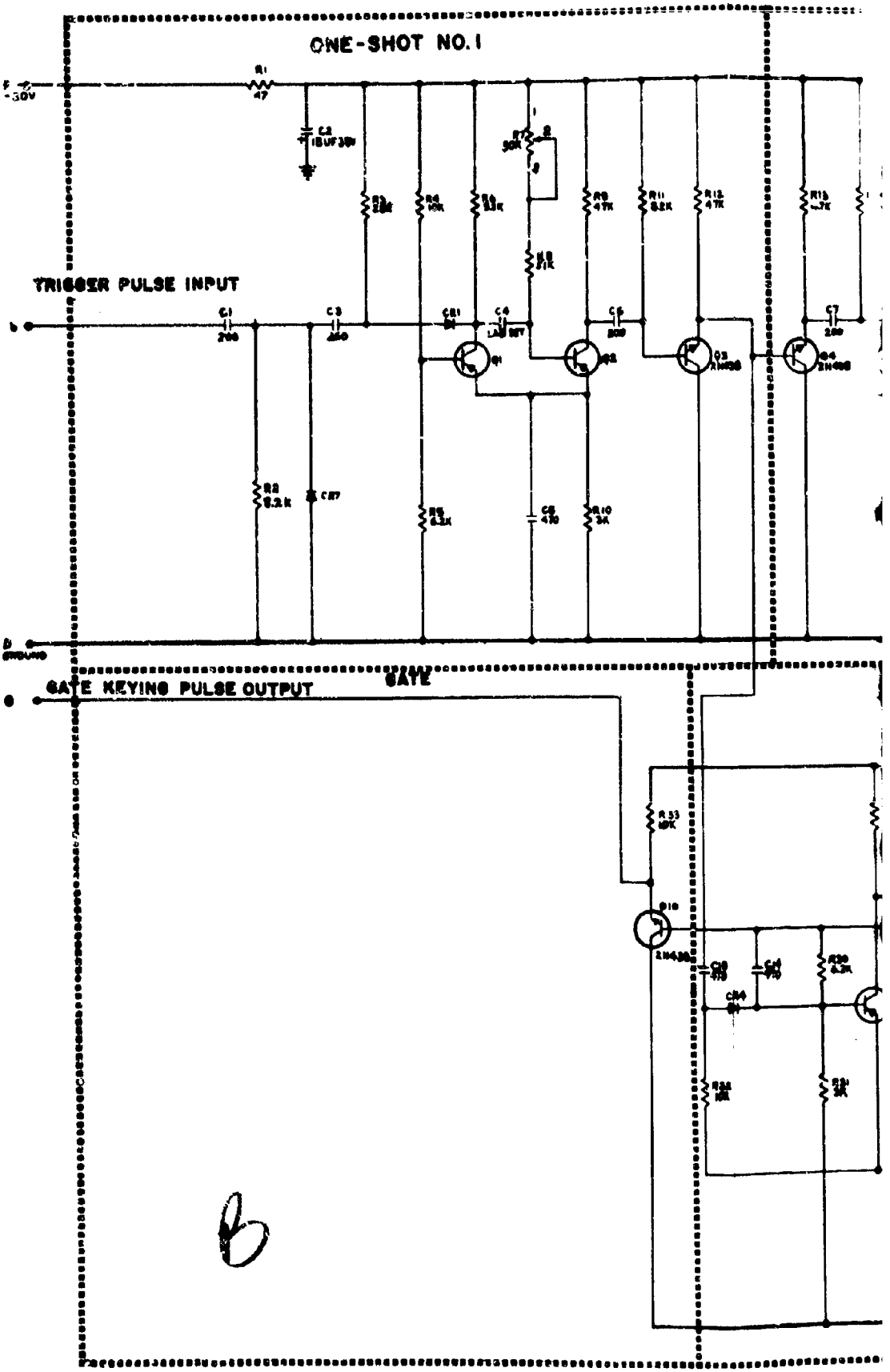
Fig. A-48 Pulse Set



PARTS LIST

Reference Designation	Part No.	Vendor or MIL Spec.
C1, 3, 6, 7, 10	DM15F201J	El Menco, Los Angeles, Calif.
C2	150D156X9035R1	Sprague Electric Co., North Adams, Mass.
C4, 8	DM15 (Lab Sup)	El Menco, Los Angeles, Calif.
C5, 9, 11, 12, 14, 15	DM15F471J	El Menco, Los Angeles, Calif.
C13	150D106X9035A2	Sprague Electric Co., North Adams, Mass.
C16	150D476X9035R1	Sprague Electric Co., North Adams, Mass.
CR1 thru 4, 7	1N498	CBS-Hytron, Danvers, Mass.
CR5	SV133	Transitron, Wakefield, Mass.
Q1, 2, 5, 6, 8, 9, 12	2N414	Raytheon, Newton, Mass.
Q3, 4, 7, 10, 11	2N438	CBS-Hytron, Danvers, Mass.
Q13	2N416	Raytheon, Newton, Mass.
R1	RC07GF470J	MIL-R-11
R2, 11, 22	RC07GF822J	MIL-R-11
R3, 14	RC07GF273J	MIL-R-11
R4, 15, 24, 32, 33, 35, 37, 40, 41	RC07GF103J	MIL-R-11
R5, 16, 25, 30, 34, 36	RC07GF682J	MIL-R-11
R6, 17	RC07GF512J	MIL-R-11
R7, 18	316-64-68K	Daystrom-Pacific, Santa Monica, Calif.
R8, 19	RC07GF513J	MIL-R-11
R9, 12, 13, 20, 23	RC07GF472J	MIL-R-11
R10, 21, 26, 27, 29, 31	RC07GF302J	MIL-R-11
R28	RC07GF751J	MIL-R-11
R39, 42	RC07GF101J	MIL-R-11

A


ONE-SHOT NO. 1
TRIGGER PULSE INPUT
GATE KEYING PULSE OUTPUT
GATE

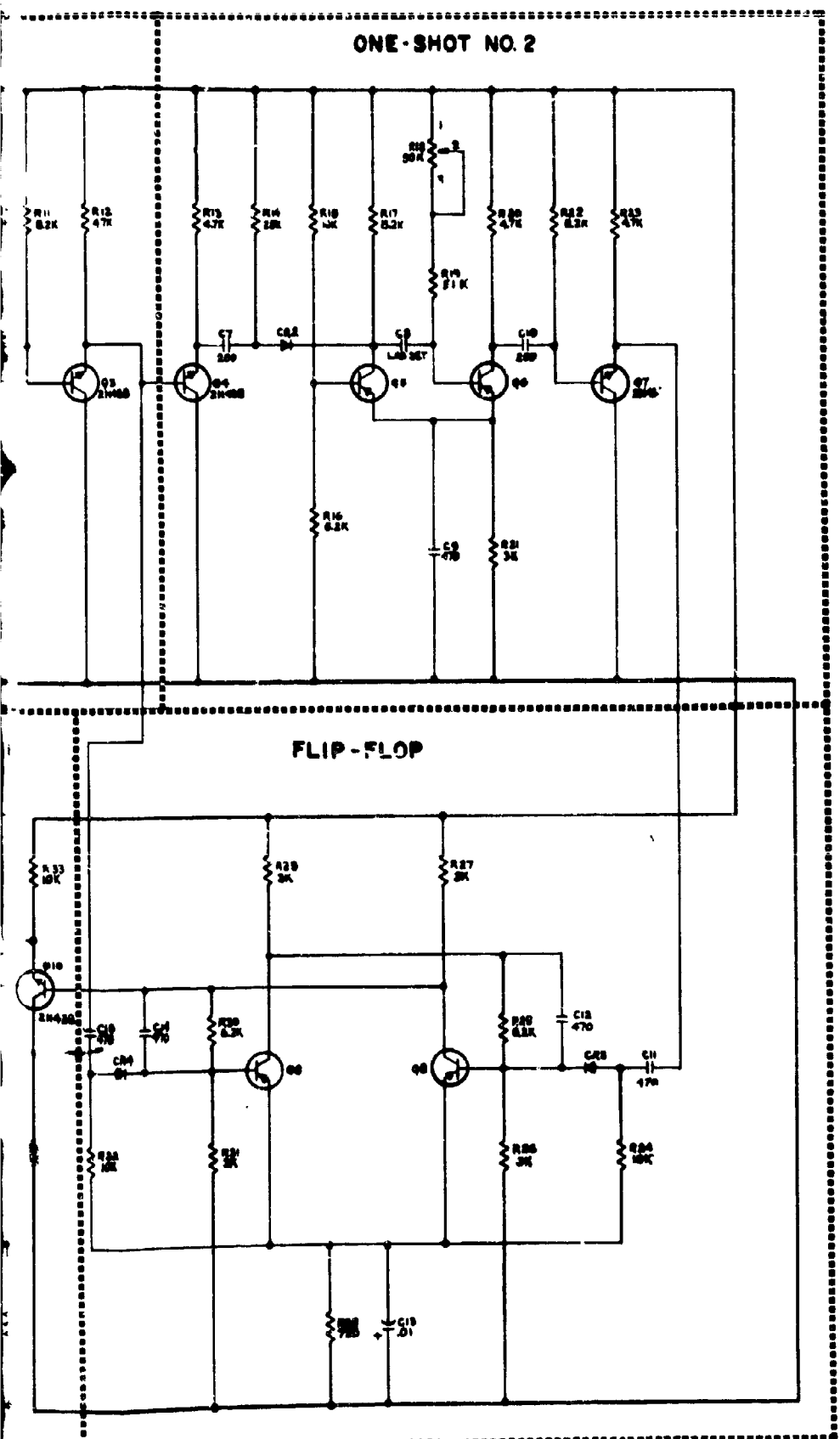
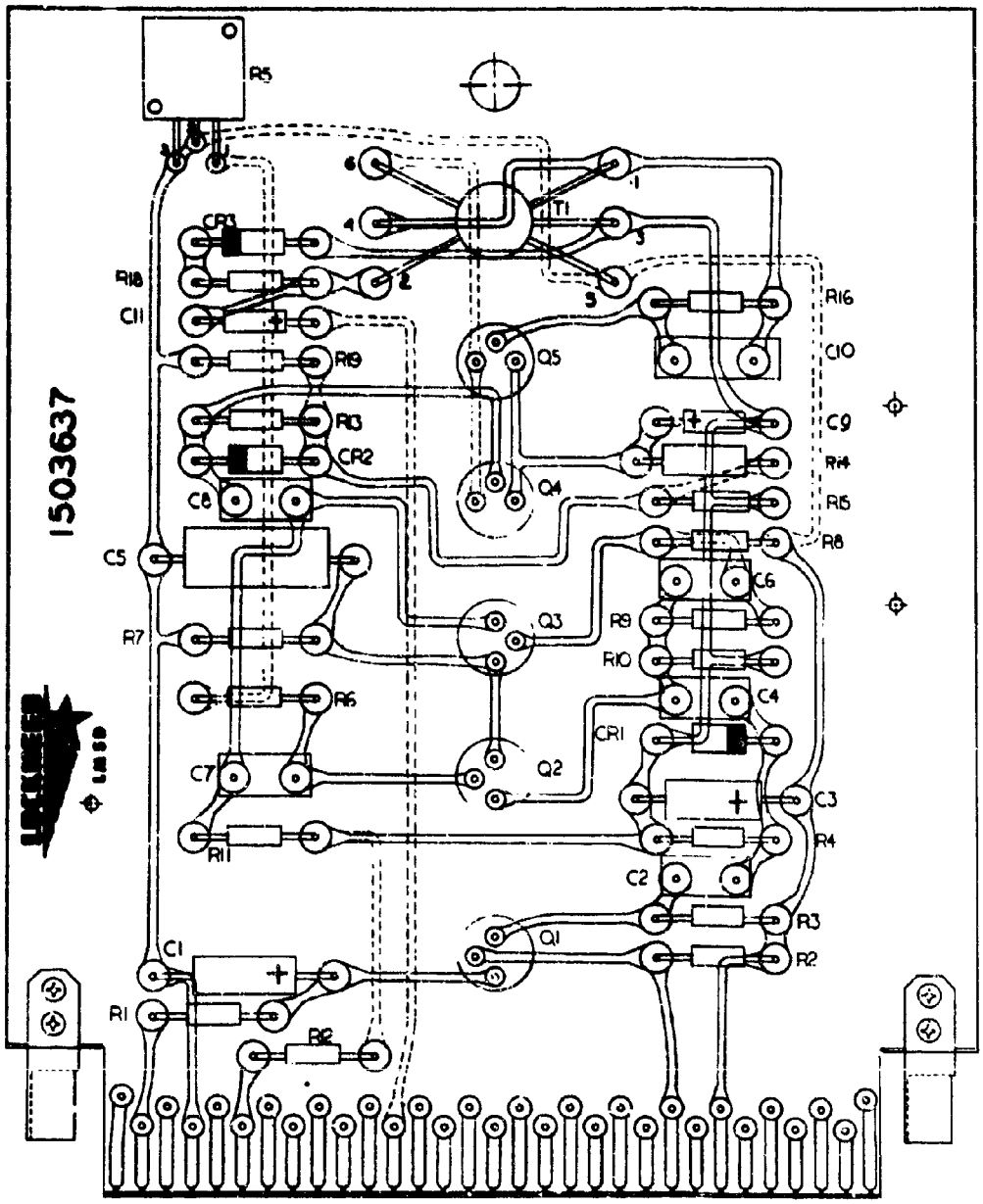


Fig. A-49 Duty Cycle II



B
+2CV

CLOCK PULS
DATA SYNC
A
INPUT

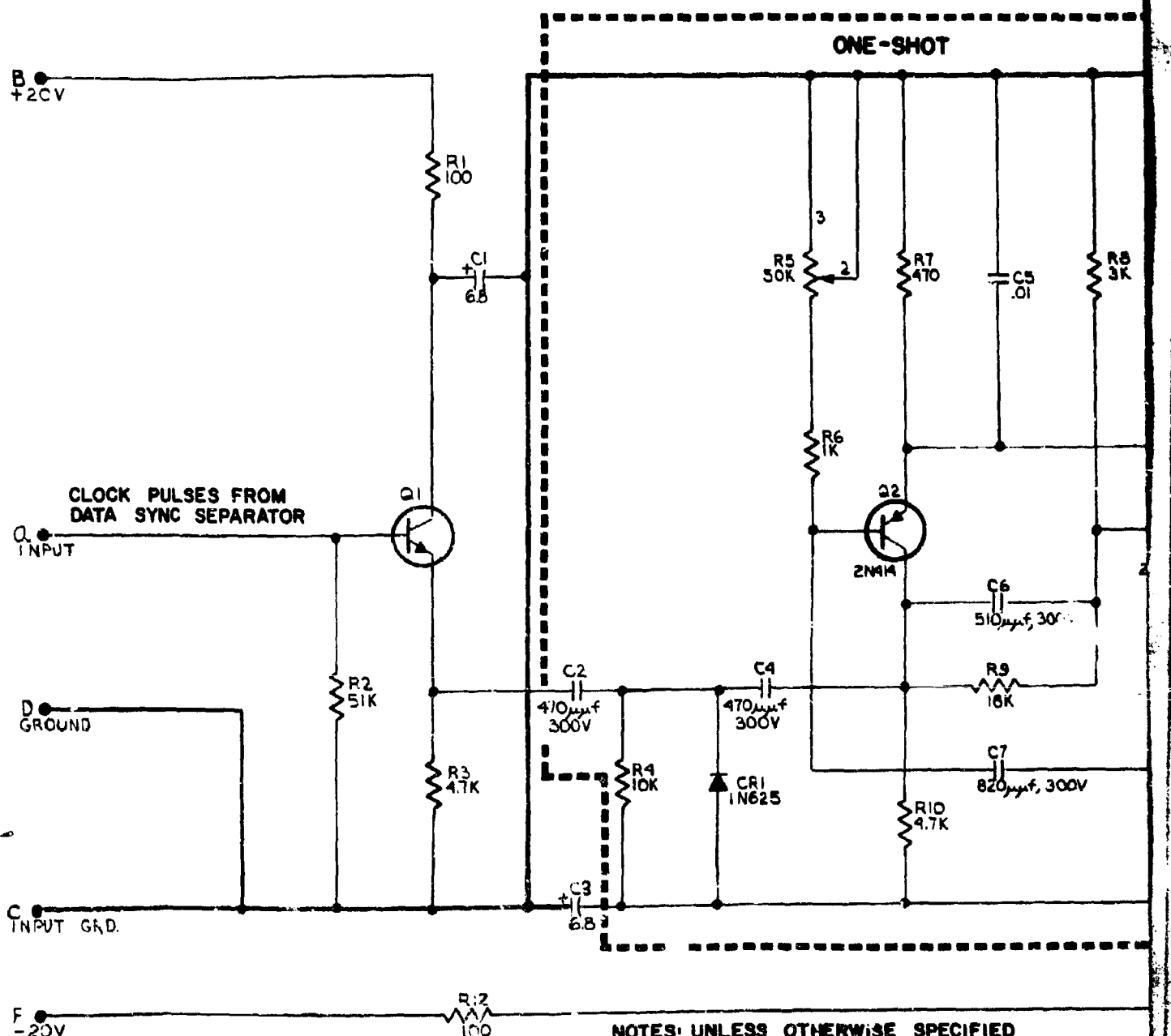
D
GROUND

C
INPUT GRD.

F
-20V

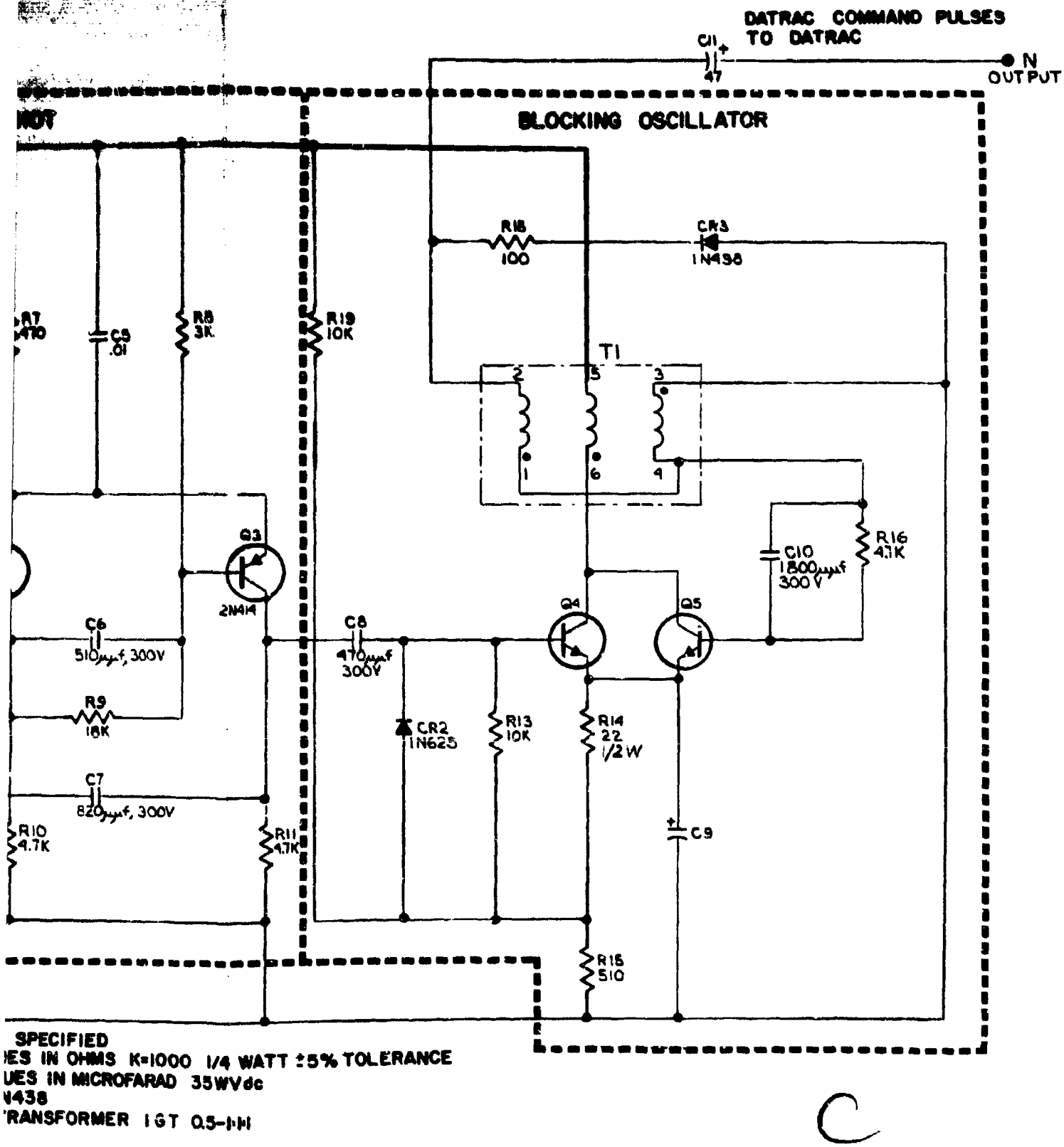
PARTS LIST

Reference Designation	Part No.	Vendor or Mfr. Spec.
C1	196D686X9063AB1	Sprague Electric Co., North Adams, Mass.
C2, 4, 6	DM-15F471-J	El Menco, Los Angeles, Calif.
C3	CPC06A1KE106K	MIL-C-6053B, MIL-C-6053/17
C5	DM15-F-121-J	El Menco, Los Angeles, Calif.
C7	DM15-F-681J	El Menco, Los Angeles, Calif.
C8	196D104X9063AA1	Sprague Electric Co., North Adams, Mass.
C10	DM19-F153J	El Menco, Los Angeles, Calif.
C11	196D474X9063AA1	Sprague Elec. Co., N. Adams, Mass.
CR1, 2	1N628	Pacific Semiconductor, Culver City, Calif.
CR3	1N498	CBS-Hytron, Danvers, Mass.
Q1, 4, 5	2N438	CBS-Hytron, Danvers, Mass.
Q2, 3	2N416	Raytheon, Newton, Mass.
R1, 12, 16	RC07GF101J	MIL-R-11
R2	RC07GF512J	MIL-R-11
R3, 10, 11	RC07GF472J	MIL-R-11
R4, 13, 19	RC07GF103J	MIL-R-11
R5	315-04-69K	Daystrom-Pacific, Santa Monica, Calif.
R6	RC07GF106J	MIL-R-11
R7	RC07GF471J	MIL-R-11
R8	RC07GF562J	MIL-R-11
R9	RC07GF183J	MIL-R-11
R14	RC07GF220J	MIL-R-11
R15	RC07GF511J	MIL-R-11
R16	RC07GF751J	MIL-R-11
T1	1GT.88 1:1:1	Gudeman, Santa Monica, Calif.



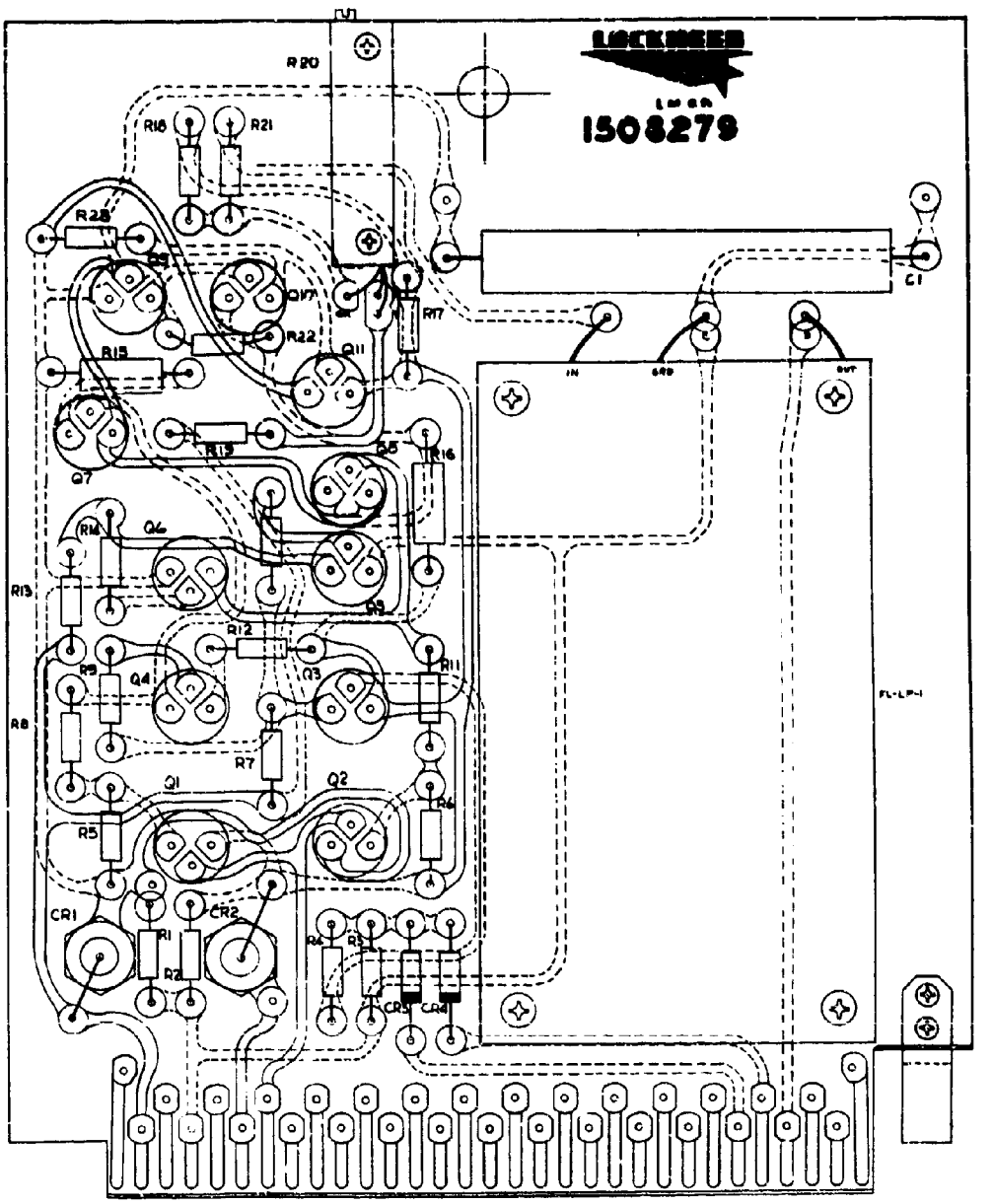
NOTES: UNLESS OTHERWISE SPECIFIED
1-ALL RESISTANCE VALUES IN OHMS K=1000 1/4
2-ALL CAPACITANCE VALUES IN MICROFARAD 35V
3-ALL TRANSISTORS 2N438
4-TI GUDEMAN PULSE TRANSFORMER 1GT 0.5-

B



C

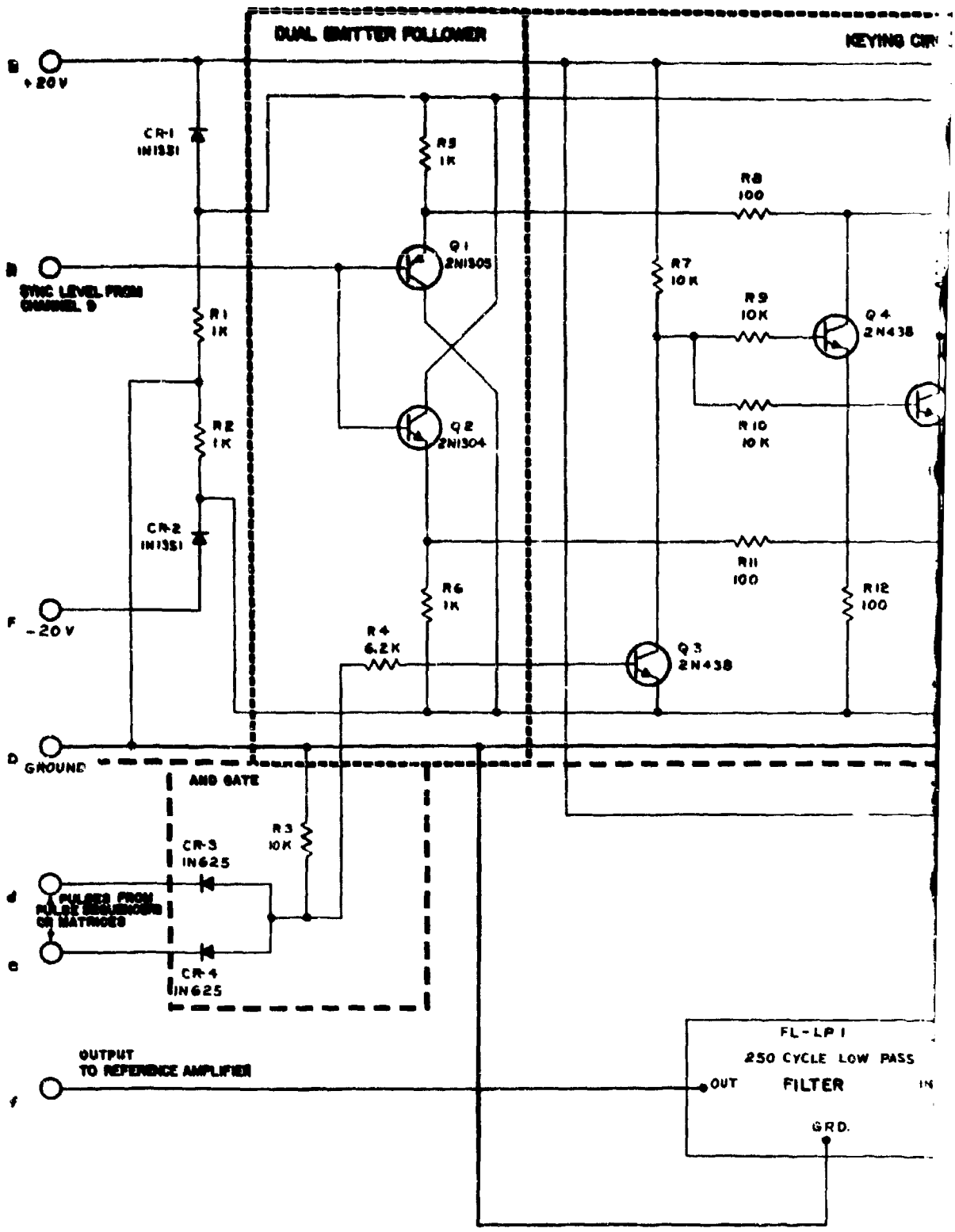
Fig. A-50 Data Sync Delay Record, G-A



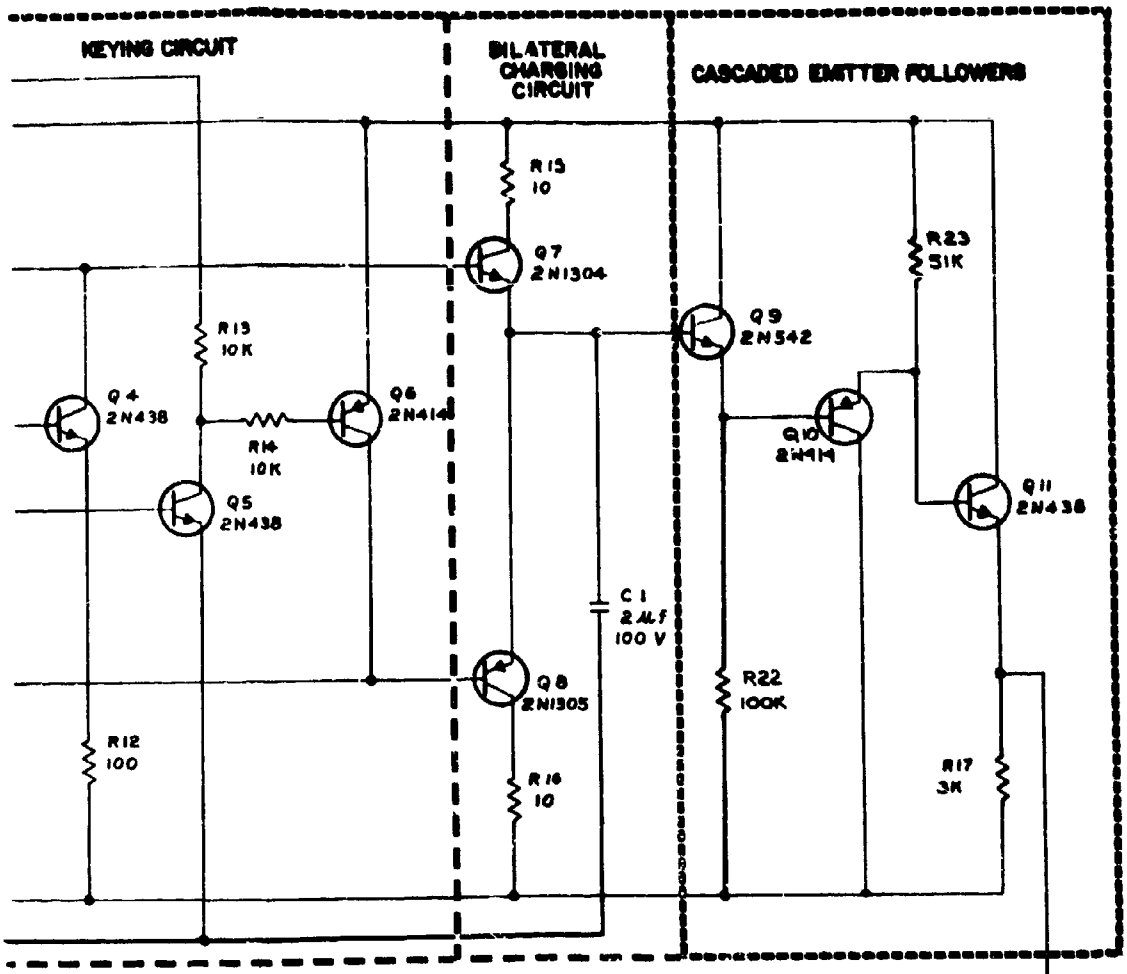
PARTS LIST

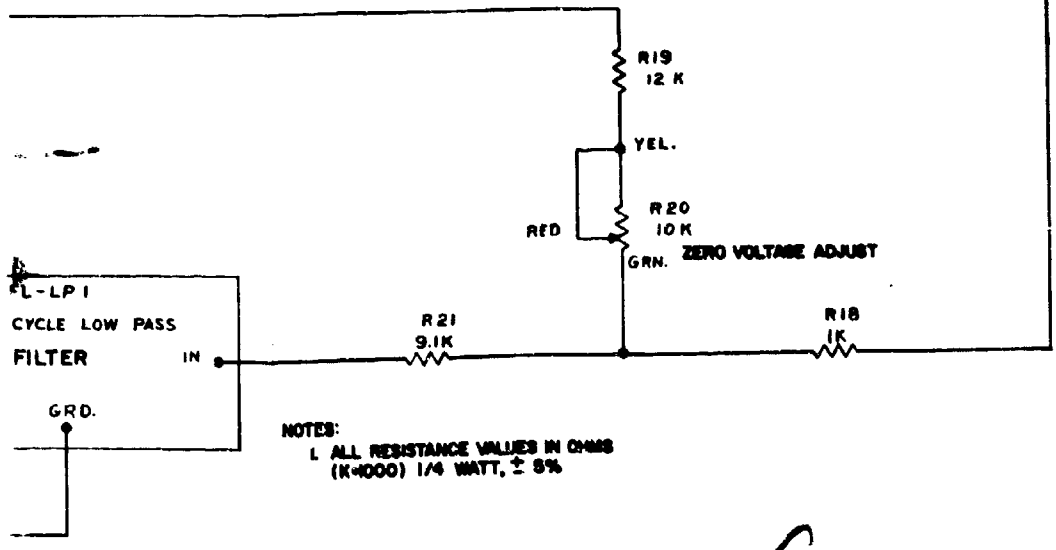
Reference Designation	Part No.	Vendor or Mfg. Spec.
C1	31-005 D	Electro Products Co. Pasadena, Calif.
C21, 2	1N1201	Hoffman Elect. Corp., Evanston, Ill.
C20, 4	1N2609	Hughes Products, Newport Beach, Calif.
Q1, 2	2N1308	RCA Corp. of America, Somerville, N. J.
Q3, 4	2N1309	RCA Corp. of America, Somerville, N. J.
Q5, 6, 9, 11	2N696	GEE Sprague, Denvers, Mass.
Q7, 10	2N696	Raytheon, Newton, Mass.
Q8	2N698	Transitron, Wakefield, Mass.
R1, 2, 5, 9, 10	RCR07G105J	MIL-R-11
R3, 7, 8, 12, 13, 14	RCR07G105J	MIL-R-11
R4	RCR07G682J	MIL-R-11
R6, 11, 15	RCR07G101J	MIL-R-11
R16, 18	1N3600A1-20	MIL-R-11
R17	RCR07G104J	MIL-R-11
R19	RCR07G103J	MIL-R-11
R20	1N6L-1-174	Beede Lab., Inc., Riverside, Calif.
R21	RCR07G915J	MIL-R-11
R22	RCR07G104J	MIL-R-11
R23	RCR07G913J	MIL-R-11
FL-LP-1	06-1681	Perromagnetics, Palo Alto, Calif.

A


DUAL EMITTER FOLLOWER
KEYING CIR
B
+20 V
CR-1
IN1351
R5
1K
R8
100
Q1
2N1305
R7
10K
SYNC LEVEL FROM
CHANNEL 9
R1
1K
R9
10K
Q4
2N438
R2
1K
Q2
2N1304
R10
10K
CR-2
IN1351
R11
100
R6
1K
R12
100
F
-20 V
R4
6.2K
Q3
2N438
D
GROUND
AND GATE
R3
10K
CR-3
IN625
d
PULSES FROM
PULSE GENERATORS
OR MATRICES
e
CR-4
IN625
OUTPUT
TO REFERENCE AMPLIFIER
f
FL-LP 1
250 CYCLE LOW PASS
OUT
FILTER
IN
GRD.

B

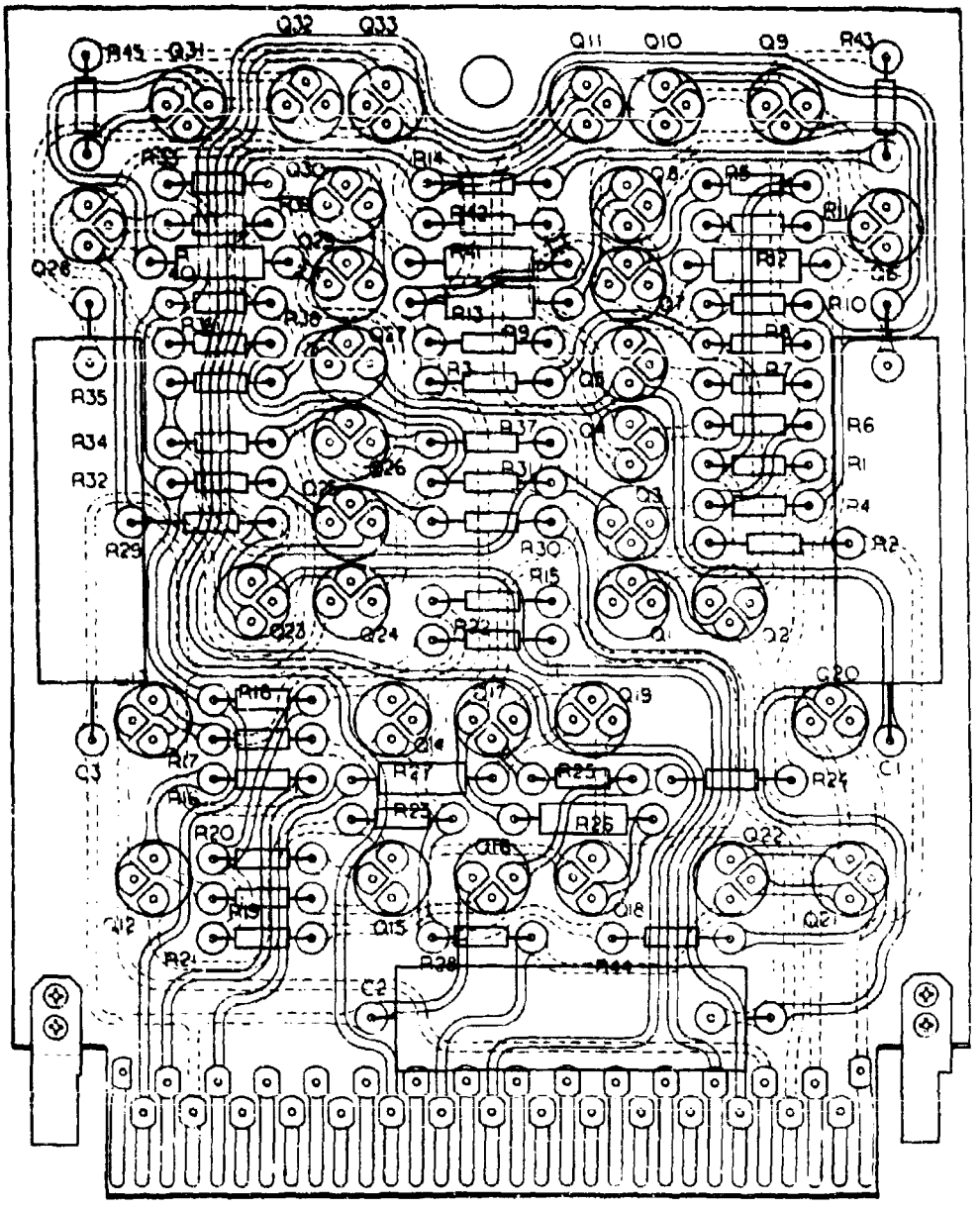




NOTES:
1. ALL RESISTANCE VALUES IN OHMS (K=1000) 1/4 WATT, ± 5%

C

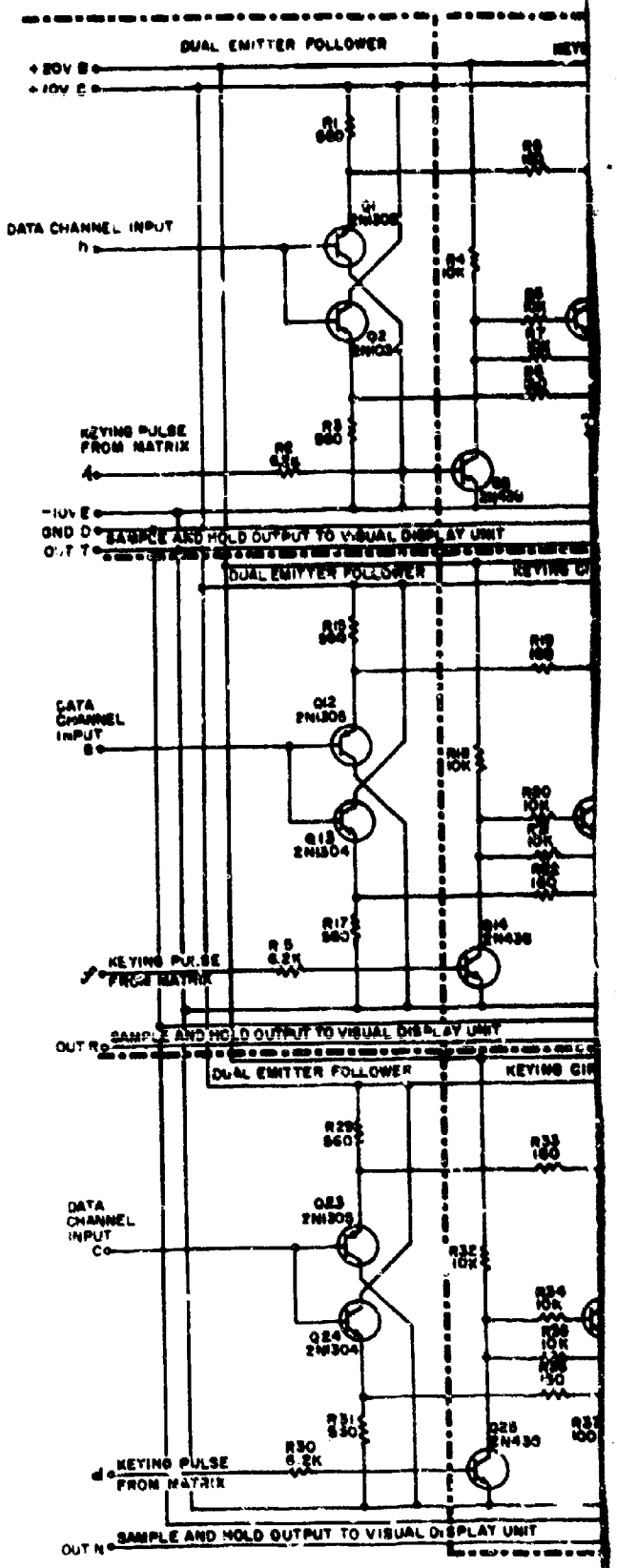
Fig. A-51 DC Reference Filter



PARTS LIST

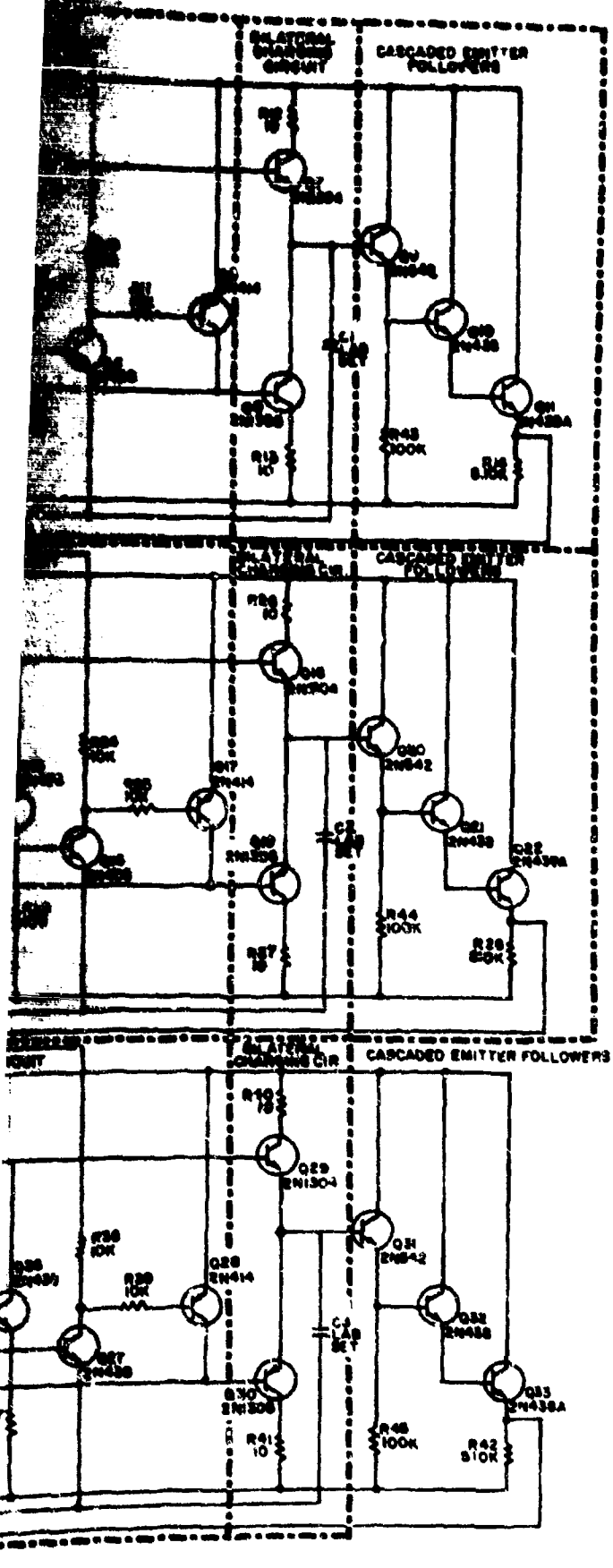
Reference Designation	Part No.	Vendor or MIL Spec.
C1, 2, 3	EL-205D-209	Electron Products, Pasadena, Calif.
Q1, 6, 12, 19, 23, 30	2N1305	RCA, Somerville, New Jersey
Q2, 7, 13, 18, 24, 29	2N1304	RCA, Somerville, New Jersey
Q3, 4, 5, 10, 14, 15, 16, 21, 25, 26, 27, 32	2N438	CBS-Hytron, Danvers, Mass.
Q8, 17, 28	2N414	Raytheon Mfg. Co., Newton, Mass.
Q9, 20, 31	2N542	Transitron, Wakefield, Mass.
Q11, 22, 33	2N438A	CBS-Hytron, Danvers, Mass.
R1, 3, 16, 17, 29, 31	RC07GF561J	MIL-R-11
R2, 15, 30	RC07GF822J	MIL-R-11
R4, 6, 7, 10, 11, 18, 20, 21, 24, 25, 32, 34, 35, 36, 39	RC07GF103J	MIL-R-11
R5, 8, 19, 22, 33, 36	RC07GF161J	MIL-R-11
R9, 23, 37	RC07GF101J	MIL-R-11
R12, 13, 26, 27, 40, 41	MS35043-39	MIL-R-11
R14, 28, 42	RC07GF512J	MIL-R-11
R43, 44, 45	RC07GF104J	MIL-R-11

A



B

Revised 25 June 1960



NOTES: UNLESS OTHERWISE SPECIFIED
1 ALL RESISTANCE VALUES IN OHMS
(K=1000) 5%, 1/4 WATT

C

Fig. A-52 Sample and Hold

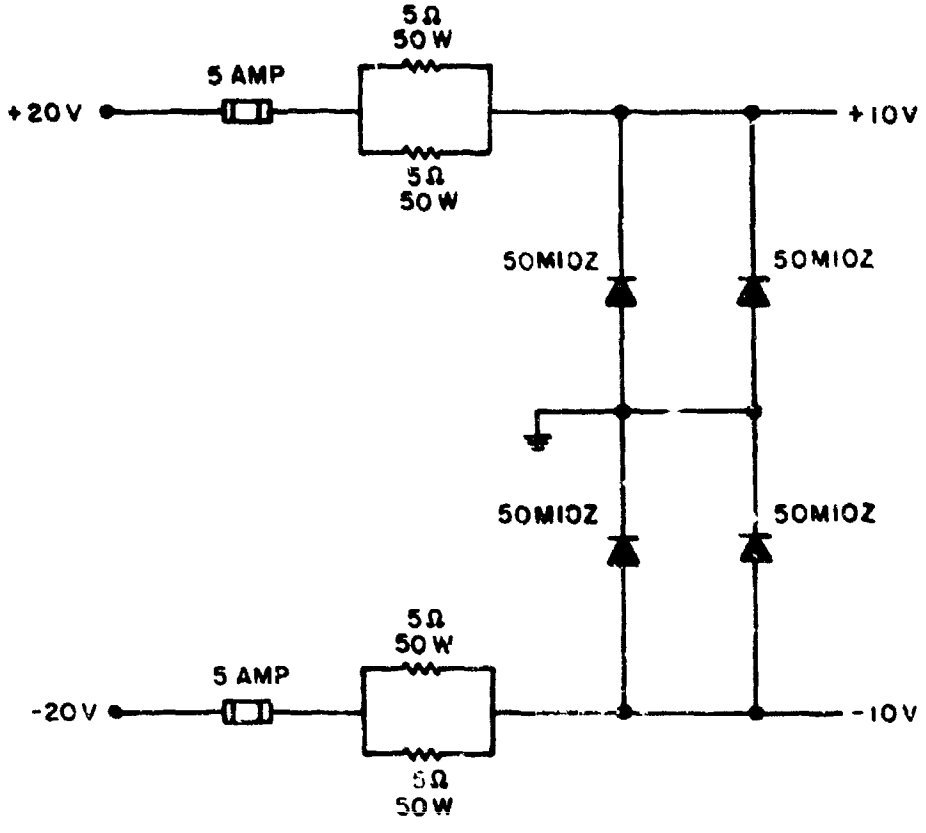
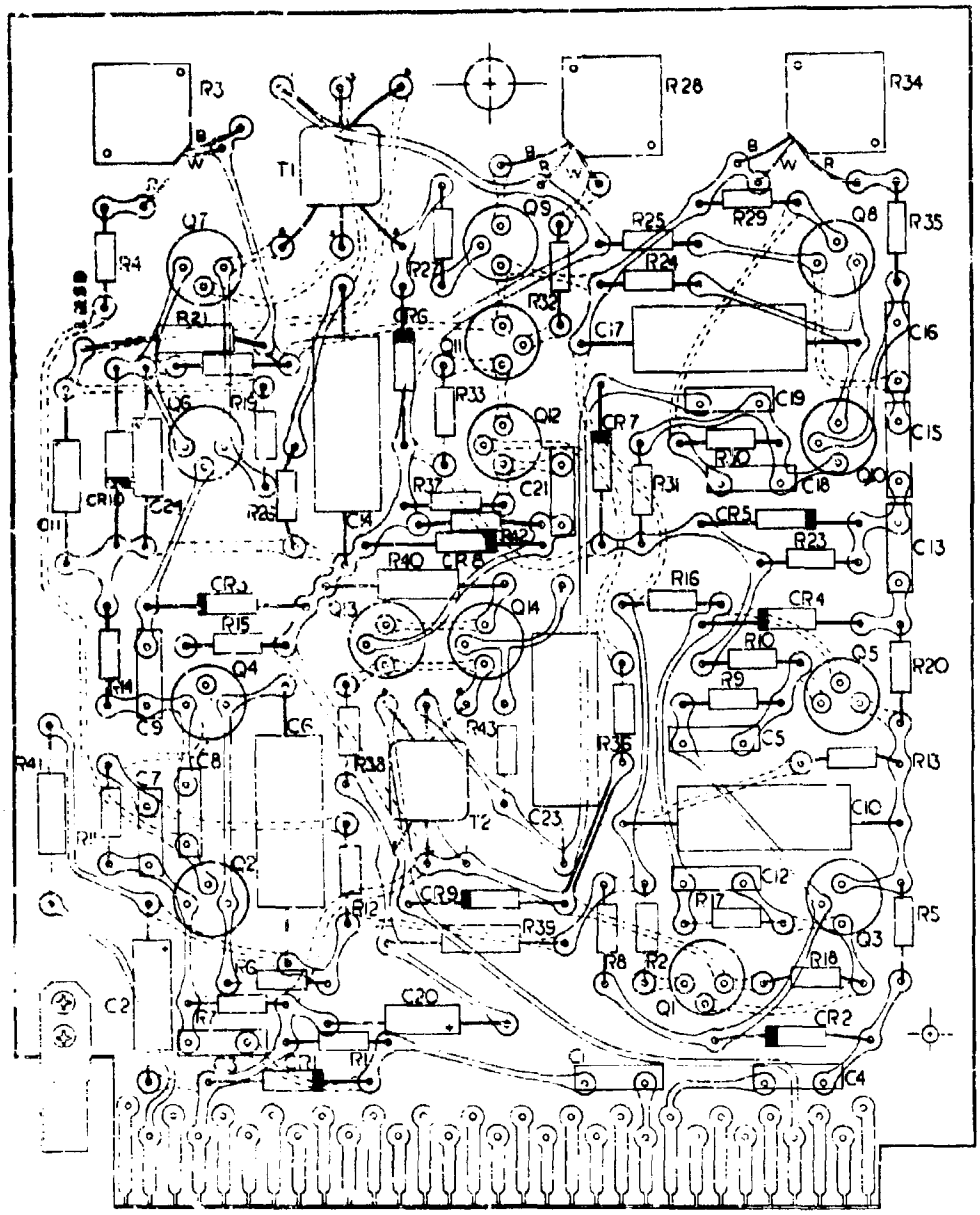
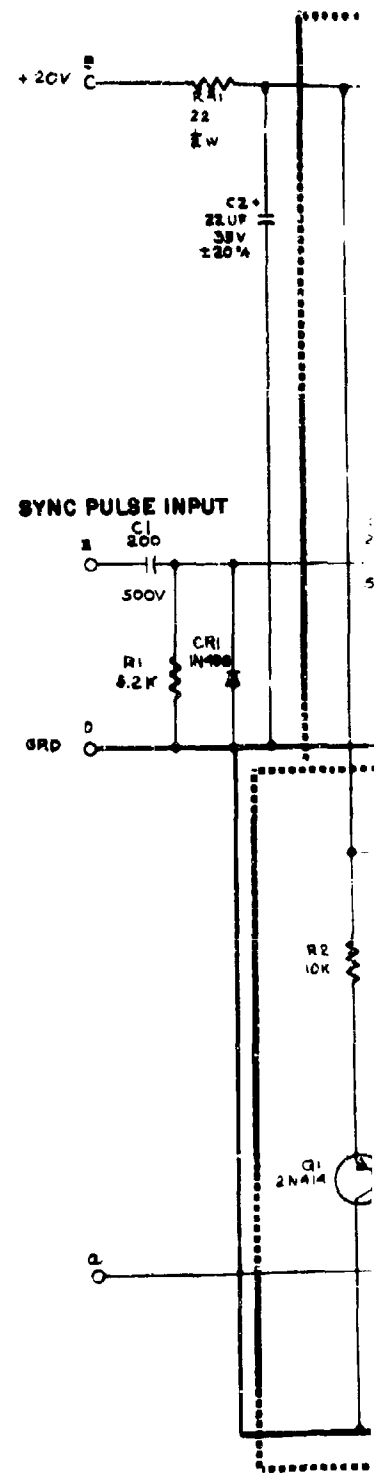


Fig. A-53 Plus/Minus 10-Volt Regulator

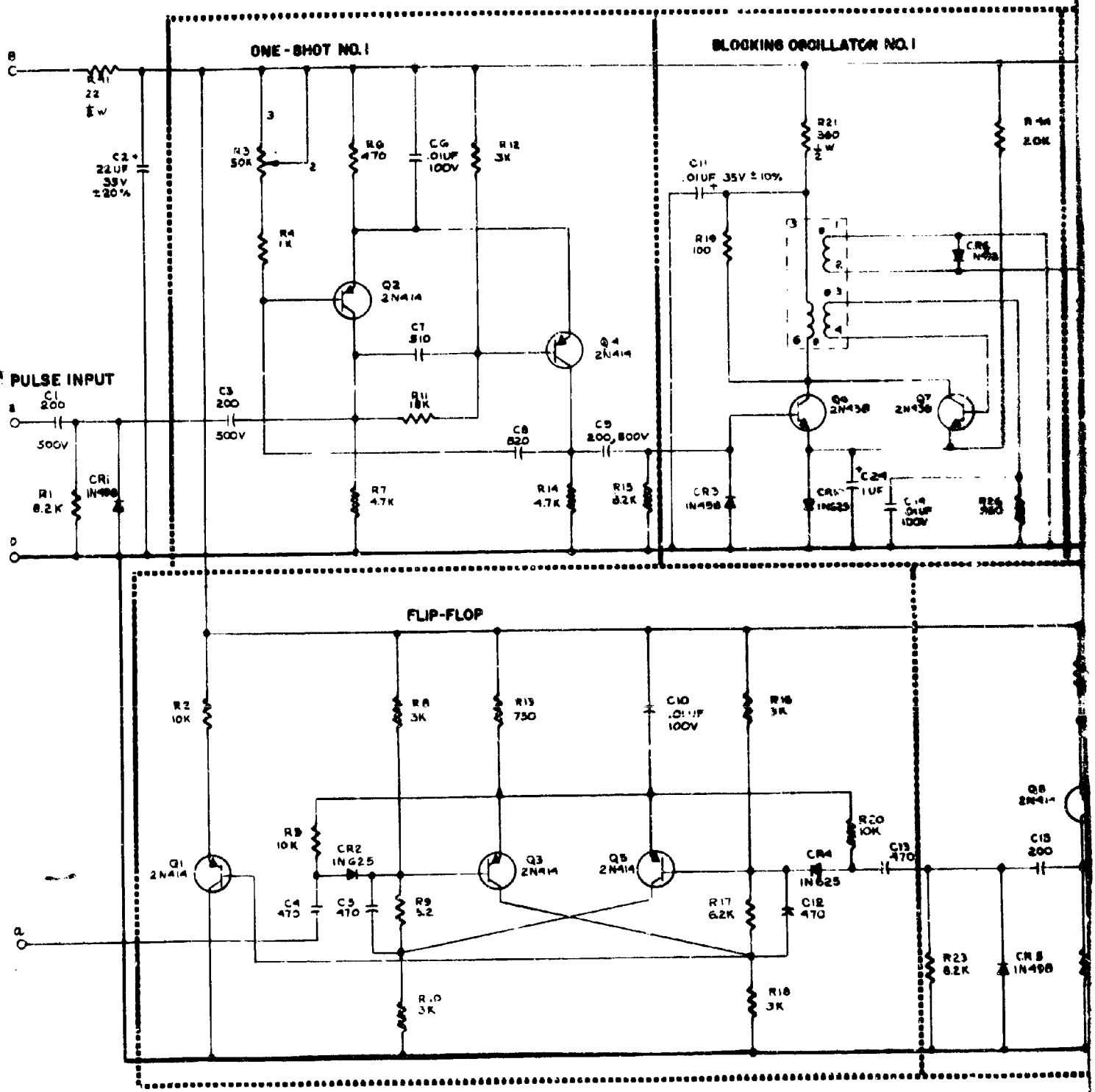




PARTS LIST

Reference Designation	Part No	Vendor or MIL Spec
C1, 3, 9, 10, 11, 21	[illegible]	El Monte, Los Angeles, Calif
C2	[illegible]	Sprague Electric Co., North Adams, Mass
C4, 5, 12, 13	[illegible]	El Monte, Los Angeles, Calif
C6, 14, 17, 23	[illegible]	Sprague Electric Co., North Adams, Mass.
C7, 15	[illegible]	El Monte, Los Angeles, Calif
C8, 16	[illegible]	El Monte, Los Angeles, Calif
C18, 24	[illegible]	Sprague Electric Co., North Adams, Mass.
C24	[illegible]	Sprague Electric Co., North Adams, Mass.
CR1, 3, 5 thru 8	1N446	[illegible] Dayrex, Mass.
CR2, 4, 10	1N645	Pacific Semiconductor, Culver City, Calif.
Q1 thru 5, 8, 10	2N414	Raytheon, Newton, Mass
Q6, 7, 9, 11, 12, 14	2N446	CBS-Hytron, Danvers, Mass.
Q13	2N416	CBS-Hytron, Danvers, Mass
R1, 18, 29, 40	RC07GF[illegible]	MIL-R-11
R2, 4, 30, 32	RC07GF[illegible]	MIL-R-11
R3, 34	RW-69-[illegible]	Dynamics Pacific, Santa Monica, Calif and MIL-R-11
R5, 35	RC07GF[illegible]	MIL-R-11
R6, 36	RC07GF[illegible]	MIL-R-11
R7, 14, 15, 31, [illegible]	RC07GF[illegible]	MIL-R-11
R8, 16, 18, 19	RC07GF[illegible]	MIL-R-11
R9, 17	RC07GF[illegible]	MIL-R-11
R11, 39	RC[illegible]	MIL-R-11
R13	[illegible]	MIL-R-11
R19, 38	RC07GF[illegible]	MIL-R-11
R21, 28	RN60D[illegible]	MIL-R-11
R22, 42	RWC 2[illegible]	MIL-R-11
R24, 44	RC07GF[illegible]	MIL-R-11
R33	RW 69-[illegible]	Dynamics Pacific, Santa Monica, Calif and MIL-R-11
R23, 25	R-07GF[illegible]	MIL-R-11
R41	[illegible]	MIL-R-11
R44	RC07GF[illegible]	MIL-R-11
T1, 2	10T-8-[illegible]	Chelmsford, Mass Moscow, Calif

A


ONE-SHOT NO.1
BLOCKING OSCILLATOR NO.1
PULSE INPUT
FLIP-FLOP
B
C
D
a
b
R41 22 ½W
C2 22UF 35V ±20%
R3 50K
R10 470
C6 .01UF 100V
R12 3K
R4 1K
Q2 2N414
C7 510
Q4 2N414
C1 200 500V
C3 200 500V
R11 18K
C8 820
C9 200, 500V
R1 8.2K
CR1 IN498
R7 4.7K
R14 4.7K
R15 8.2K
R21 360 ½W
R44 2.0K
C11 .01UF 35V ±10%
R19 100
CR6 IN498
Q6 2N438
Q7 2N438
CR3 IN498
CR5 IN625
C24 1UF
C19 .01UF 100V
R26 360
R2 10K
R8 3K
R13 750
C10 .01UF 100V
R16 3K
R20 10K
Q8 2N414
C13 470
C18 200
R9 10K
CR2 IN625
Q1 2N414
Q3 2N414
Q5 2N414
CR4 IN625
C4 470
C5 470
R9 5.2
R17 6.2K
C12 470
R23 8.2K
CR8 IN498
R10 3K
R18 3K

B

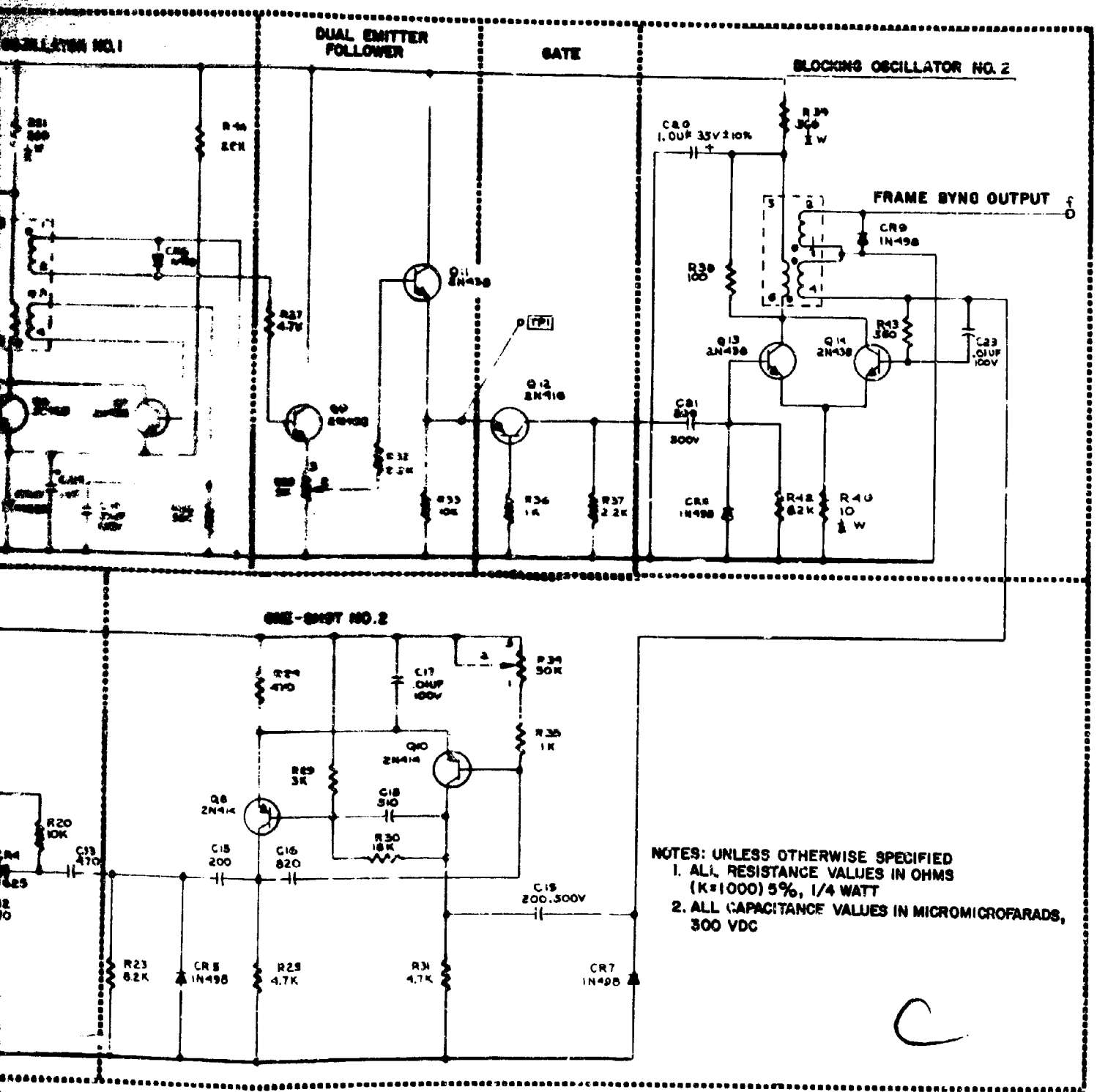
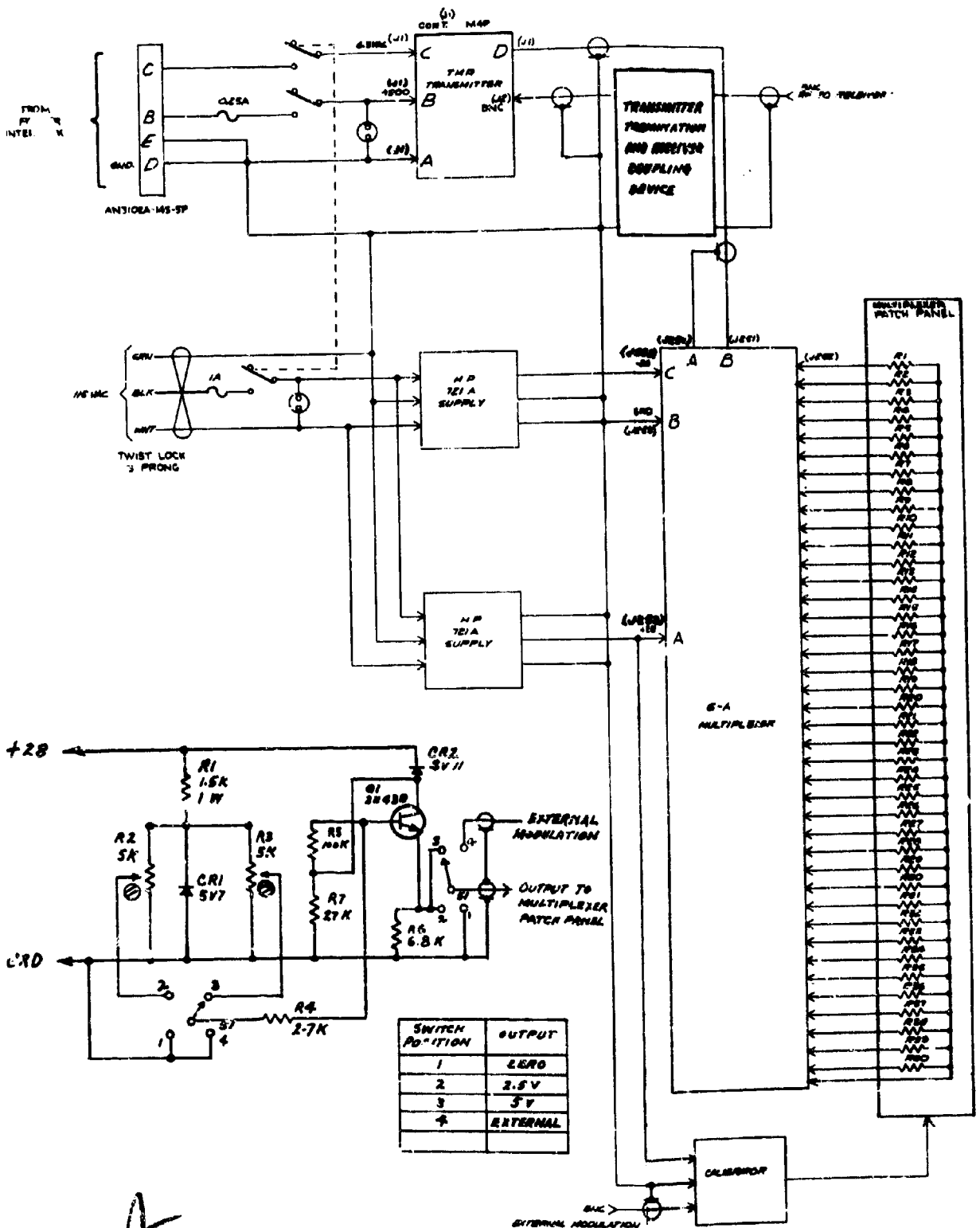
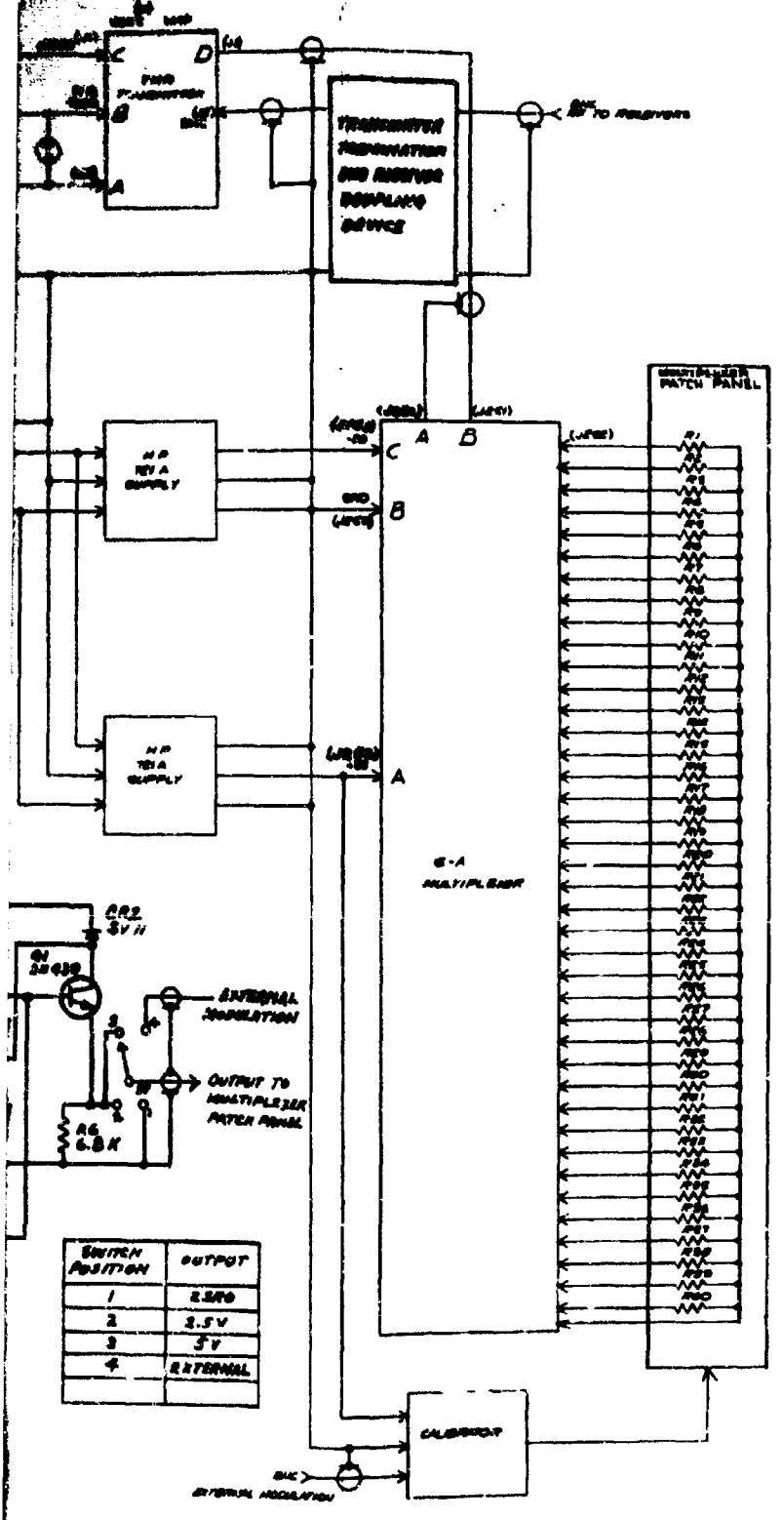


Fig. A-54 Frame Sync Delay Reproduce, G-A



SWITCH POSITION	OUTPUT
1	ZERO
2	2.5 V
3	5 V
4	EXTERNAL



B

Fig. A-55 Test Signal Generator